

## 15W X-Band High Power Amplifier

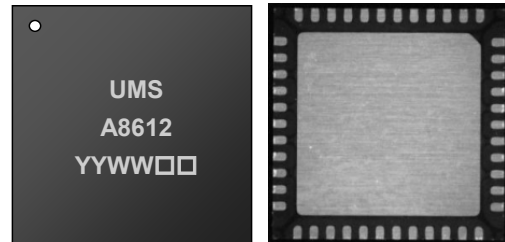
GaN Monolithic Microwave IC in SMD leadless package

### Description

The CHA8612-QDB is a two stage High Power Amplifier operating between 7.9 and 11GHz and providing typically 15W of saturated output power and 40% of Power Added Efficiency.

It is designed for a wide range of applications, from military to commercial radar and communication systems.

The circuit is manufactured with a GaN HEMT process, 0.25 $\mu$ m gate length, via holes through the substrate, air bridges and electron beam gate lithography.

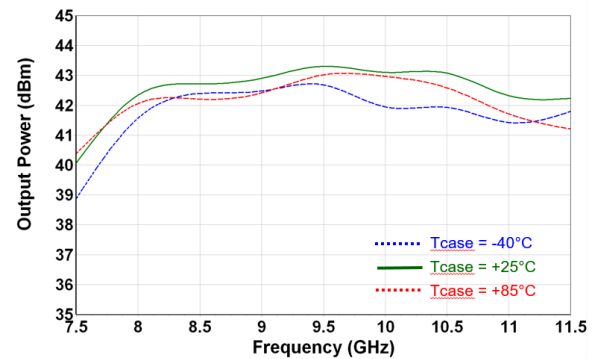


46 lead 7x7 mm QFN package

### Main Electrical Characteristics

- Broadband performances: 7.9-11GHz
- High output power: 15W
- High PAE: 40%
- Linear Gain: 26dB
- DC bias:  $V_d=30\text{Volt}$  @  $I_{dq}=680\text{mA}$
- MSL 3

Output power vs frequency  
 $P_{in} = 26\text{dBm}$



**Specifications (Pulsed mode)**

T<sub>case</sub> = +25°C, V<sub>d1</sub>=V<sub>d2</sub>=V<sub>d</sub> = +30V, I<sub>dq</sub> = 680mA, Pulse width = 25µs, Duty cycle = 10%.

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	7.9		11	GHz
Gain	Linear Gain		26		dB
Pout	Output Power (Pin = 26dBm)		42.5		dBm
PAE	Associated Power Added Efficiency (Pin = 26dBm)		40		%
I <sub>d</sub>	Associated current (Pin = 26dBm)		1.7		A
S <sub>11</sub>	Input Return Loss		8		dB
S <sub>22</sub>	Output Return Loss		10		dB
I <sub>dq</sub>	Quiescent Current		680		mA
V <sub>d</sub>	Drain bias Voltage		30		V
V <sub>g</sub>	Gate bias Voltage		-3.1		V

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board" at QFN reference plan.

**Specifications (CW mode)**

T<sub>case</sub> = +25°C, V<sub>d1</sub>=V<sub>d2</sub>=V<sub>d</sub> = +30V, I<sub>dq</sub> = 680mA, Pulse width = 25µs, Duty cycle = 10%.

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	7.9		11	GHz
Gain	Linear Gain		25		dB
Pout	Output Power (Pin = 26dBm)		42.5		dBm
PAE	Associated Power Added Efficiency (Pin = 26dBm)		35		%
I <sub>d</sub>	Associated current (Pin = 26dBm)		1.7		A
S <sub>11</sub>	Input Return Loss		8		dB
S <sub>22</sub>	Output Return Loss		10		dB
I <sub>dq</sub>	Quiescent Current		680		mA
V <sub>d</sub>	Drain bias Voltage		30		V
V <sub>g</sub>	Gate bias Voltage		-3.1		V

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board" at QFN reference plan.

**Absolute Maximum Ratings** <sup>(1)</sup>T<sub>case</sub>= +25°C

Symbol	Parameter	Values	Unit
V <sub>d</sub>	Drain bias voltage	35	V
I <sub>dq</sub>	Drain bias current	1	A
P <sub>in</sub>	Maximum peak input power overdrive	+35	dBm
T <sub>j</sub>	Junction temperature <sup>(2)</sup>	230	°C

<sup>(1)</sup> Operation of this device above anyone of these parameters may cause permanent damage.

<sup>(2)</sup> See paragraph "Device thermal performances"

**Recommended Operating Range** <sup>(3), (4)</sup>

Symbol	Parameter	Values	Unit
V <sub>d</sub>	Drain bias voltage	30	V
I <sub>dq_stg1</sub>	Drain bias current	200	mA
I <sub>dq_stg2</sub>	Gate bias voltage	480	mA
P <sub>in</sub>	Maximum peak input power overdrive	28	dBm

<sup>(3)</sup> Electrical performances are defined for specified test conditions

<sup>(4)</sup> Electrical performances are not guaranteed over all recommended operating conditions

**Temperature Range**

T <sub>case</sub>	Operating temperature range	-40 to +85	°C
T <sub>stg</sub>	Storage temperature range	-55 to +150	°C

**Typical Bias Conditions**T<sub>case</sub>= +25°C

Symbol	Pad N°	Parameter	Values	Unit
VG1	13	DC Gate voltage 1 <sup>st</sup> stage	-3.1	V
VG2	18, 40	DC Gate voltage 2 <sup>nd</sup> stage	-3.1	V
VD1	15, 43	DC Drain voltage 1 <sup>st</sup> stage	30	V
VD2	22, 36	DC Drain voltage 2 <sup>nd</sup> stage	30	V

## “Power ON” sequence

1. Bias HPA gate voltage at  $V_g$  close to  $V_{pinch-off}$  (example:  $V_g \approx -5V$ ).
2. Apply  $V_d$  bias voltage (Example:  $V_d = 30V$ ).
3. Increase  $V_g$ s up to quiescent bias drain current  $I_{ds0}$  (680mA applied on the gate).
4. Apply RF signal.

## “Power OFF” sequence

1. Turn off RF signal.
2. Bias HPA gate voltage at  $V_g$  close to  $V_{pinch-off}$  (example:  $V_g \approx -5V$ ).
3. Set  $V_d$  to 0V.
4. Turn off  $V_d$  supply.
5. Turn off  $V_g$  supply.

**Device thermal performances**

All the figures given in this section are obtained assuming that the QFN device is only cooled down by conduction through the package thermal pad (to be adapted to the assembly/package) (no convection mode considered).

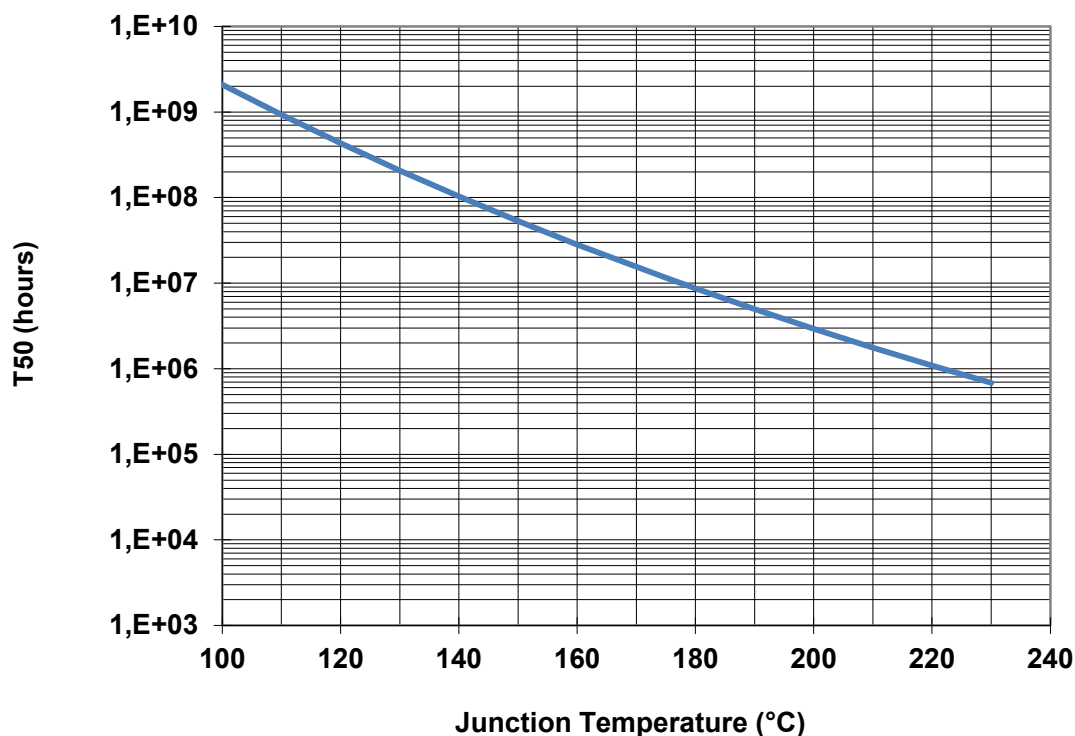
The temperature is monitored at the package back-side interface (Tcase).

The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Absolute Maximum Ratings table.

So, the system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	Tjunction (°C)	RTH (°CW)	T50 (hours)
RTH <sup>(1)</sup> Thermal Resistance (Junction to Case)	Vd= 30V Id_drive= 1.5A Pdiss= 30W CW	172	2.9	1.9E+07

<sup>1</sup> Assuming 85°C Tcase



### Typical Package Sij parameters

Tcase= +25°C, Vd1=Vd2=Vd = +30V, Id = 680mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
0.5	-1.73	159.93	-67.51	-40.69	-67.79	-62.92	-0.03	-16.04
1	-2.06	137.04	-68.88	-162.08	-27.79	53.40	-0.04	-31.48
1.5	-2.89	112.39	-61.27	109.99	-42.15	-42.37	-0.06	-46.69
2	-4.81	84.94	-67.56	-176.73	-53.30	-36.80	-0.09	-61.63
2.5	-8.55	55.72	-57.22	149.87	-51.83	-45.32	-0.09	-76.15
3	-15.84	25.51	-65.33	-126.74	-51.48	29.80	-0.11	-90.17
3.5	-32.59	-136.23	-57.99	-16.44	-40.08	28.87	-0.12	-104.09
4	-16.39	171.55	-53.98	123.47	-29.70	3.58	-0.09	-118.26
4.5	-12.26	150.60	-53.37	-128.54	-25.37	-60.43	-0.11	-132.71
5	-10.11	131.59	-58.56	127.58	-28.76	-94.21	-0.17	-148.19
5.5	-8.88	111.73	-49.72	-55.41	-26.28	-34.10	-0.25	-165.09
6	-8.01	89.26	-51.38	-91.64	-11.76	-44.21	-0.44	175.28
7	-7.16	16.16	-48.23	108.42	13.91	-149.83	-2.10	114.90
7.5	-10.04	-56.74	-53.28	-27.99	24.56	95.36	-7.05	63.82
8	-12.59	-118.63	-52.31	124.35	26.06	-19.74	-15.44	4.52
8.5	-11.27	177.03	-57.87	104.80	25.67	-108.27	-15.38	-110.69
9	-10.55	123.58	-51.89	-5.64	25.68	174.01	-11.19	-172.28
9.5	-11.38	70.00	-63.92	-89.20	26.18	95.94	-11.39	133.33
10	-12.76	3.86	-56.96	76.61	26.53	13.54	-17.10	74.67
10.5	-10.79	-72.40	-64.05	6.64	26.74	-74.77	-28.51	-12.03
11	-7.69	-142.22	-51.51	-48.36	26.27	-176.08	-17.76	-52.01
11.5	-11.13	175.95	-63.15	46.91	24.11	63.58	-8.16	-104.38
12	-5.30	177.36	-57.38	-146.96	12.98	-78.58	-4.44	-158.27
12.5	-4.84	141.77	-67.51	-40.69	-3.20	-159.10	-3.36	166.42
13	-5.18	120.58	-68.88	-162.08	-17.61	147.75	-2.54	138.18
13.5	-5.58	104.76	-61.27	109.99	-31.37	110.60	-2.03	113.99
14	-5.83	90.86	-67.56	-176.73	-49.43	81.73	-1.73	93.57
14.5	-6.13	78.66	-57.22	149.87	-55.08	-155.69	-1.48	76.42
15	-6.27	66.68	-65.33	-126.74	-53.22	95.12	-1.24	62.09
15.5	-6.45	55.27	-57.99	-16.44	-64.06	11.81	-0.98	49.78
16	-6.57	44.25	-53.98	123.47	-54.86	76.24	-0.69	39.40

## Typical Board Measurements (CW mode)

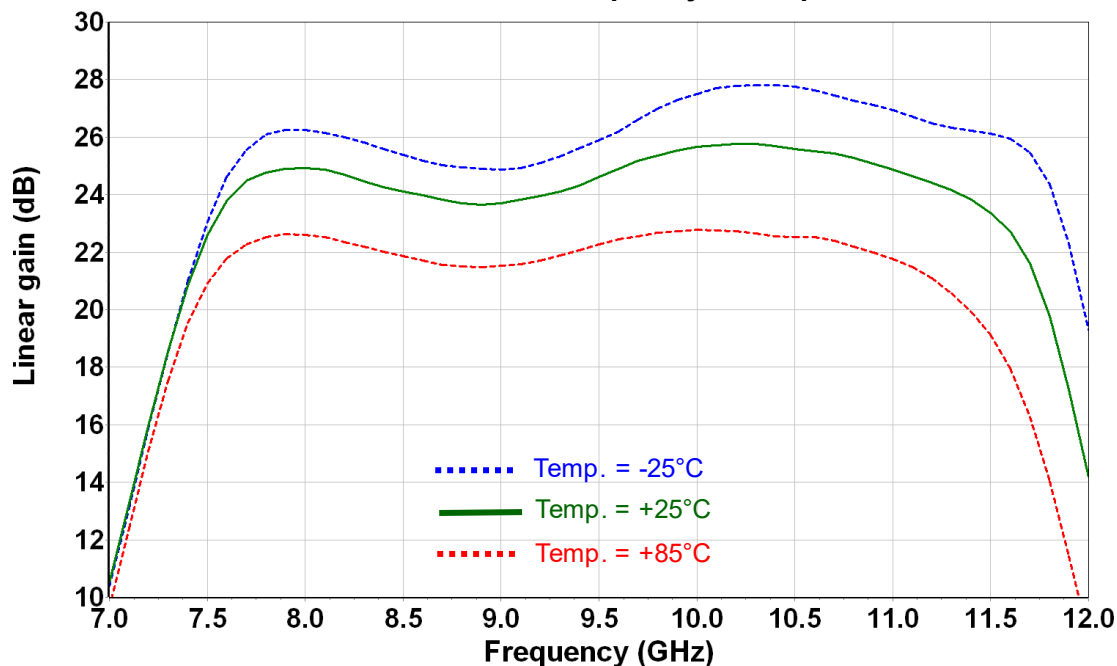
Vd1 = Vd2 = Vd = +30V. Idq = 680mA.

Tcase = -25°C. +25°C. +85°C

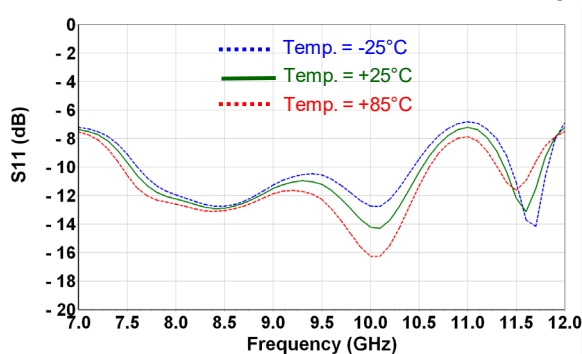
Measurements are given in the connectors access plans using the proposed land pattern and board given in the paragraph "Evaluation mother board".

For these measurements, losses due to board are not de-embedded.

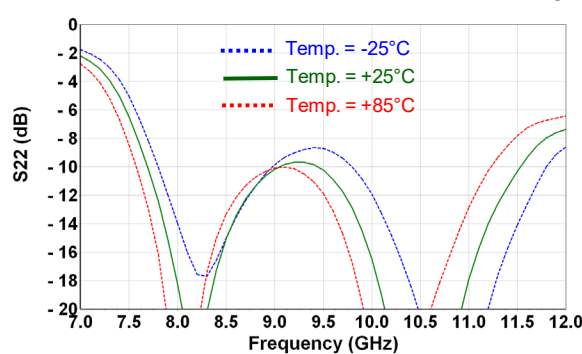
### Linear Gain versus Frequency & Temperature



### Input Return Loss versus Frequency



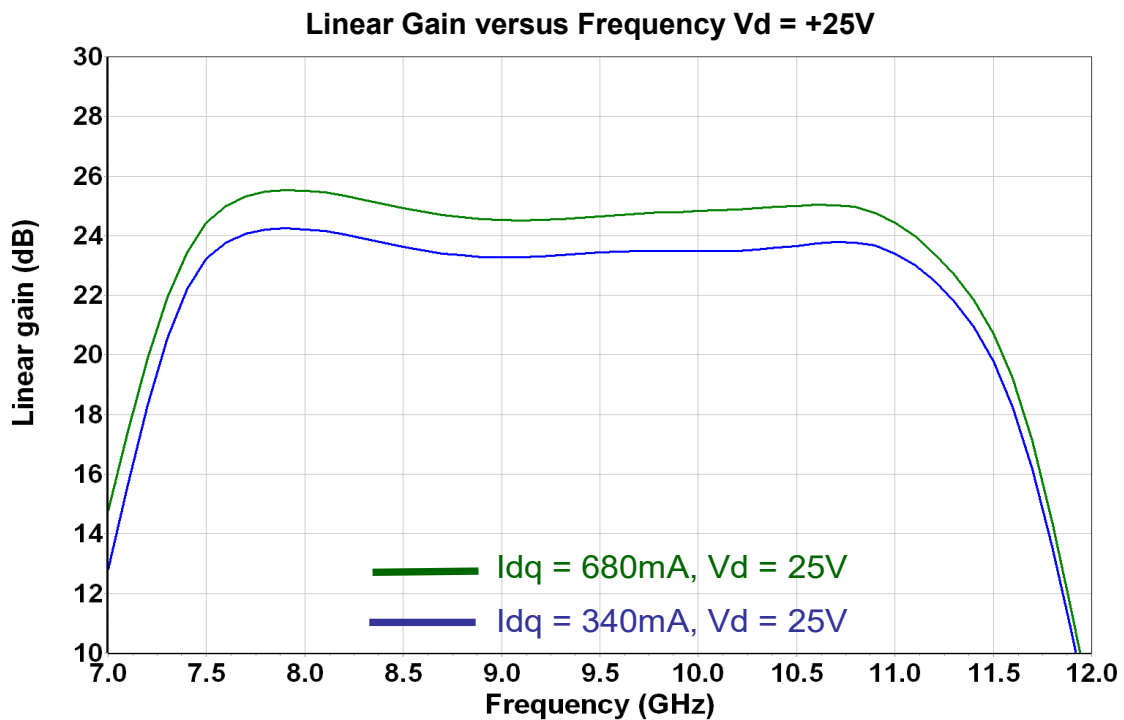
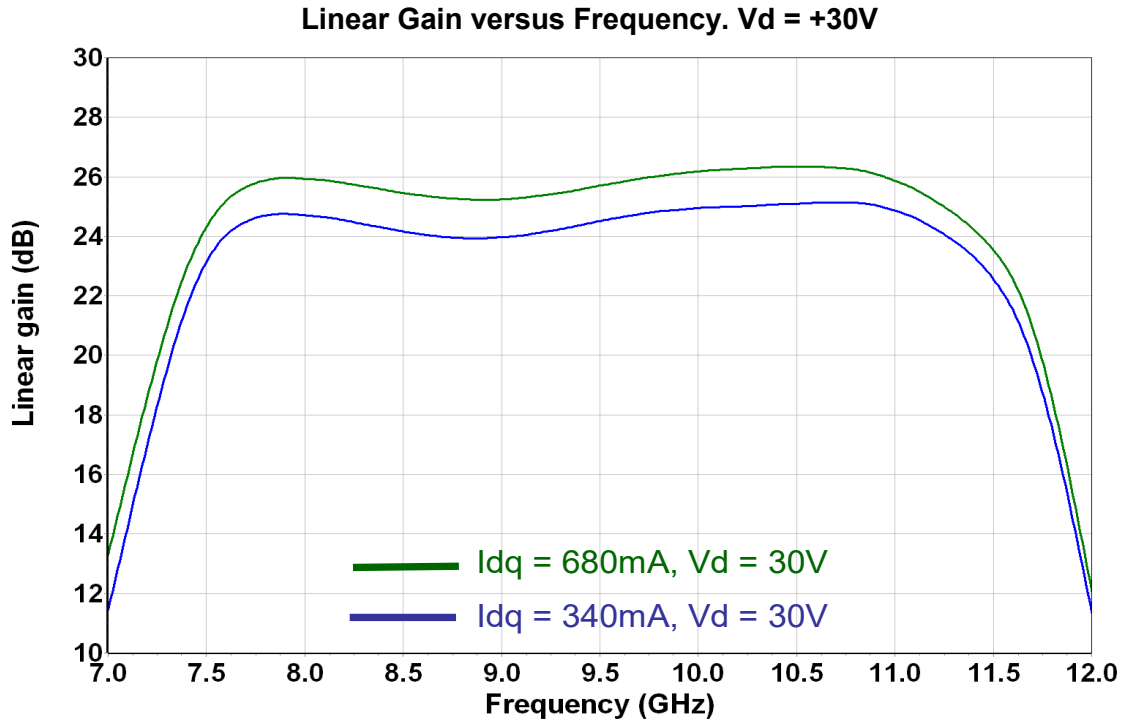
### Output Return Loss versus Frequency



## Typical Board Measurements (Pulsed mode)

T<sub>case</sub> = +25°C. Pulse width = 25µs. Duty cycle = 10%.

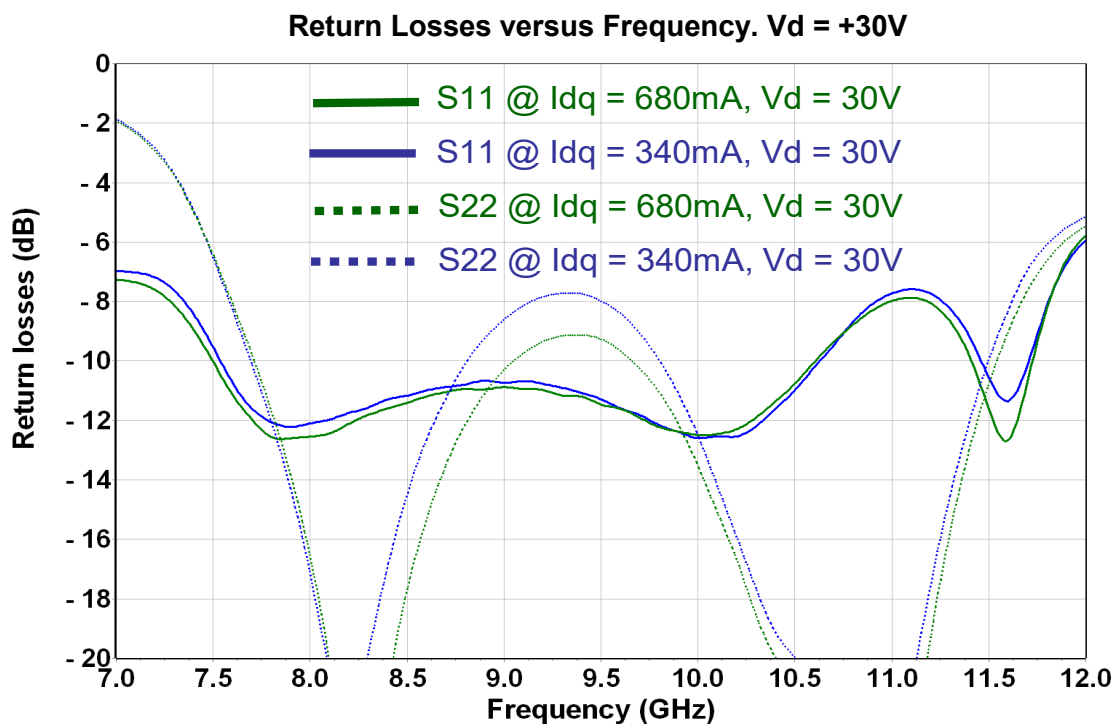
Measurements are given in the QFN access plans.





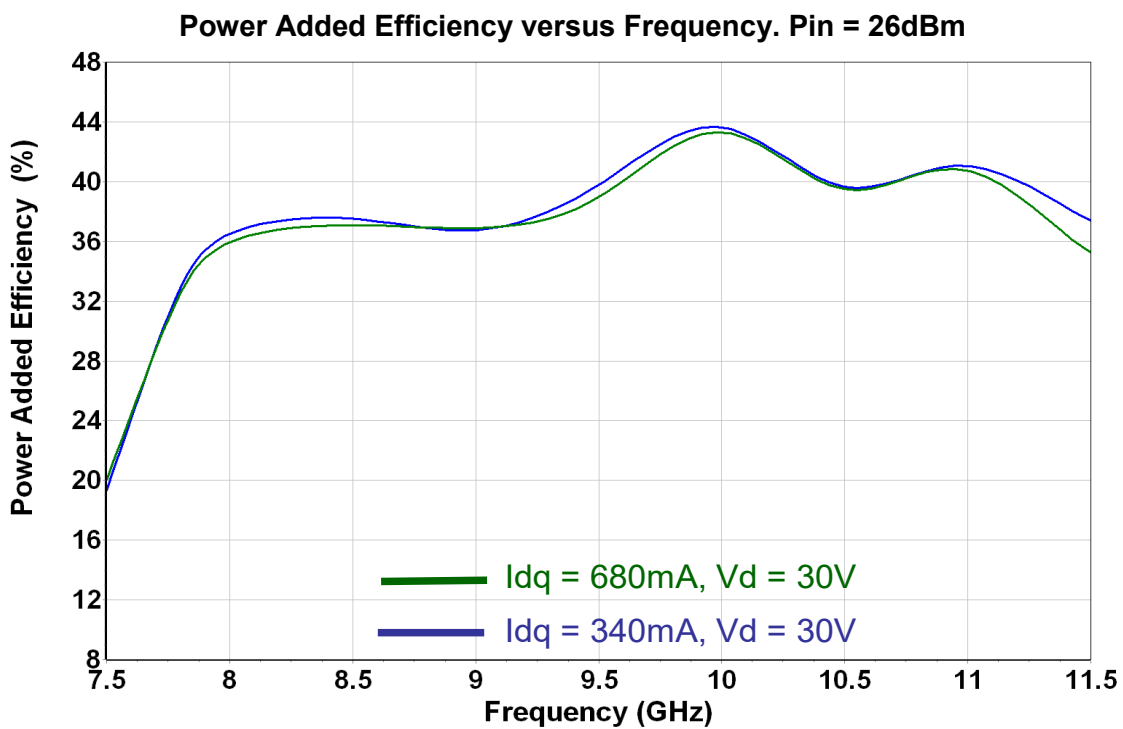
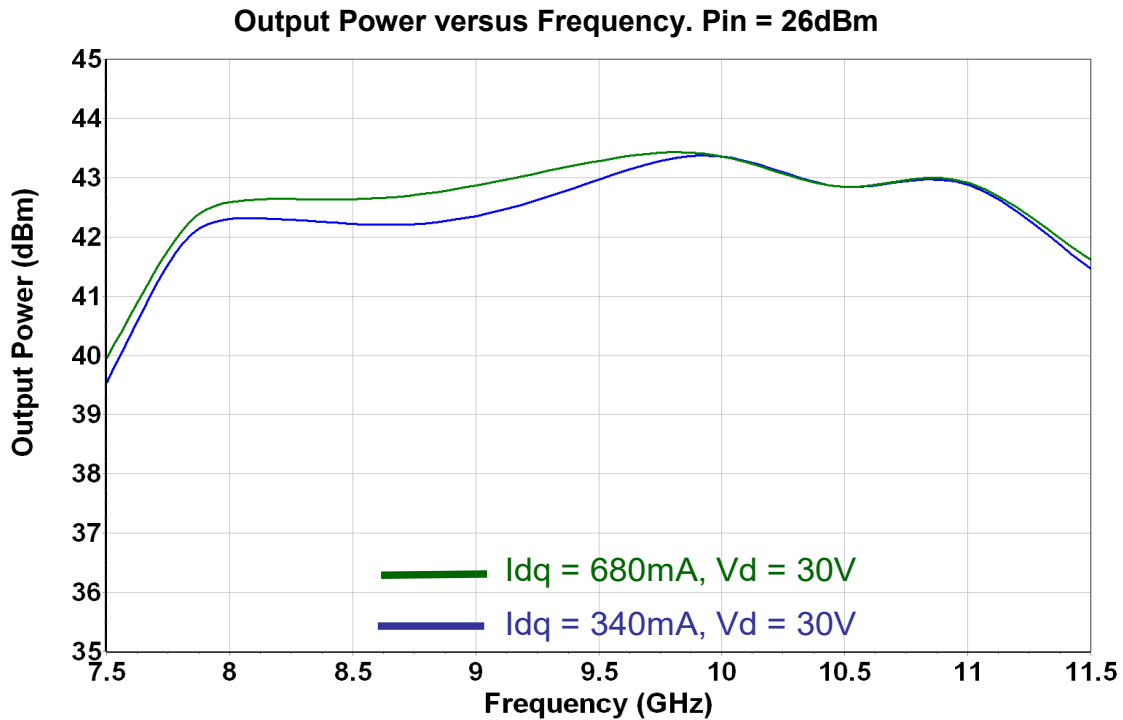
Typical Board Measurements (Pulsed mode)

Tcase = +25°C. Pulse width = 25µs. Duty cycle = 10%.



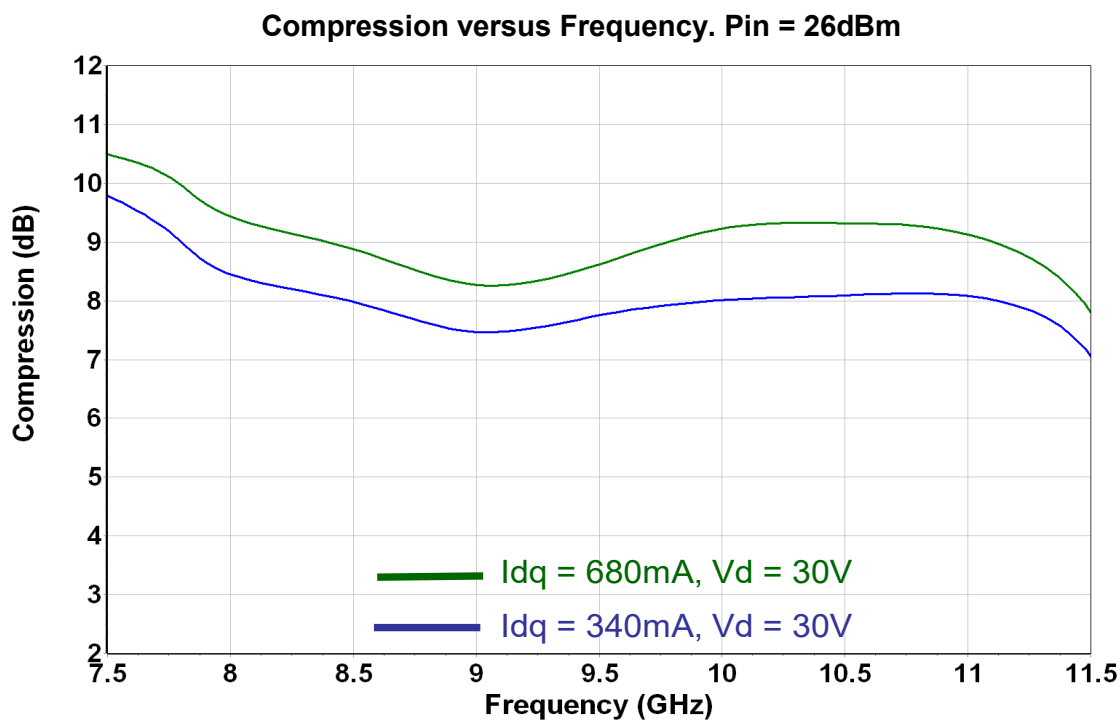
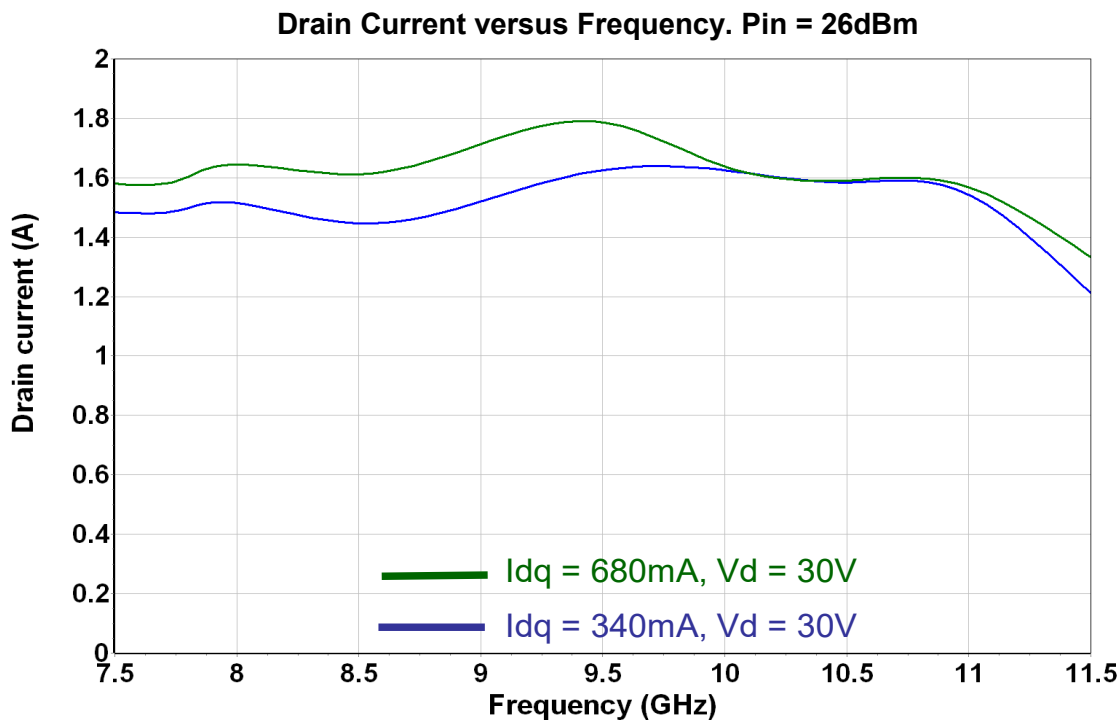
## Typical Board Measurements (Pulsed mode)

T<sub>case</sub> = +25°C. V<sub>d1</sub> = V<sub>d2</sub> = V<sub>d</sub> = +30V. Pulse width = 25µs. Duty cycle = 10%.



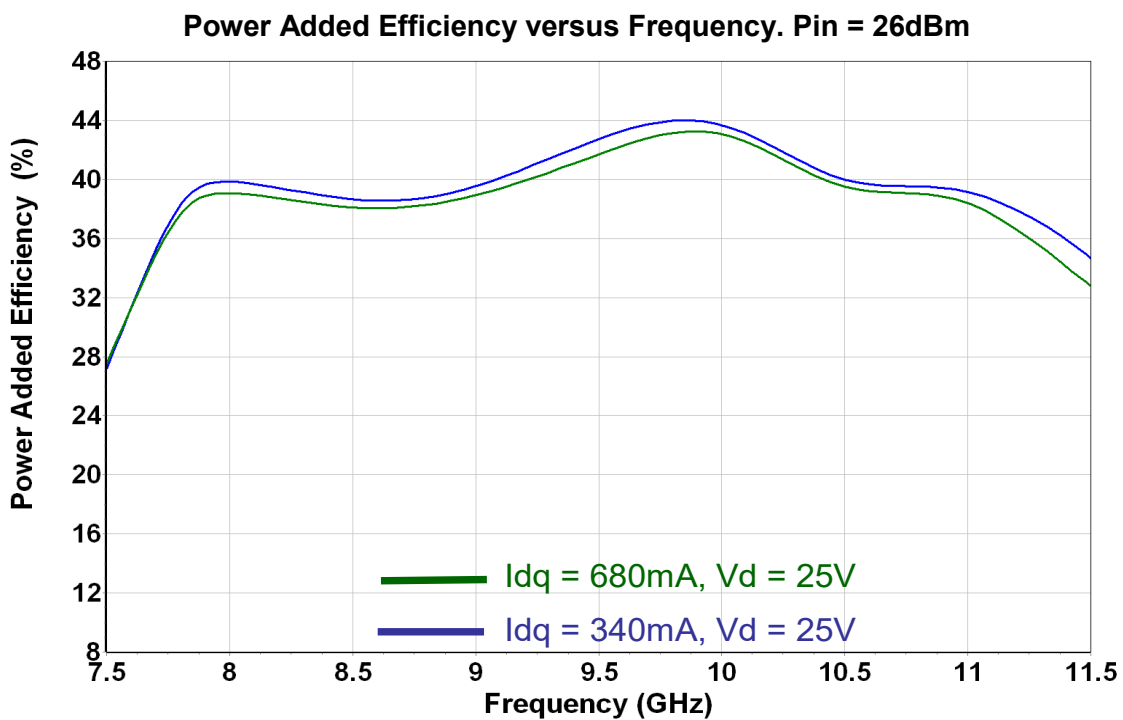
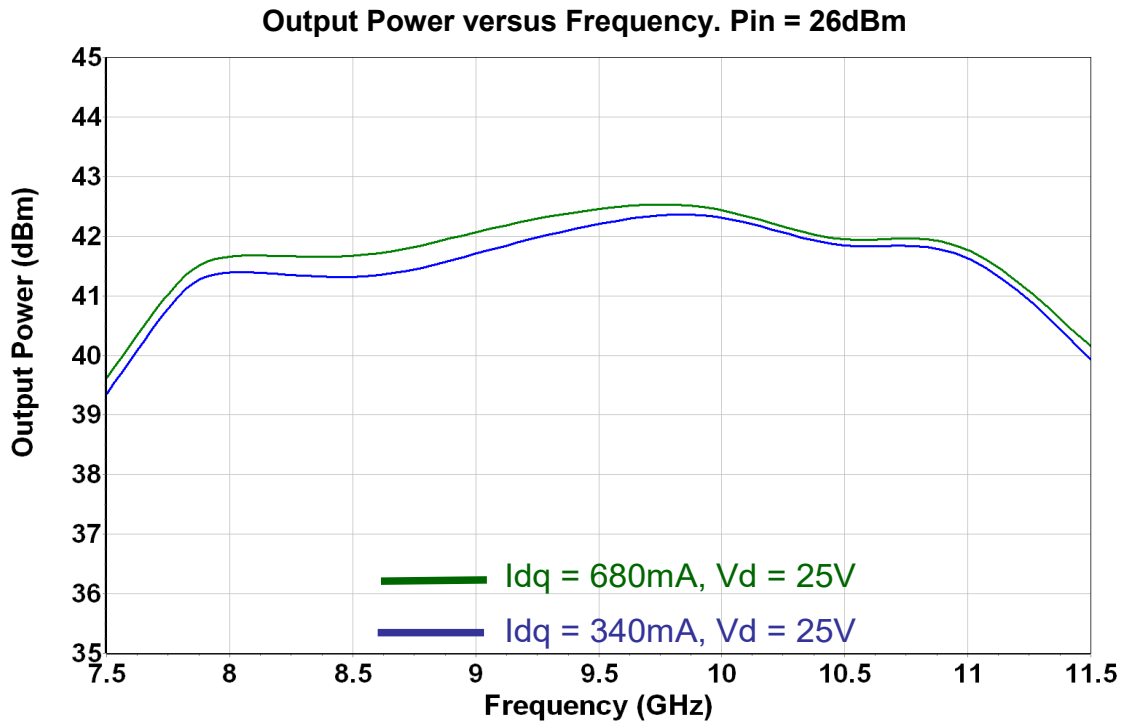
**Typical Board Measurements (Pulsed mode)**

T<sub>case</sub> = +25°C. V<sub>d1</sub> = V<sub>d2</sub> = V<sub>d</sub> = +30V. Pulse width = 25µs. Duty cycle = 10%.



## Typical Board Measurements (Pulsed mode)

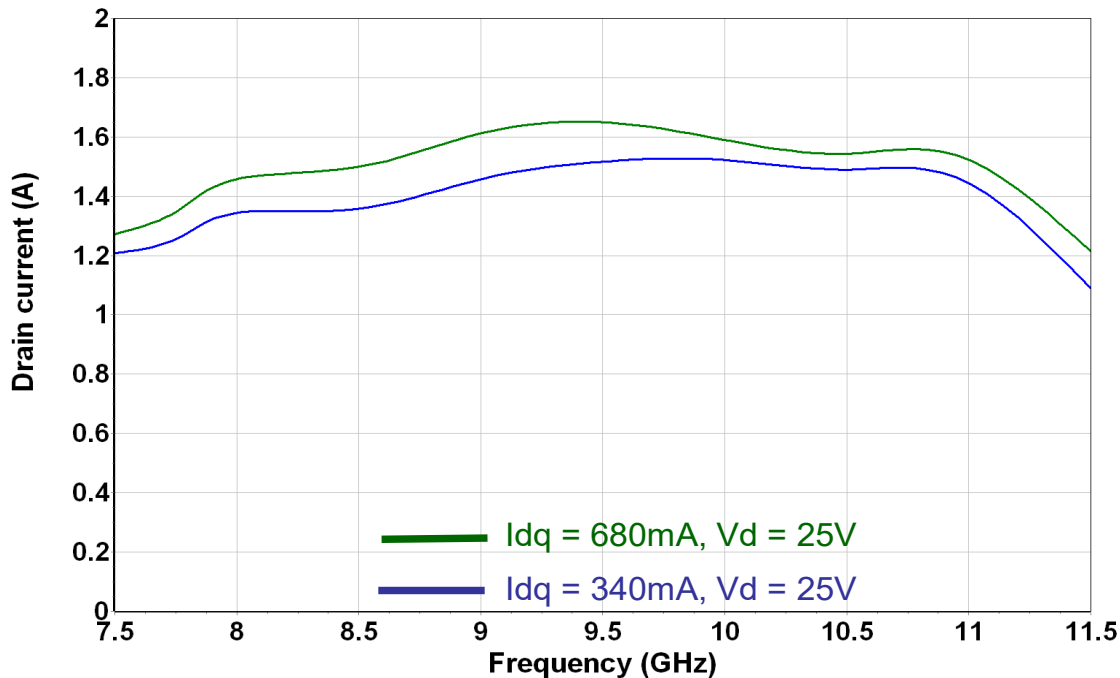
T<sub>case</sub> = +25°C. V<sub>d1</sub> = V<sub>d2</sub> = V<sub>d</sub> = +25V. Pulse width = 25µs. Duty cycle = 10%.



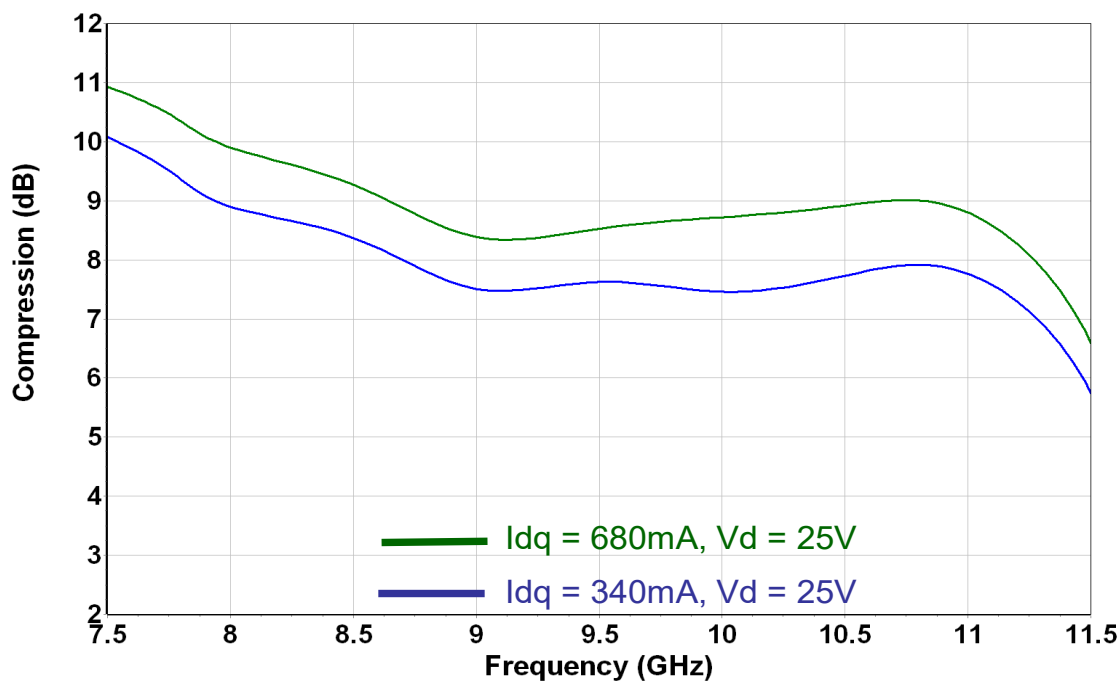
**Typical Board Measurements (Pulsed mode)**

T<sub>case</sub> = +25°C. V<sub>d1</sub> = V<sub>d2</sub> = V<sub>d</sub> = +25V. Pulse width = 25µs. Duty cycle = 10%.

**Drain Current versus Frequency. Pin = 26dBm**



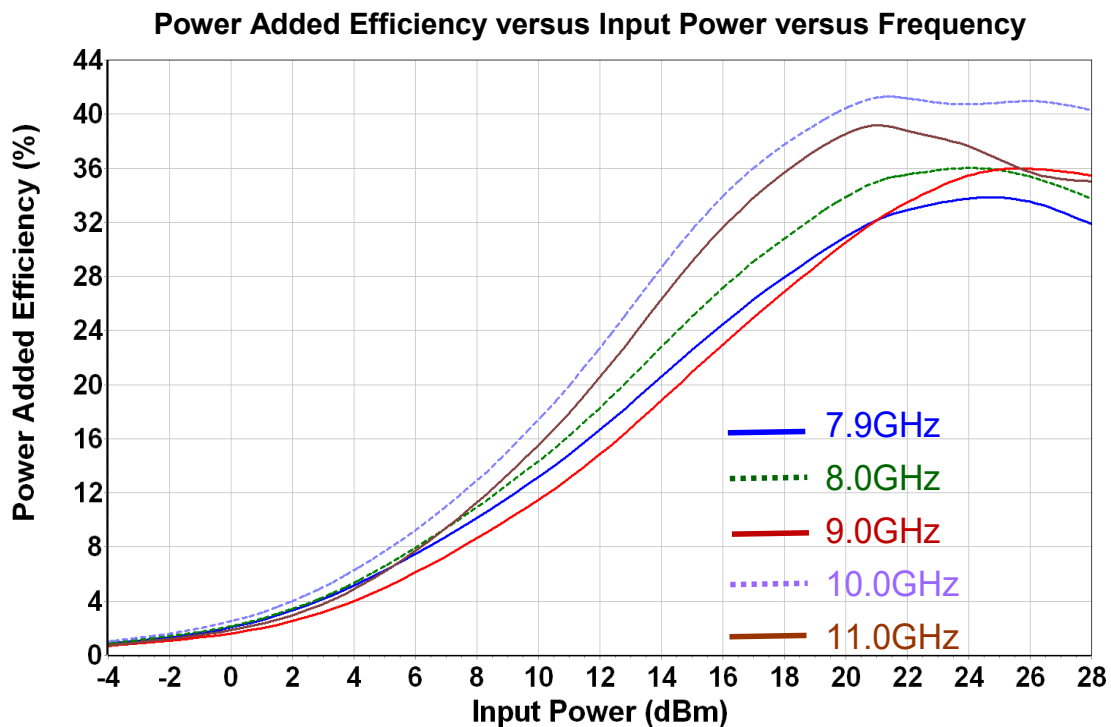
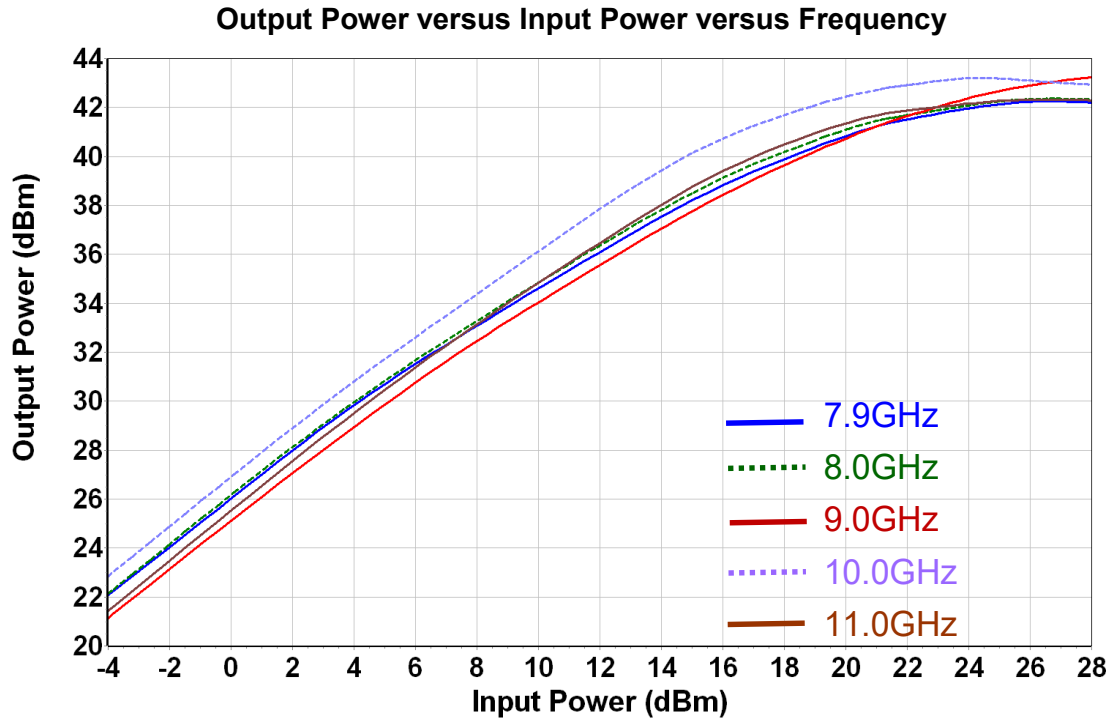
**Compression versus Frequency. Pin = 26dBm**



## Typical Board Measurements (Pulsed mode)

Tcase = +25°C. Vd1 = Vd2 = Vd = +30V. Idq = 680mA.

Pulse width = 25µs. Duty cycle = 10%.

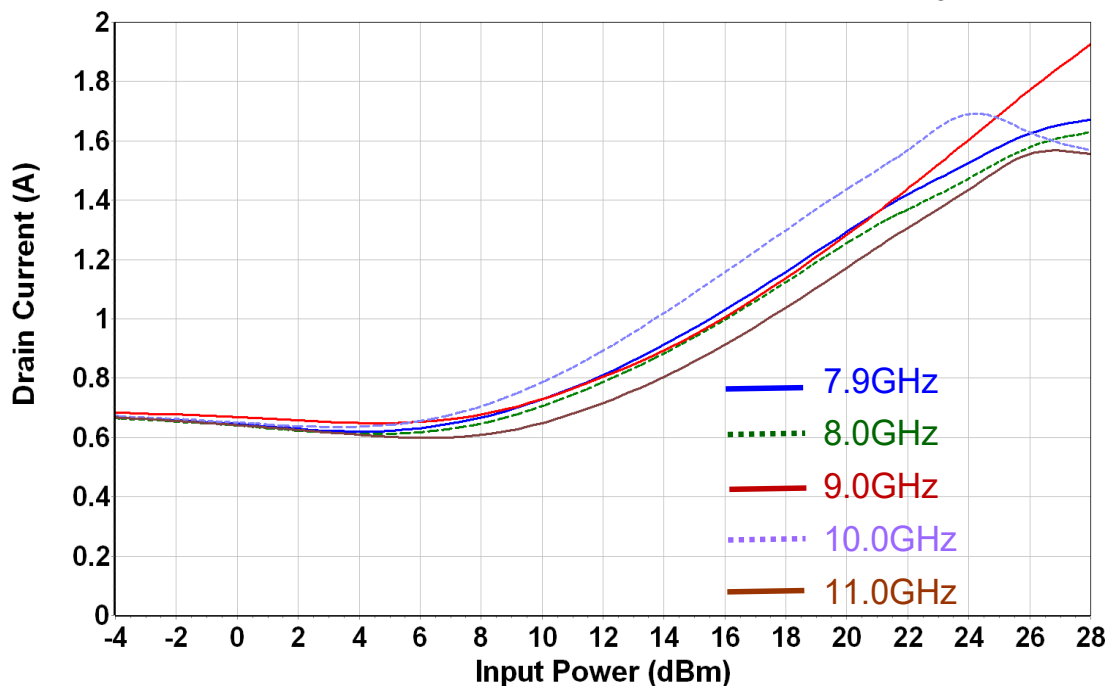


## Typical Board Measurements (Pulsed mode)

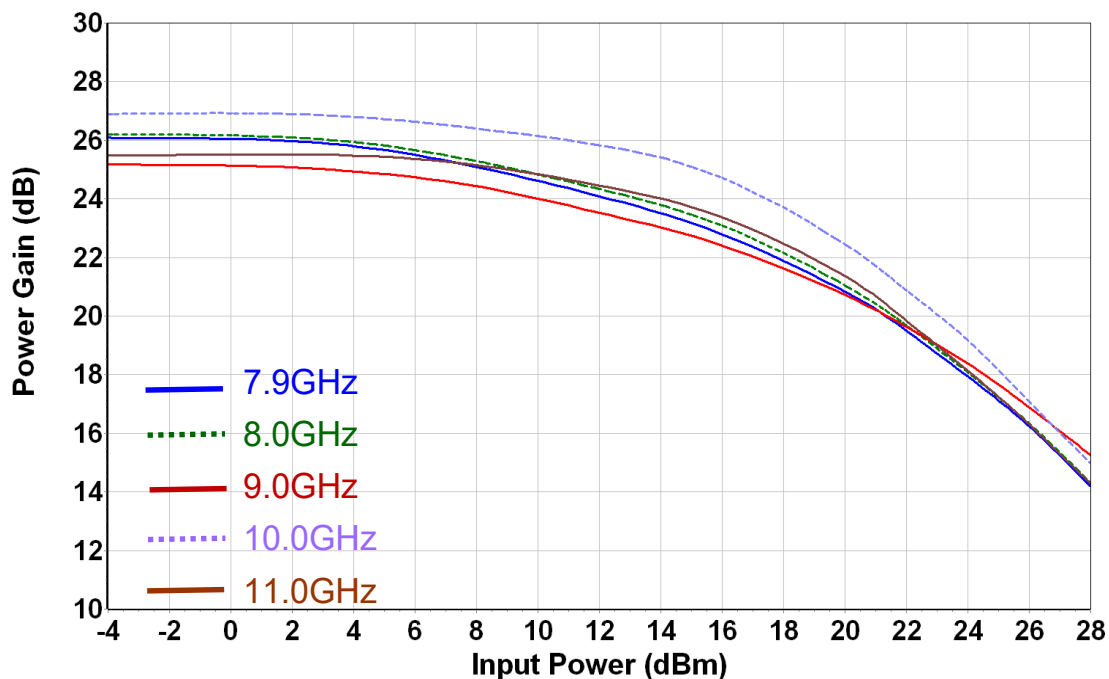
T<sub>case</sub> = +25°C. V<sub>d1</sub> = V<sub>d2</sub> = V<sub>d</sub> = +30V. I<sub>dq</sub> = 680mA.

Pulse width = 25µs. Duty cycle = 10%.

**Drain Current versus Input Power versus Frequency**



**Power Gain versus Input Power versus Frequency**



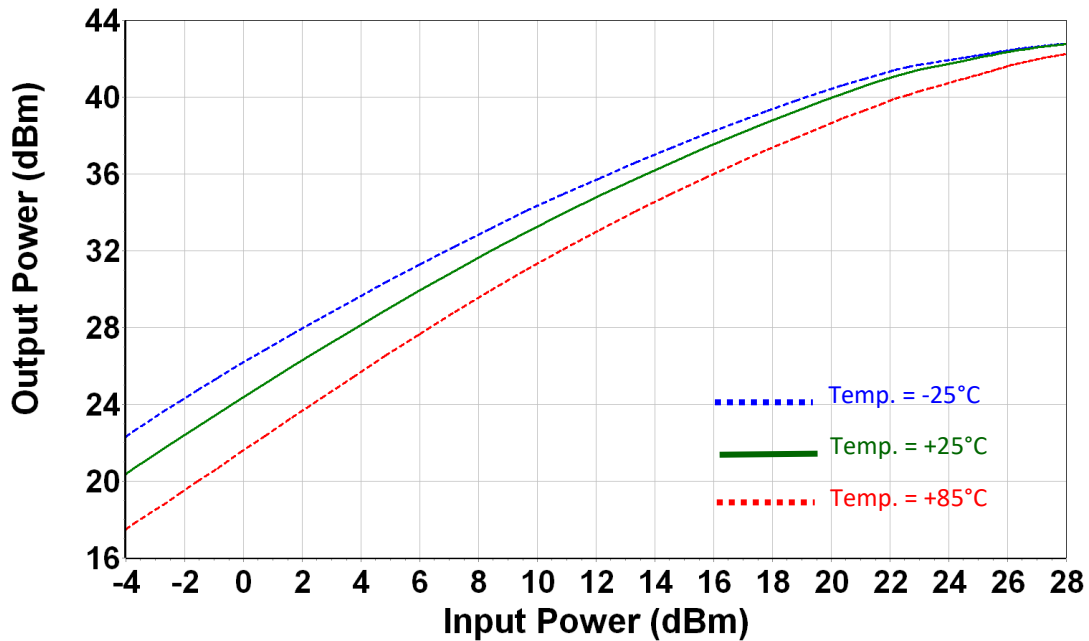
## Typical Board Measurements (CW mode)

Vd1 = Vd2 = Vd = +30V. Idq = 680mA.

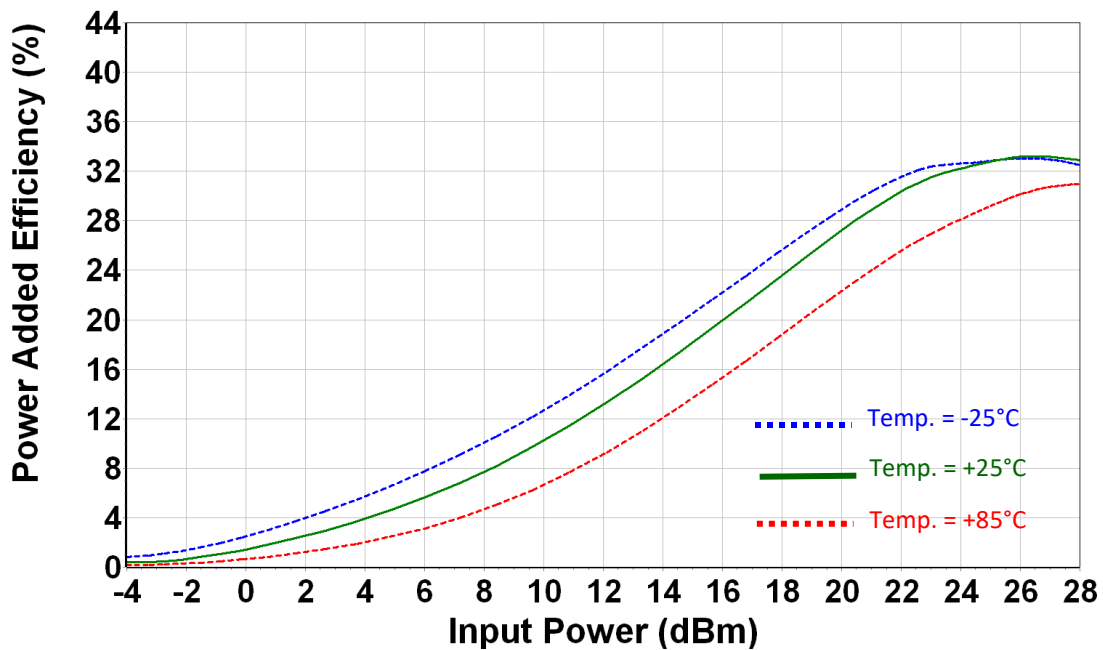
Tcase = -25°C. +25°C. +85°C

Frequency = 9GHz.

Output Power versus Input Power versus Temperature



Power Added Efficiency versus Input Power versus Temperature



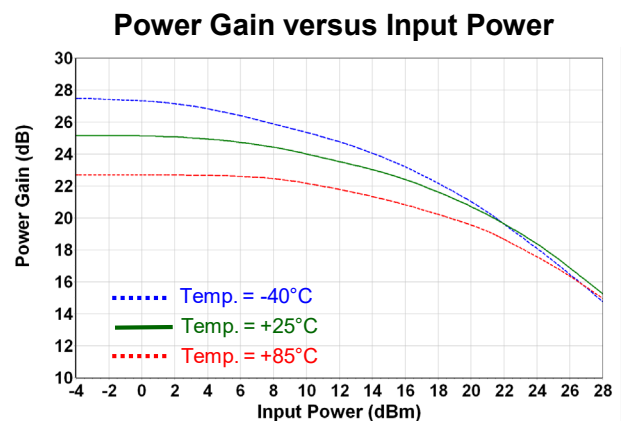
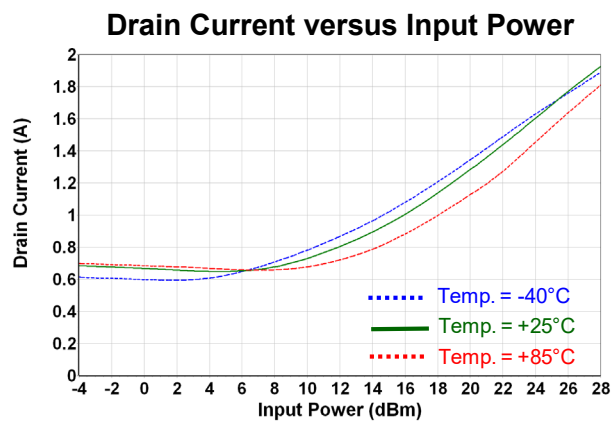
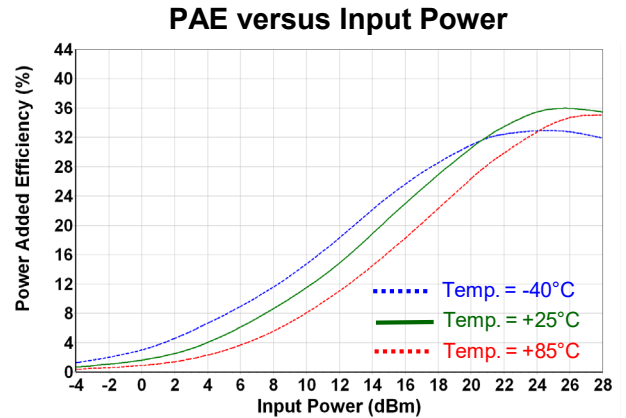
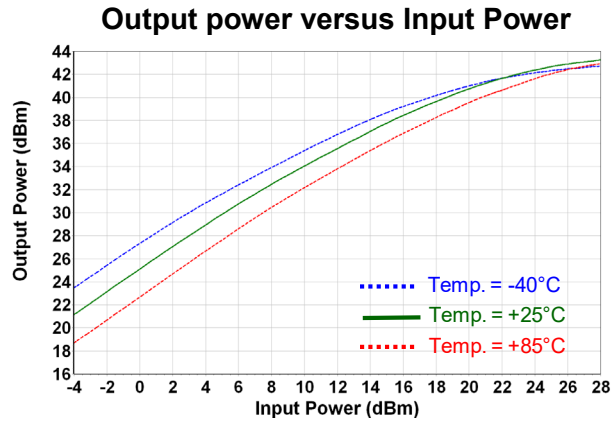


## Typical Board Measurements (Pulsed mode)

Vd1 = Vd2 = Vd = +30V. Idq = 680mA. Pulse width = 25µs. Duty cycle = 10%.

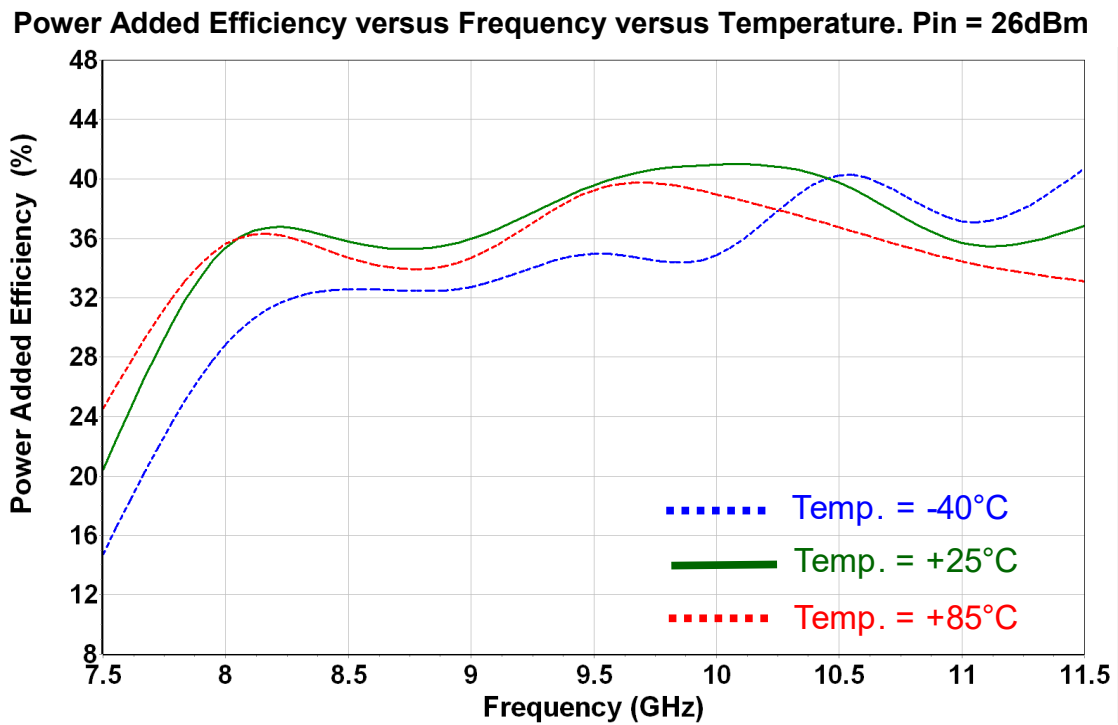
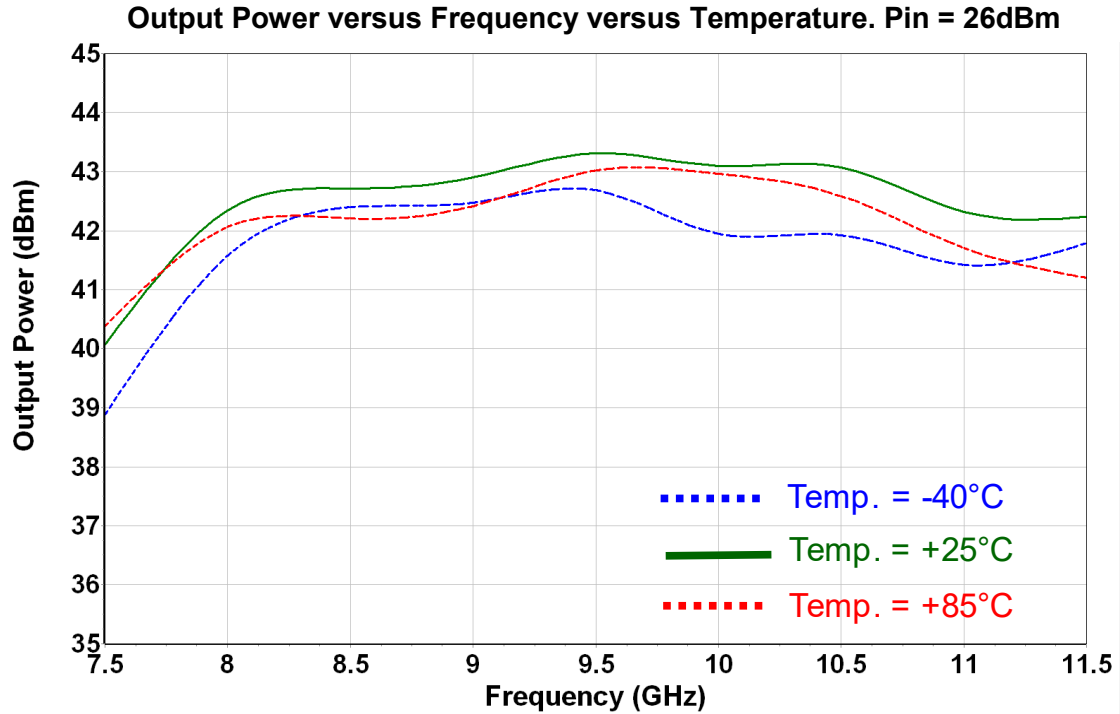
Tcase = -40°C. +25°C. +85°C

Frequency = 9GHz.



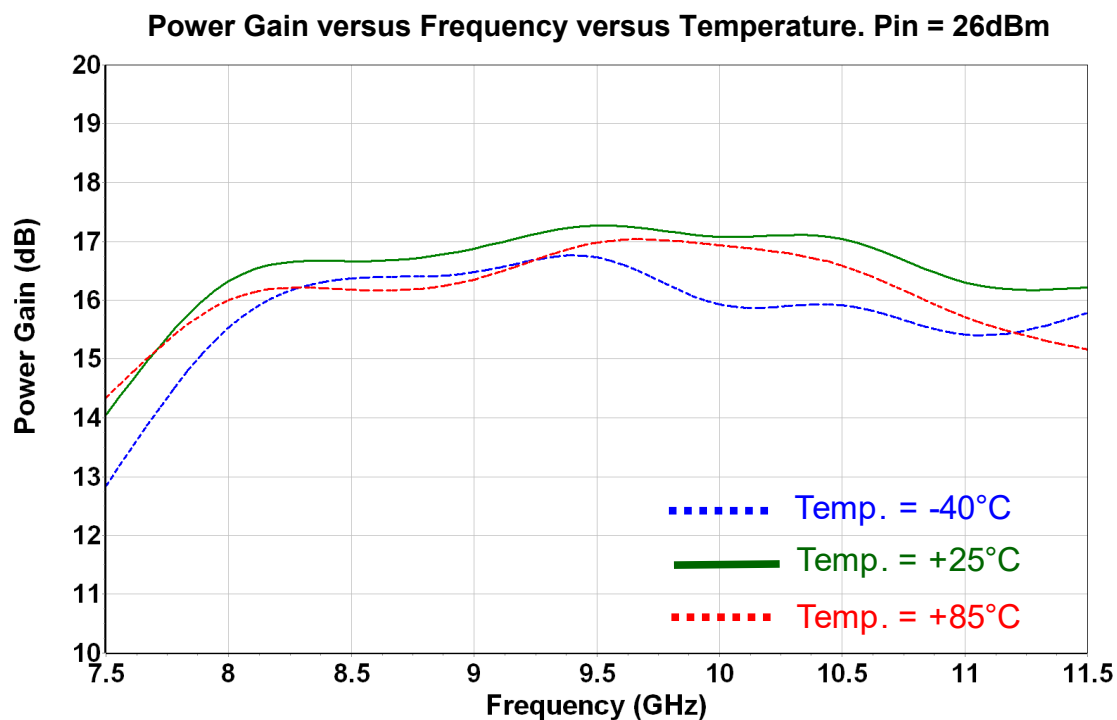
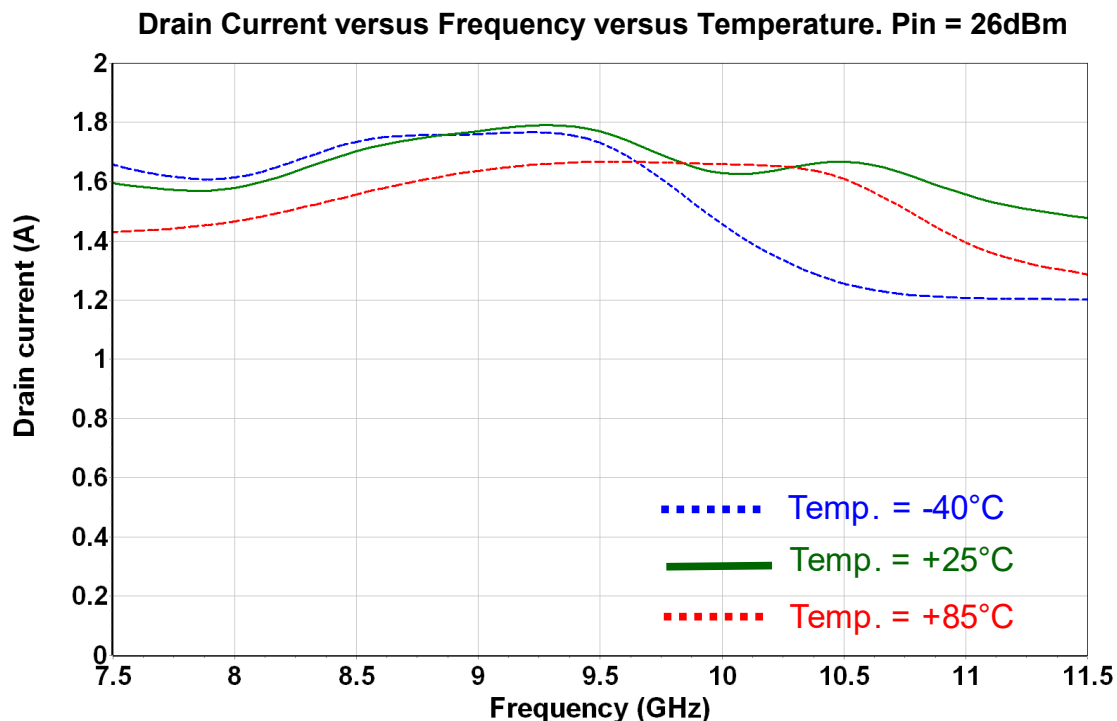
## Typical Board Measurements (Pulsed mode)

Vd1 = Vd2 = Vd = +30V. Idq = 680mA. Pulse width = 25µs. Duty cycle = 10%.  
 Tcase = -40°C. +25°C. +85°C

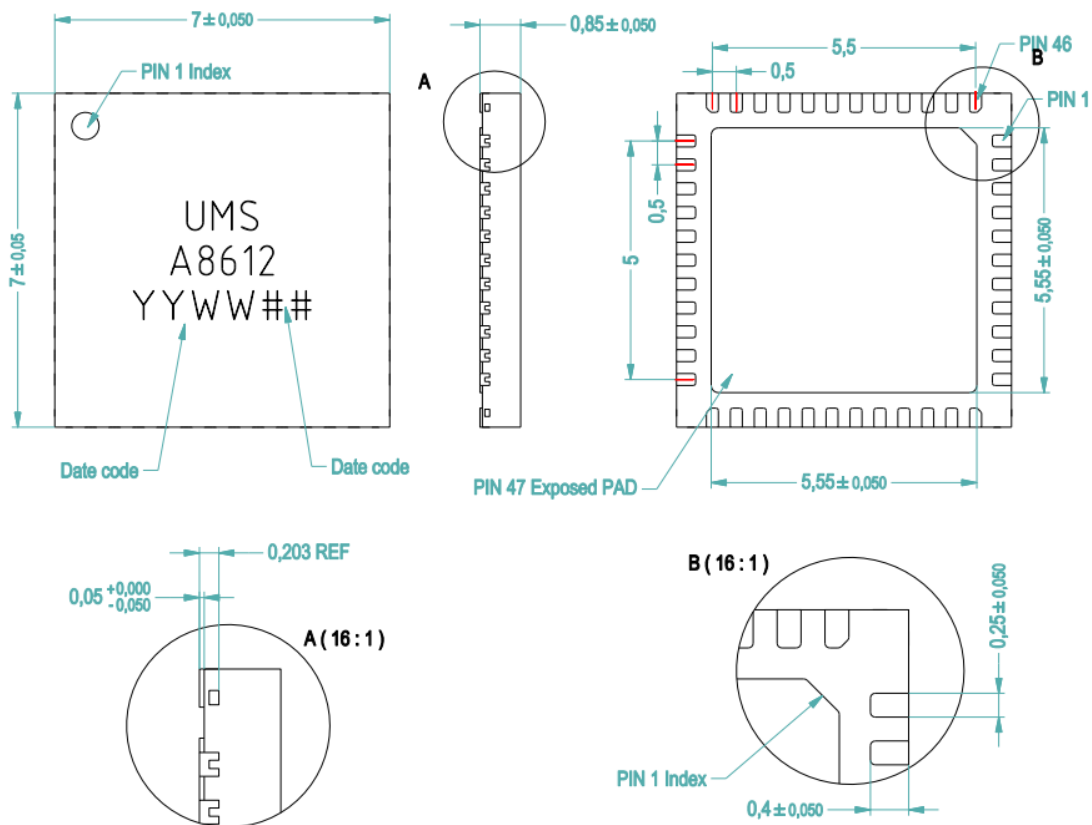


**Typical Board Measurements (Pulsed mode)**

Vd1 = Vd2 = Vd = +30V. Idq = 680mA. Pulse width = 25µs. Duty cycle = 10%.  
 Tcase = -40°C. +25°C. +85°C



## Package outline (1)



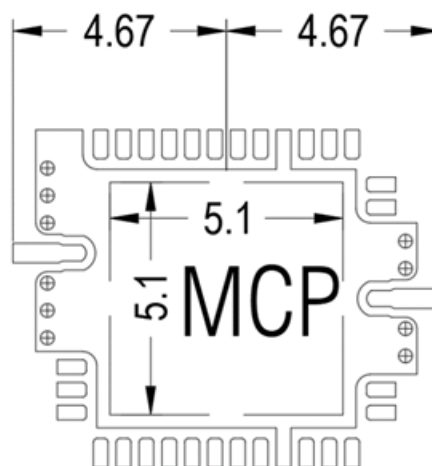
Matte tin. Lead Free (Green)	1- Nc	17- Nc	33- Nc
Units : mm	2- Nc	18- VG2	34- Nc
From the standard : JEDEC MO-220 (VGGD)	3- Gnd <sup>(2)</sup>	19- Nc	35- Nc
	4- RF IN	20- Gnd <sup>(2)</sup>	36- VD2
	6- Nc	22- VD2	38- Gnd <sup>(2)</sup>
	7- Gnd <sup>(2)</sup>	23- Nc	39- Nc
	8- Nc	24- Nc	40- VG2
	9- Gnd <sup>(2)</sup>	25- Nc	41- Nc
	10- Nc	26- Gnd <sup>(2)</sup>	42- Nc
	11- Nc	27- Nc	43- VD1
	12- Nc	28- Gnd <sup>(2)</sup>	44- Nc
	13- VG1	29- RF OUT	45- Nc
	14- Nc	30- Gnd <sup>(2)</sup>	46- Nc
	15- VD1	31- Nc	47- GND
	16- Nc	32- Gnd <sup>(2)</sup>	

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (<https://www.ums-rf.com>) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked "Gnd" through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

## Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at **4.67mm** offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation motherboard".



## ESD sensitivity

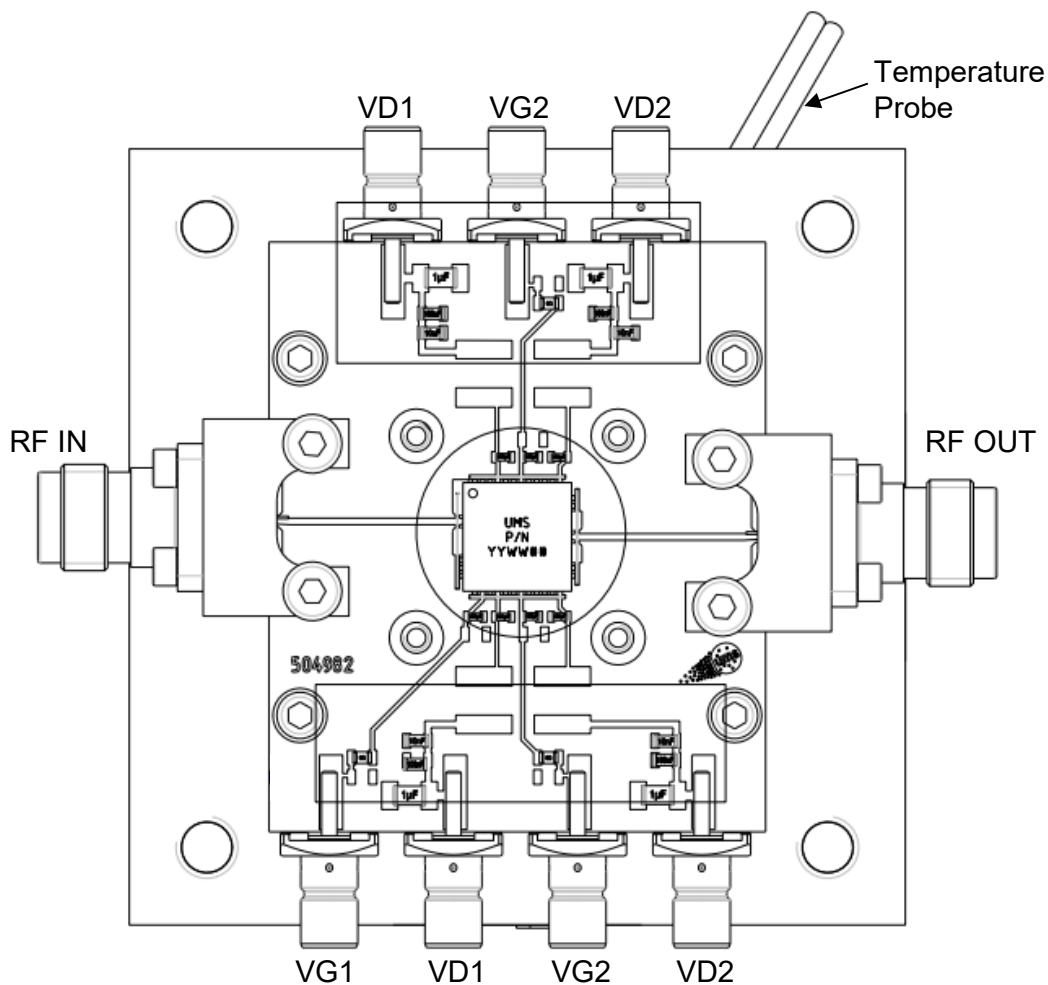
Standard	Value
MIL-STD-1686C	HBM Class 1 (<2000V)

## Package Information

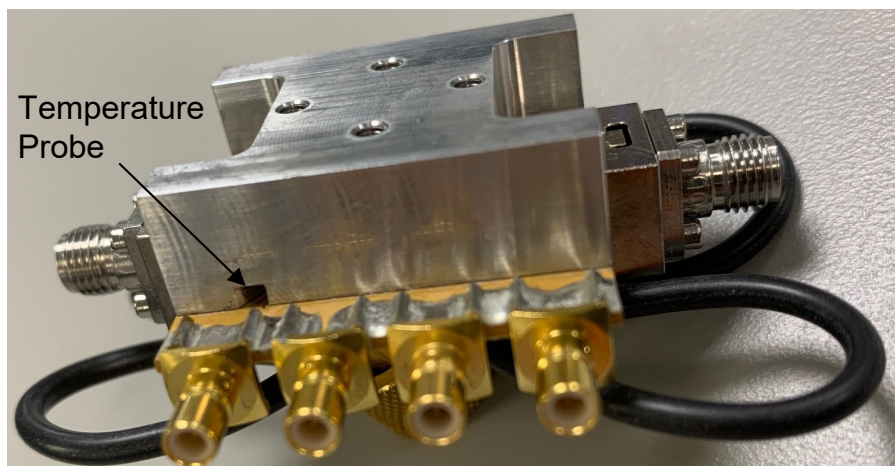
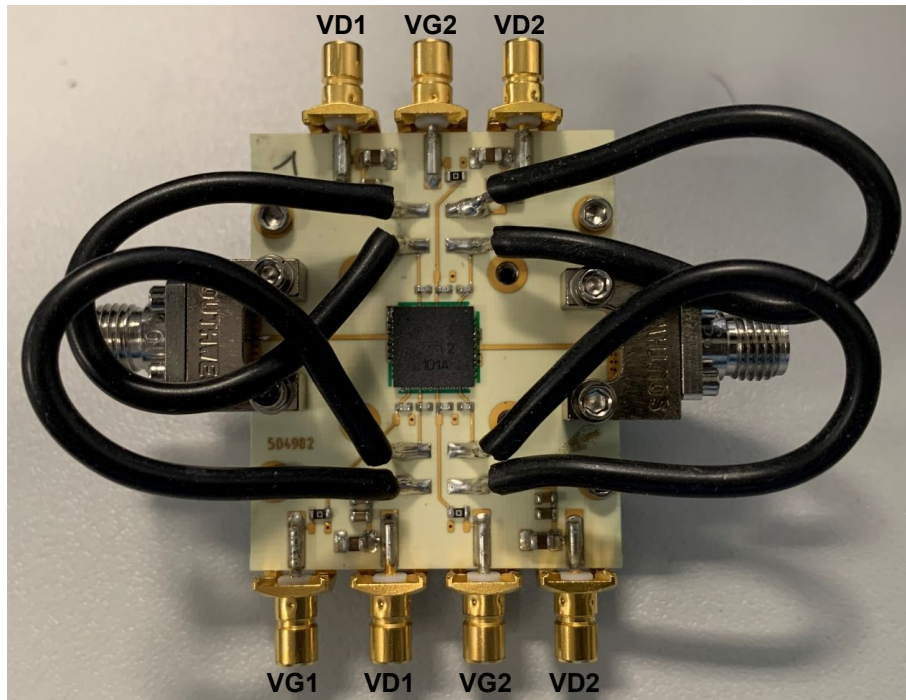
Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% matte tin (Sn)
MSL Rating	MSL3

## Evaluation mother board

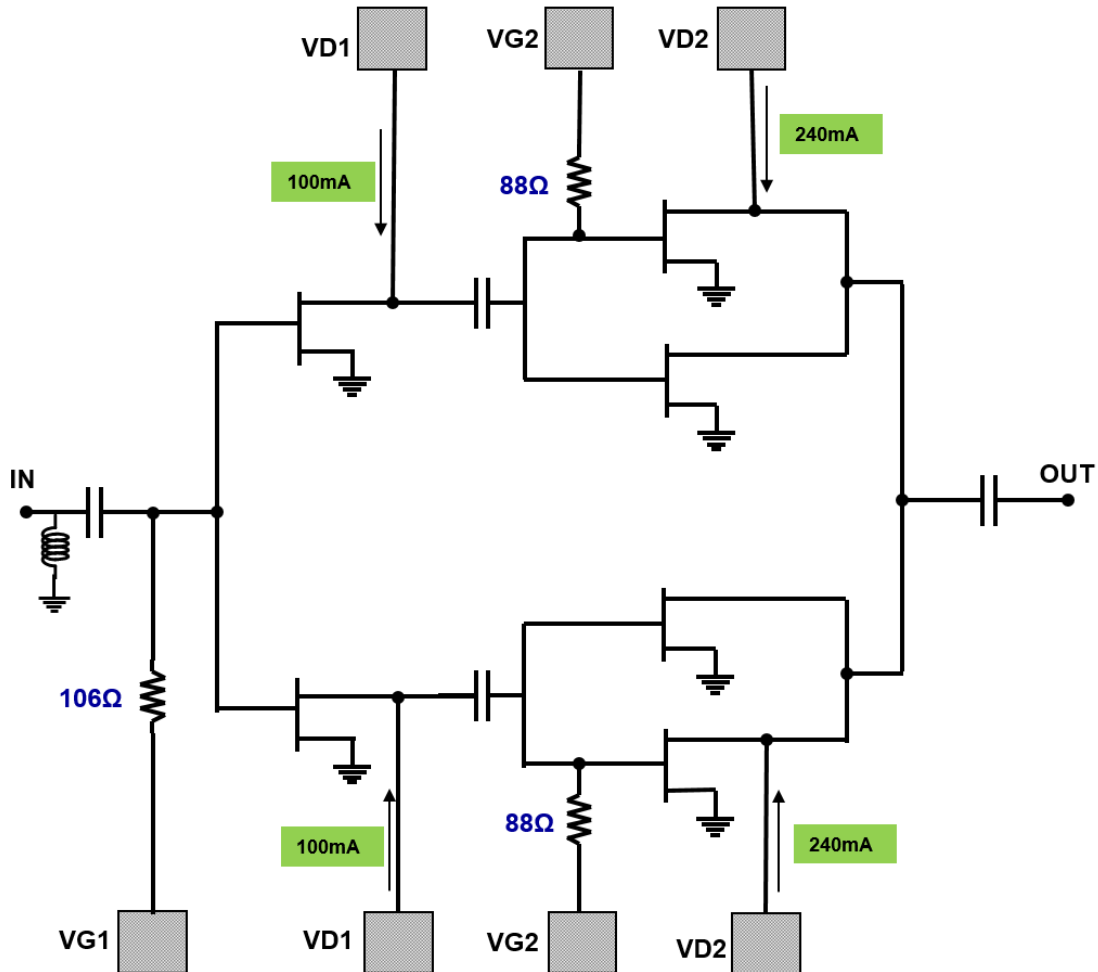
- Compatible with the proposed footprint.
- Based on typically Ro4350 / 10mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of  $100\text{pF} \pm 5\%$  and  $10\text{nF} \pm 10\%$  are recommended for all DC accesses.
- See application note AN0017 for details.



Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.



## DC Schematic



## Notes

Due to ESD protection circuits on RF input, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF input access.

The DC connections do not include any decoupling capacitor in package. Therefore it is mandatory to provide a good external DC decoupling on the PC board as close as possible to the package.





## Recommended package footprint

Refer to the application note AN0017 available at <https://www.ums-rf.com> for package footprint recommendations and exact package dimensions.

## SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017 available at <https://www.ums-rf.com>.

## Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <https://www.ums-rf.com>.

## Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations for the UMS package products.

## Sampling request reference

QFN 7x7 package:

CHA8612-QDB/XY

Stick: XY = 20

Tape & reel: XY = 21

Contact us

Web site: <https://www.ums-rf.com>

e.mail: [mktsales@ums-rf.com](mailto:mktsales@ums-rf.com)

Phone: 33 (1) 69 86 32 00 (France)

1 (781) 791-5078 (USA)

65 9298 8316 (Singapour)

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