

5W X Band Medium Power Amplifier

GaN Monolithic Microwave IC

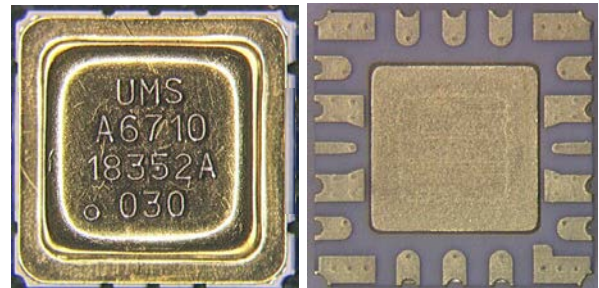
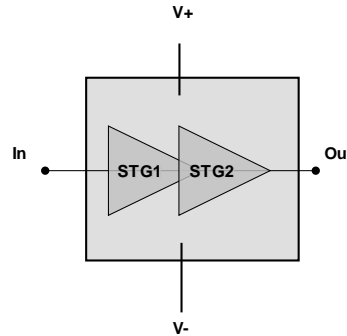
Description

The CHA6710-FAB is a two stage Medium Power Amplifier operating between 8 and 12.75GHz. It typically provides 5W of saturated output power and 35% of Power Added Efficiency.

It is designed for a wide range of applications, from defence to space communication systems.

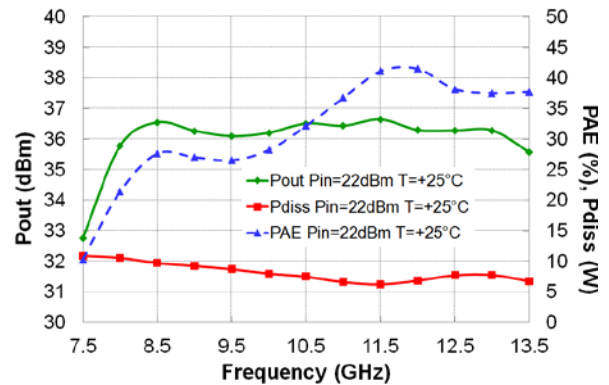
The circuit is manufactured with a GaN pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is proposed in a RoHS leadless surface mount hermetic metal ceramic 6x6mm² package, compliant SMD assembly tools.



Main Features

- Frequency range: 8-12.75GHz
- High output power: 4.5W
- High PAE: 35%
- Linear Gain: 22.5dB
- DC bias: Vd=25Volt @ Idq=0.2A
- 6x6mm² hermetic metal ceramic package



Main Electrical Characteristics

Tamb.= +25°C, Vd = +25V, Idq = 200mA, Pulse width=25µs, Duty cycle =10%

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	8		12.75	GHz
Gain	Linear Gain		22.5		dB
Pout	Output Power		4.5		W
PAE	Associated Power Added Efficiency		35		%

Electrical Characteristics (Pulsed mode)

Tamb.= +25°C, Vd = +25V, Idq = 200mA, Pulse width=25µs, Duty cycle =10%

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	8		12.75	GHz
Gain	Linear Gain		22.5		dB
Pout	Output Power (Pin=23dBm)		4.5		W
PAE	Associated Power Added Efficiency (Pin=22dBm)		35		%
Id	Associated current (Pin=23dBm)		0.49		A
IRL	Input Return Loss		10		dB
ORL	Output Return Loss		10		dB
Idq	Quiescent Current		0.2		A
Vd	Drain Voltage		25		V
Vg	Gate Voltage		-3.2		V

These values are representative of measurements done in test fixture with a bonding wire of typically 0.25 to 0.3nH.

Electrical Characteristics (CW mode)

Tamb.= +25°C, Vd = +25V, Idq = 200mA

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	8		12.75	GHz
Gain	Linear Gain		22		dB
Pout	Output Power (Pin=23dBm)		4.3		W
PAE	Associated Power Added Efficiency (Pin=22dBm)		34		%
Id	Associated current (Pin=23dBm)		0.49		A
IRL	Input Return Loss		10		dB
ORL	Output Return Loss		10		dB
Idq	Quiescent Current		0.2		A
Vd	Drain Voltage		25		V
Vg	Gate Voltage		-3.25		V

These values are representative of measurements done in test fixture with a bonding wire of typically 0.25 to 0.3nH.

Electrical Characteristics (Pulsed mode)

Tamb.= +25°C, Vd = +30V, Idq = 200mA, Pulse width=25µs, Duty cycle =10%

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	8		12.75	GHz
Gain	Linear Gain		23.5		dB
Pout	Output Power (Pin=23dBm)		5		W
PAE	Associated Power Added Efficiency (Pin=23dBm)		33		%
Id	Associated current (Pin=23dBm)		0.53		A
IRL	Input Return Loss		10		dB
ORL	Output Return Loss		10		dB
Idq	Quiescent Current		0.2		A
Vd	Drain Voltage		30		V
Vg	Gate Voltage		-3.2		V

These values are representative of measurements done in test fixture with a bonding wire of typically 0.25 to 0.3nH.

Electrical Characteristics (CW mode)

Tamb.= +25°C, Vd = +30V, Idq = 200mA

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	8		12.75	GHz
Gain	Linear Gain		23		dB
Pout	Output Power (Pin=23dBm)		5		W
PAE	Associated Power Added Efficiency (Pin=23dBm)		33		%
Id	Associated current (Pin=23dBm)		0.52		A
IRL	Input Return Loss		10		dB
ORL	Output Return Loss		10		dB
Idq	Quiescent Current		0.2		A
Vd	Drain Voltage		30		V
Vg	Gate Voltage		-3.25		V

These values are representative of measurements done in test fixture with a bonding wire of typically 0.25 to 0.3nH.

Absolute Maximum Ratings ⁽¹⁾

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	55V	V
Pin	Maximum peak input power overdrive	30	dBm
Pdiss	Maximum dissipated power	22	W
Tj	Junction temperature	230	°C
Tstg	Storage temperature range	-55 to +150	°C

⁽¹⁾ Operation of this device above any one of these parameters may cause permanent damage.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad N°	Parameter	Typical Values	Unit
Vd	Vd1, Vd2	Drain voltage	25 / 30	V
Vg	Vg1, Vg2	Gate voltage		
		HPA on (pulsed mode)	-3.2	V
		HPA on (CW mode)	-3.25	V
		HPA off	-8 to -5	V

Biassing up Procedure

1. Bias HPA gate voltage at Vg close to Vpinch-off (Typically: Vg ≈ -5V)
2. Apply Vds bias voltage (Typically: Vd = 25V)
3. Increase Vgs up to quiescent bias drain current Idq (pulsed applied on the gate)
4. Apply RF signal

Biassing down Procedure

1. Turn off RF signal
2. Bias HPA gate voltage at Vg close to Vpinch-off (Typically: Vg ≈ -5V)
3. Turn Vds bias voltage to 0V
4. Turn Vgs bias voltage to 0V

Typical FAB Sij parameters (Pulsed mode)

Tback side.= +25°C, Vd = +25V, Idq = 200mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
1	-0.24	-55.91	-51.10	175.72	-28.62	-115.54	-1.08	-62.61
1.50	-0.50	-85.78	-65.61	43.68	-42.67	-50.94	-0.61	-99.09
2.00	-1.25	-117.12	-46.77	-143.57	-46.49	43.31	-0.78	-132.58
2.50	-2.56	-152.25	-78.40	148.85	-39.26	-121.21	-1.20	-165.85
3.00	-5.33	171.98	-56.43	-32.21	-17.29	171.91	-1.81	161.66
3.5	-9.49	137.13	-52.84	158.34	-11.52	71.25	-2.70	129.06
4	-16.40	98.24	-54.98	-138.52	-10.11	21.65	-3.85	96.06
4.5	-28.15	14.63	-57.36	-168.81	-9.16	-12.75	-5.43	62.87
5	-22.24	-91.28	-51.20	58.81	-8.10	-27.52	-7.18	30.76
5.5	-19.49	-117.83	-48.80	111.72	-3.48	-34.47	-8.64	1.49
6	-20.91	-114.54	-52.40	95.90	3.78	-57.88	-8.93	-25.71
6.5	-13.30	-119.66	-49.19	106.58	10.76	-102.19	-8.80	-60.55
7	-9.50	-149.07	-55.71	-92.56	16.12	-157.22	-8.03	-105.67
7.5	-9.36	178.83	-46.99	-20.07	20.12	139.79	-8.44	-157.69
8	-9.93	158.56	-48.77	-72.82	21.66	72.81	-10.98	160.41
8.5	-9.93	142.46	-46.81	-30.76	21.37	15.78	-13.68	143.00
9	-9.95	121.37	-51.02	-143.52	21.08	-31.16	-13.09	123.10
9.5	-10.43	96.72	-48.64	-88.22	21.45	-74.83	-12.49	95.23
10	-11.98	66.70	-65.90	119.84	22.43	-120.29	-12.30	60.64
10.5	-15.64	24.58	-49.17	30.63	23.59	-171.46	-12.12	18.37
11	-25.62	-80.46	-58.31	-167.21	24.24	130.61	-13.01	-36.11
11.5	-17.01	167.15	-47.96	-76.00	23.69	70.75	-13.92	-91.42
12	-13.01	130.99	-47.28	-36.46	22.60	13.22	-13.18	-136.08
12.5	-10.50	107.31	-41.36	-124.75	21.58	-46.85	-11.33	-170.76
13	-7.10	84.06	-47.53	-128.99	19.64	-116.85	-7.93	151.98
13.5	-4.98	52.20	-44.14	-159.10	14.73	171.24	-6.10	112.87
14	-4.16	21.78	-49.74	30.00	8.08	114.52	-5.30	79.70
14.5	-3.85	-3.13	-48.80	-166.79	1.42	69.01	-4.77	53.38
15	-3.56	-24.58	-46.81	-41.71	-5.11	30.11	-3.97	28.98
15.5	-3.19	-44.27	-51.71	-22.98	-11.43	-4.41	-3.17	5.49
16	-2.87	-62.91	-46.22	9.78	-17.90	-35.33	-2.65	-16.38
16.5	-2.54	-80.24	-54.16	46.75	-23.96	-65.82	-2.14	-36.52
17	-2.35	-96.21	-51.63	29.94	-30.16	-97.16	-1.72	-55.12
17.5	-2.14	-110.93	-46.79	76.33	-38.91	-117.18	-1.42	-73.58
18	-1.94	-125.42	-41.09	87.76	-39.16	-115.64	-1.24	-90.39
18.5	-1.79	-138.77	-42.09	31.39	-51.27	-78.39	-1.03	-105.93
19	-1.65	-151.96	-44.34	8.57	-45.73	-5.09	-0.91	-120.73
19.5	-1.52	-163.87	-41.87	-2.86	-57.05	-58.99	-0.89	-134.44
20	-1.40	-176.01	-42.21	-53.02	-49.33	-116.03	-0.68	-146.35

Device thermal information

The device thermal performances below are based on UMS rules to evaluate the junction temperature.

This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHA6710-FAB is manufactured (GaN Power HEMT 0.25µm).

The temperature T_{case} is defined as the case back side. The thermal resistance (R_{th_eq}) is given for the full circuit, and assumes CW and pulsed operation mode are given in the table.

Thermal Resistance ⁽¹⁾	R_{th_eq}	$T_{b_chip} = 25^{\circ}C, V_d = 25V,$ $I_{d_drive} = 0.49A$	7.6	$^{\circ}C/W$
Junction Temperature	T_j	$P_{in} = 22dBm$ $P_{out} = 36.3dBm$ $P_{diss} = 8W$ CW	86	$^{\circ}C$
Median Life	T50		2.31×10^{11}	Hrs

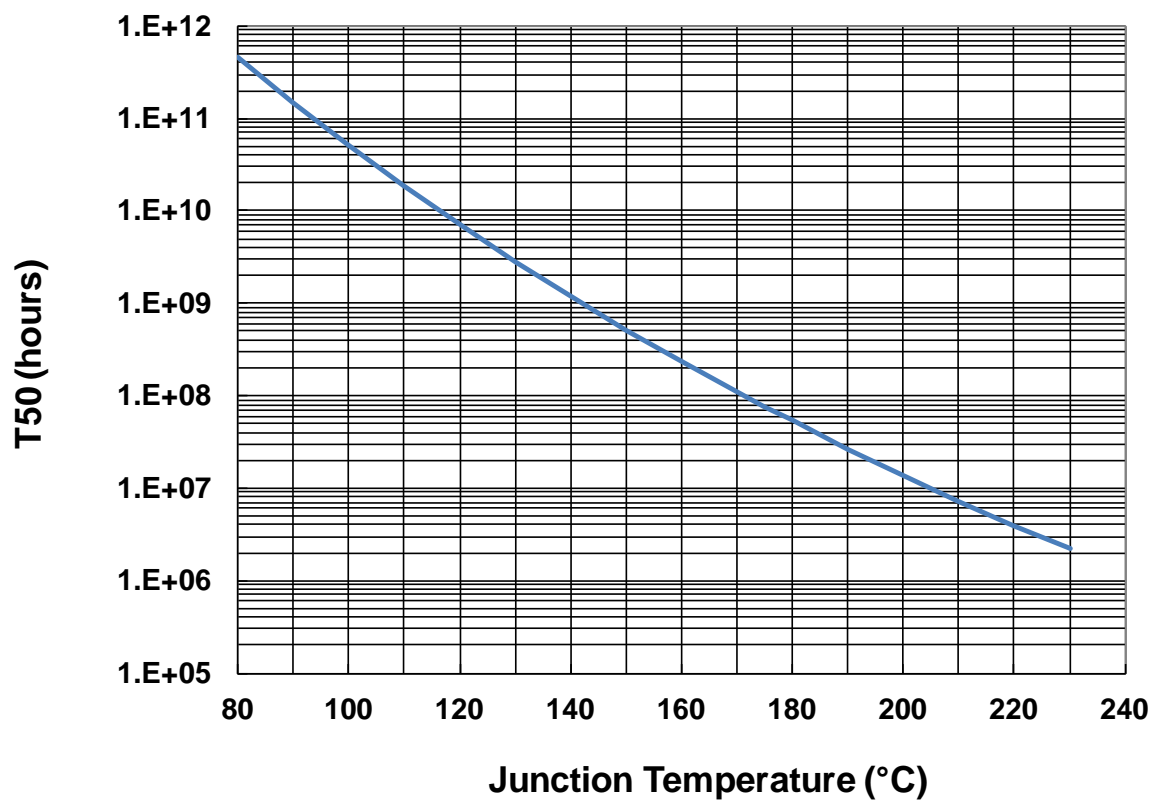
Thermal Resistance ⁽¹⁾	R_{th_eq}	$T_{b_chip} = 85^{\circ}C, V_d = 25V,$ $I_{d_drive} = 0.490A$	10.8	$^{\circ}C/W$
Junction Temperature	T_j	$P_{in} = 23dBm$ $P_{out} = 36dBm$ $P_{diss} = 8.35W$ CW	175	$^{\circ}C$
Median Life	T50		7.63×10^7	Hrs

Thermal Resistance ⁽¹⁾	R_{th_eq}	$T_{b_chip} = 25^{\circ}C, V_d = 30V,$ $I_{d_drive} = 0.518A$	8.33	$^{\circ}C/W$
Junction Temperature	T_j	$P_{in} = 22dBm$ $P_{out} = 37.1dBm$ $P_{diss} = 10.56W$ CW	92	$^{\circ}C$
Median Life	T50		2.19×10^{11}	Hrs

Thermal Resistance ⁽¹⁾	R_{th_eq}	$T_{b_chip} = 85^{\circ}C, V_d = 30V,$ $I_{d_drive} = 0.520A$	10.38	$^{\circ}C/W$
Junction Temperature	T_j	$P_{in} = 23dBm$ $P_{out} = 36.9dBm$ $P_{diss} = 10.87W$ CW	198	$^{\circ}C$
Median Life	T50		1.57×10^7	Hrs

⁽¹⁾ Thermal resistance measured to back of the package.

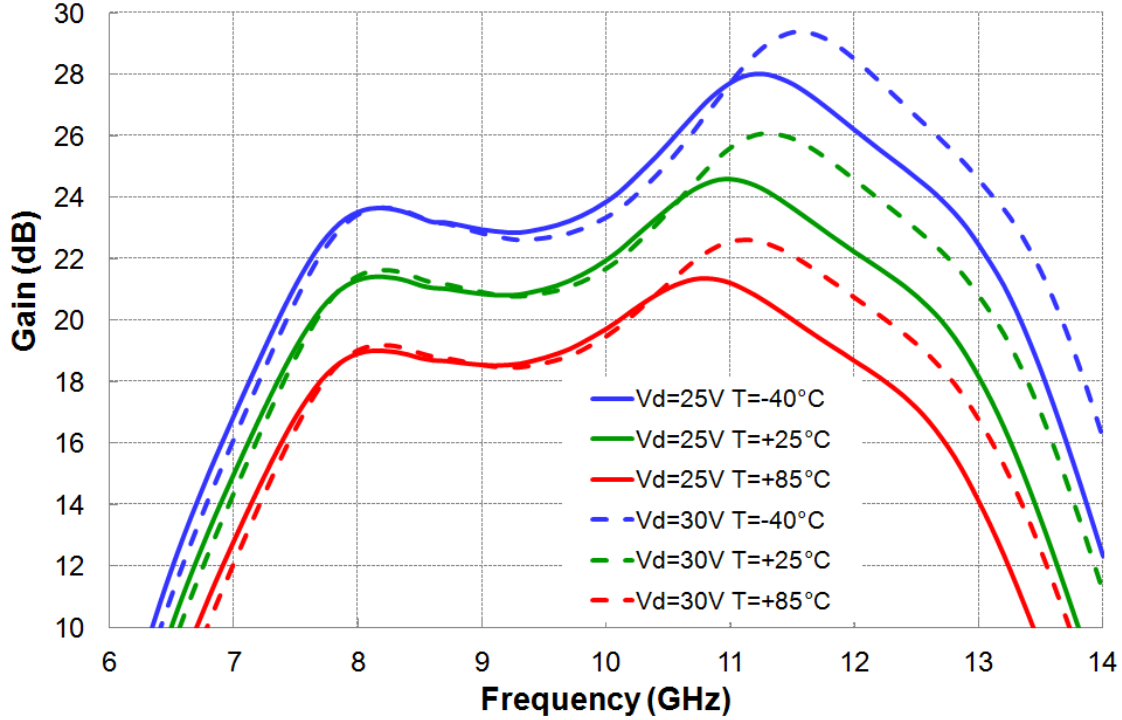
Median Life Time versus Junction Temperature



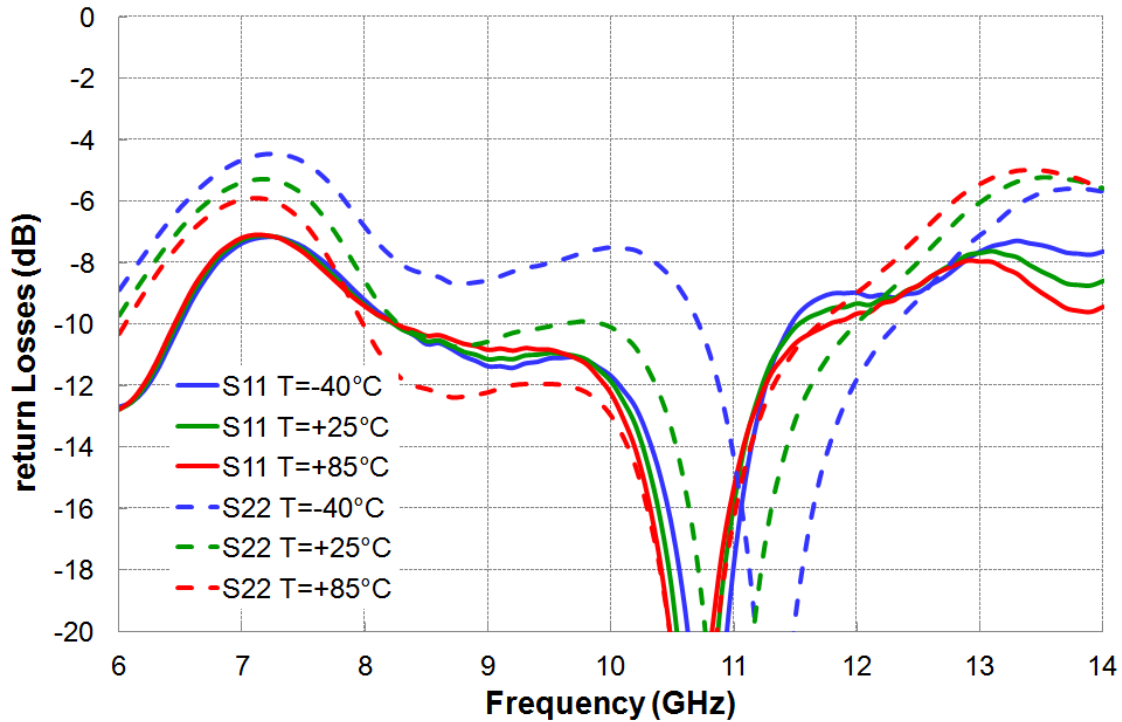
Typical Board Measurements (CW mode)

Vd = +25 & 30V, Idq = 200mA @ Tback side = +25°C

Linear Gain versus Frequency (Temp.= -40 & +25 & +85 °C)



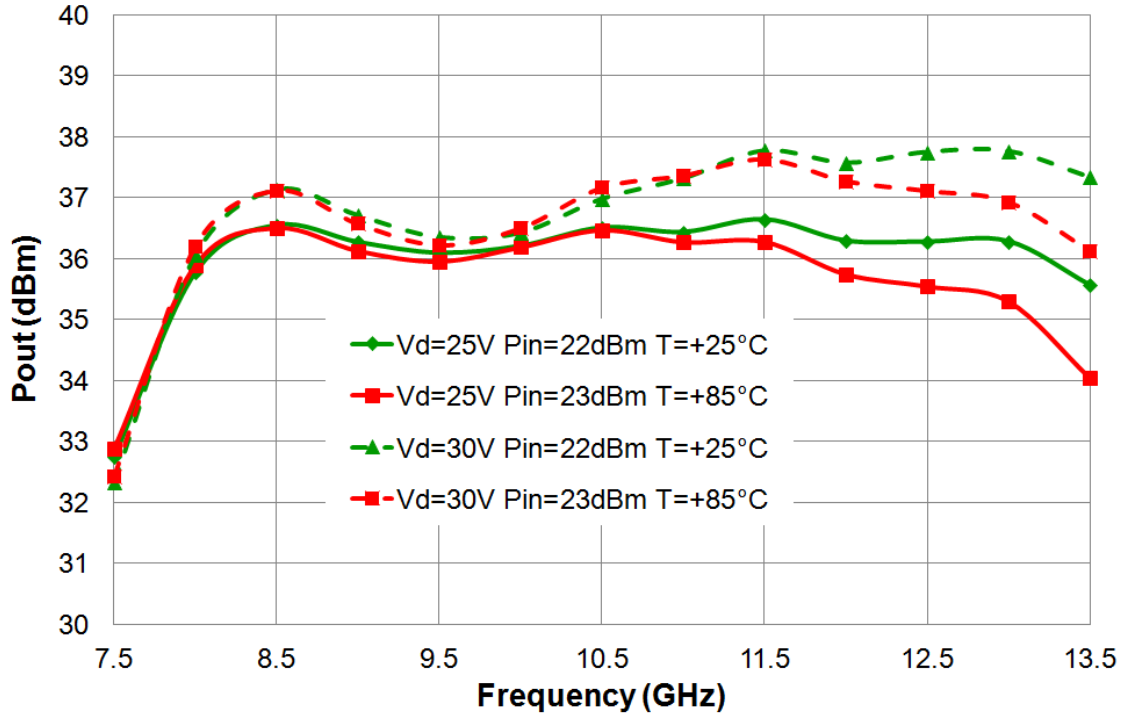
Return Losses versus Frequency (Temp.= -40 & +25 & +85 °C) Vd=25V



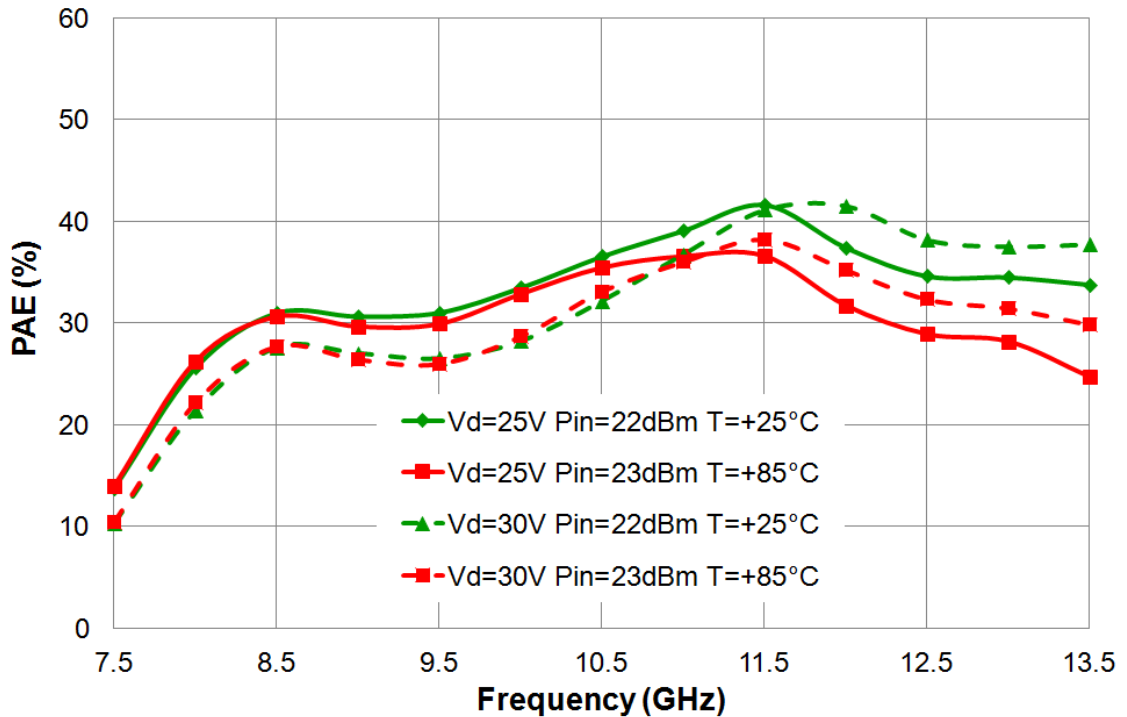
Typical Board Measurements (CW mode)

Vd = +25 & 30V, Idq = 200mA @ Tback side = +25°C

Output Power versus Frequency (Temp. = +25 & +85 °C)



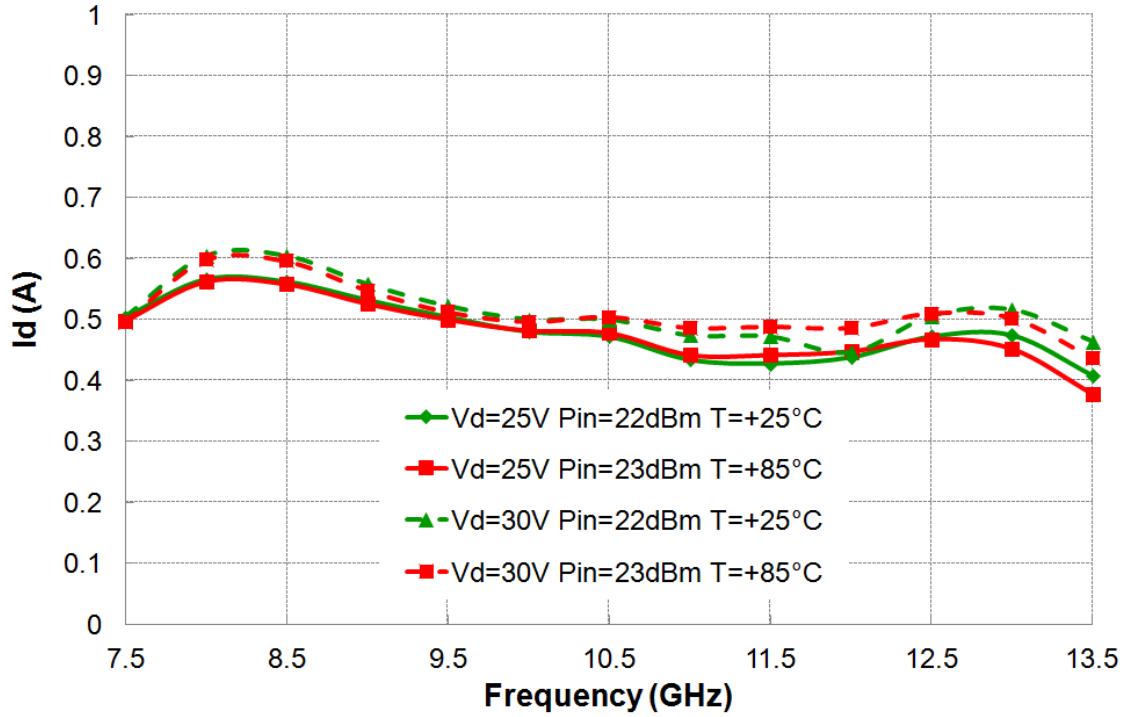
Power Added Efficiency versus Frequency (Temp +25 & +85 °C)



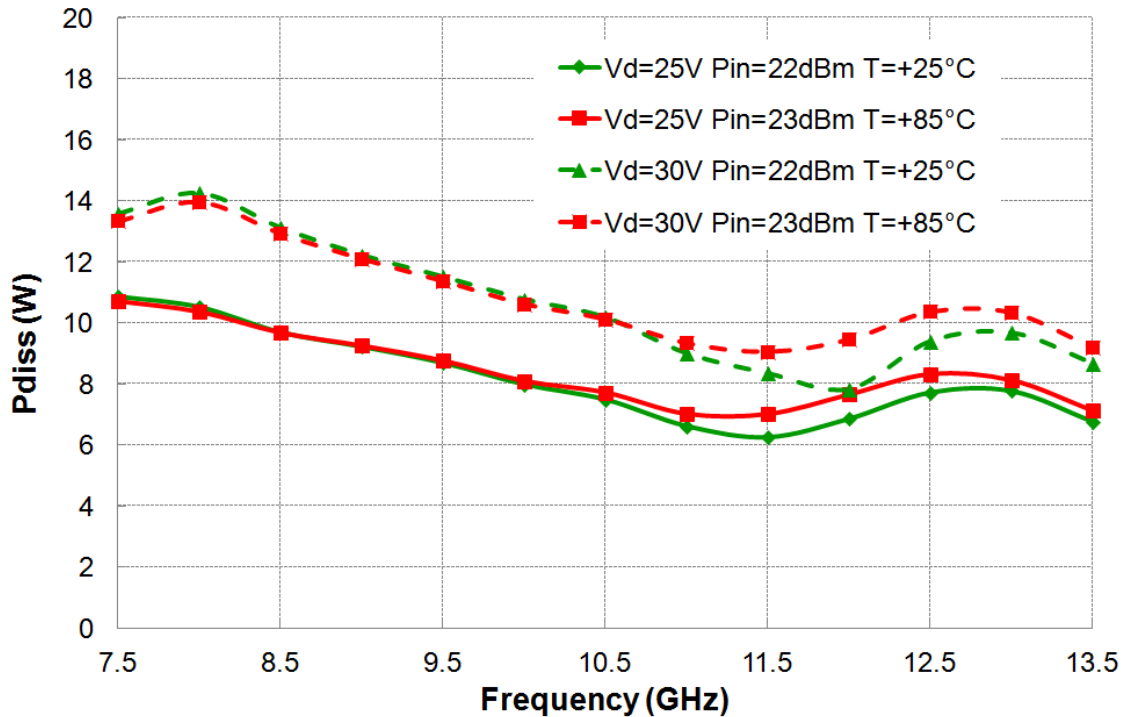
Typical Board Measurements (CW mode)

Vd = +25 & 30V, Idq = 200mA @ Tback side = +25°C

Drain Current versus Frequency (Temp.= +25 & +85 °C)

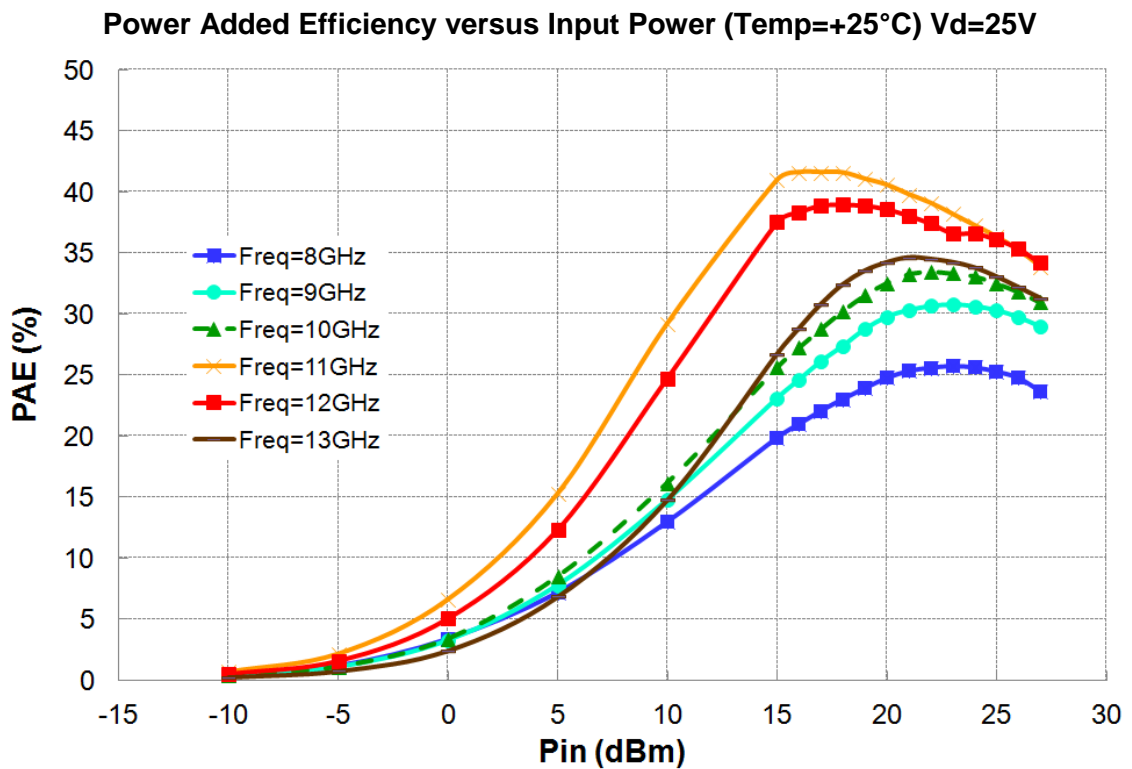
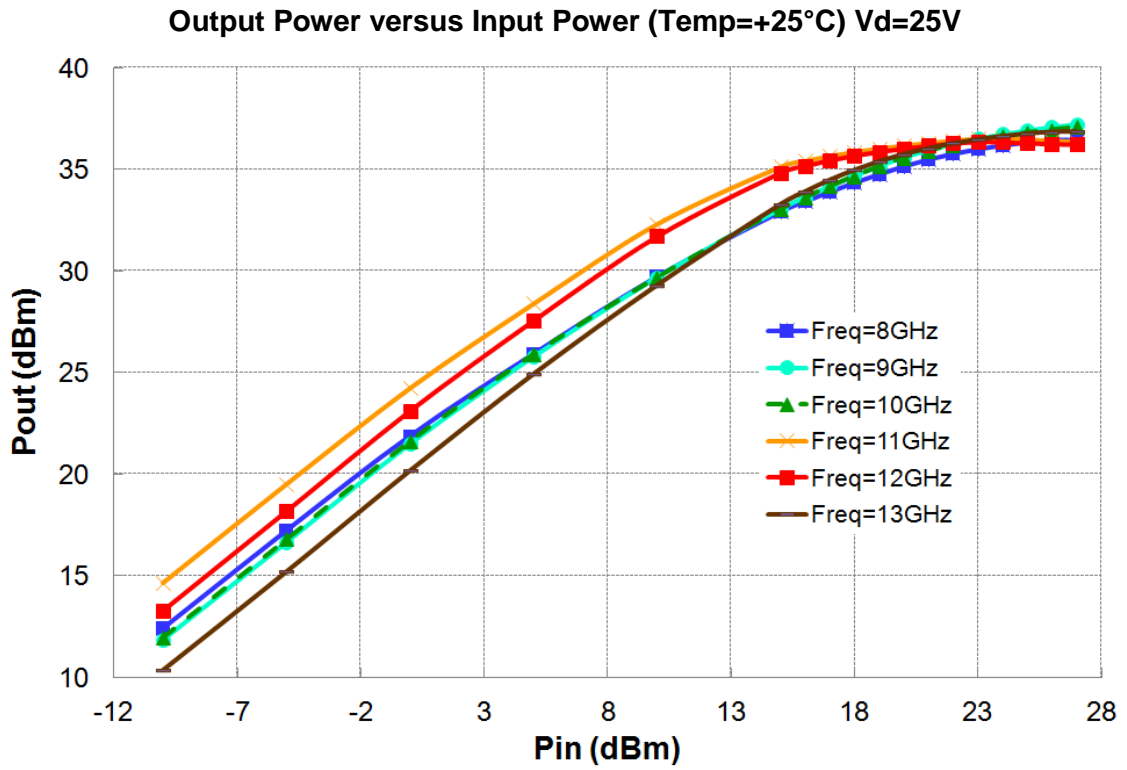


Dissipated Power versus Frequency (Temp.= +25 & +85 °C)



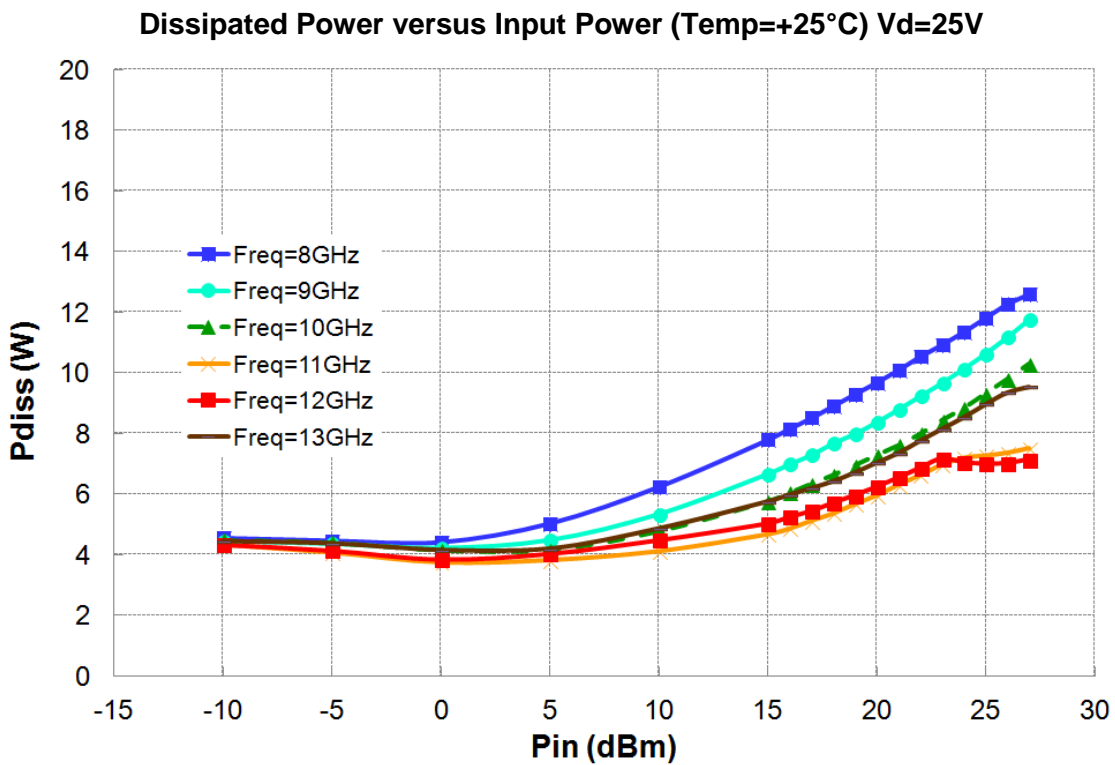
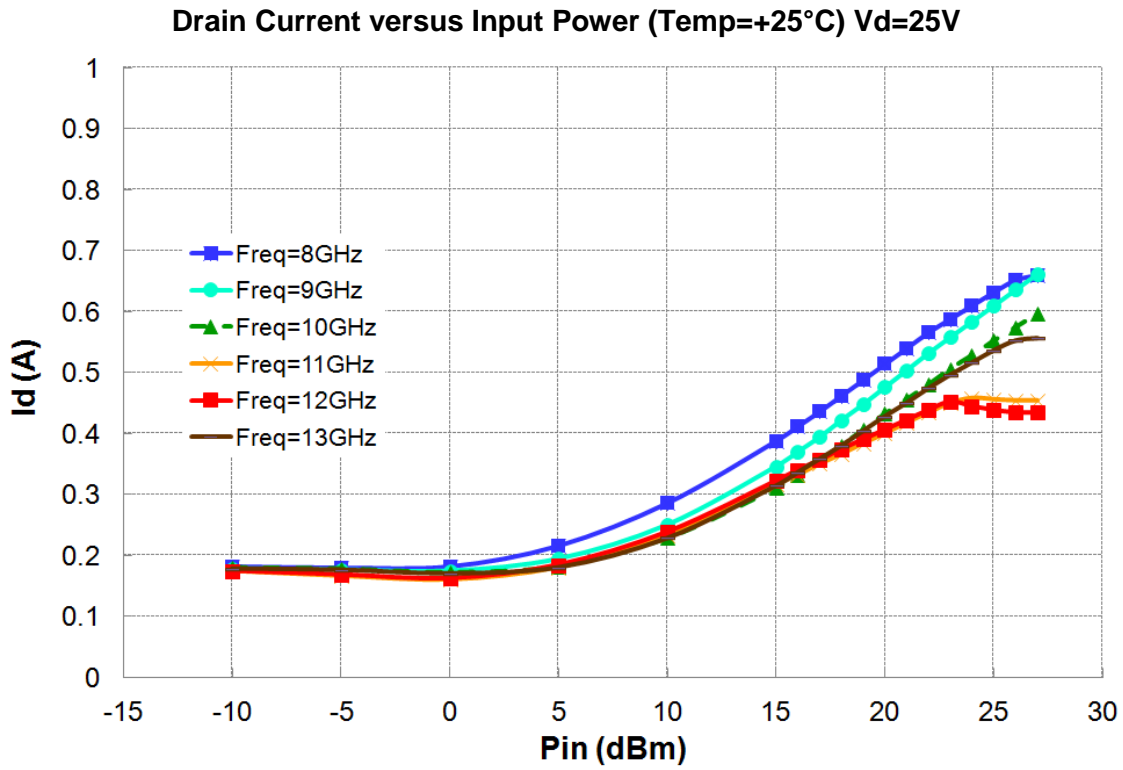
Typical Board Measurements (CW mode)

Tback side = +25°C, Vd = +25V, Idq = 200mA



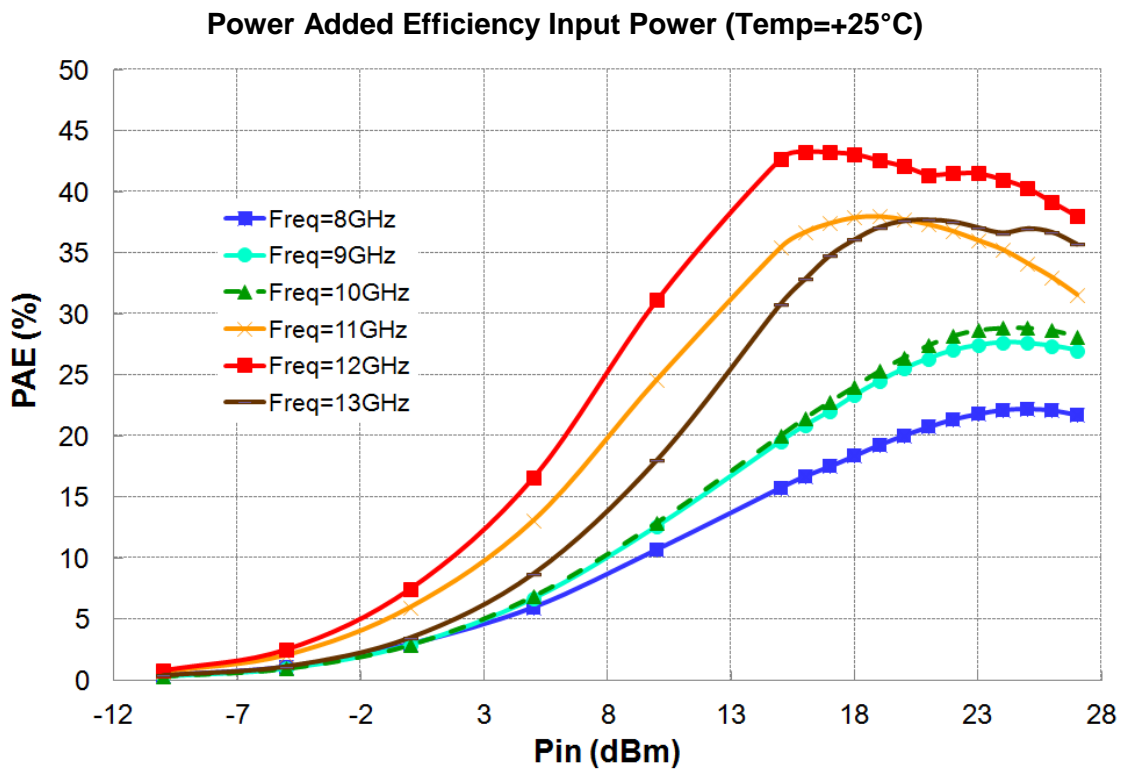
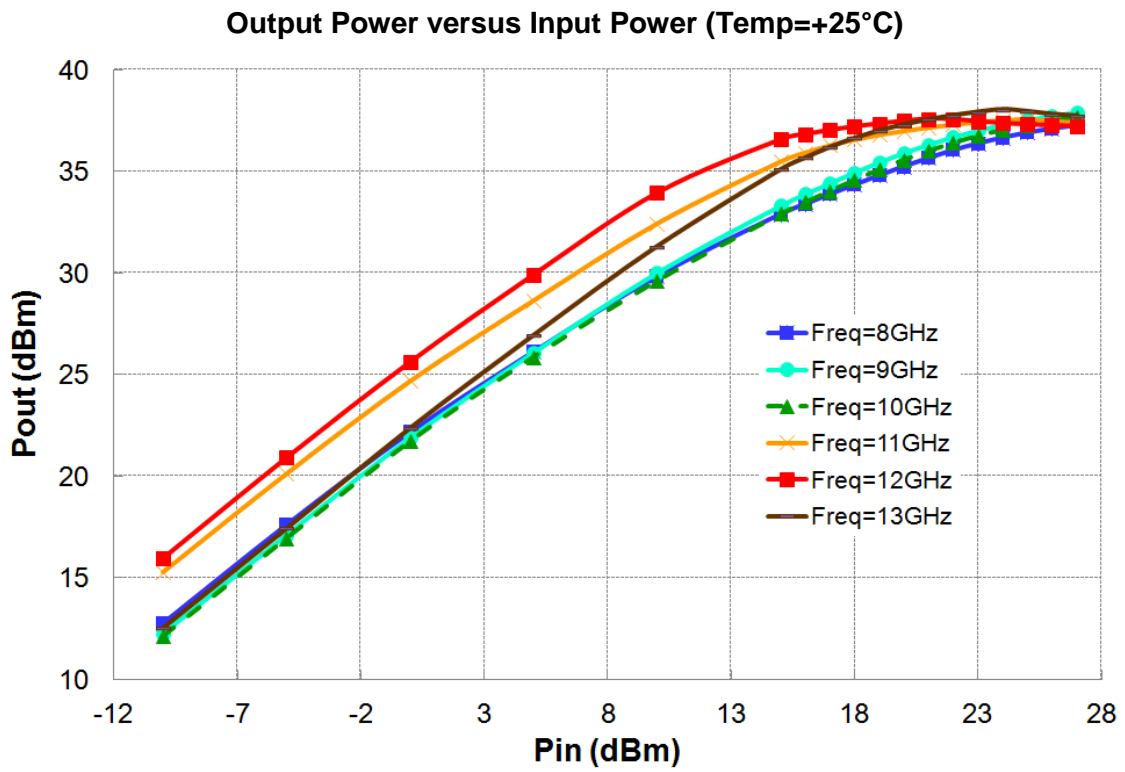
Typical Board Measurements (CW mode)

Tback side = +25°C, Vd = +25V, Idq = 200mA



Typical Board Measurements (CW mode)

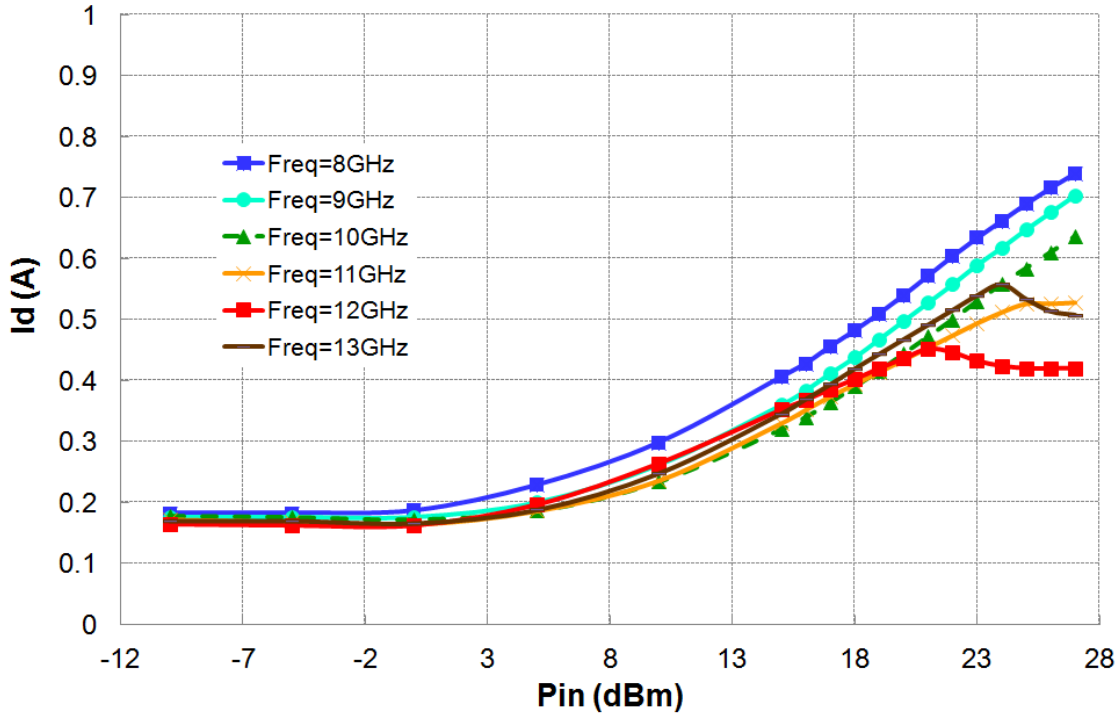
Tback side = +25°C, Vd = +30V, Idq = 200mA



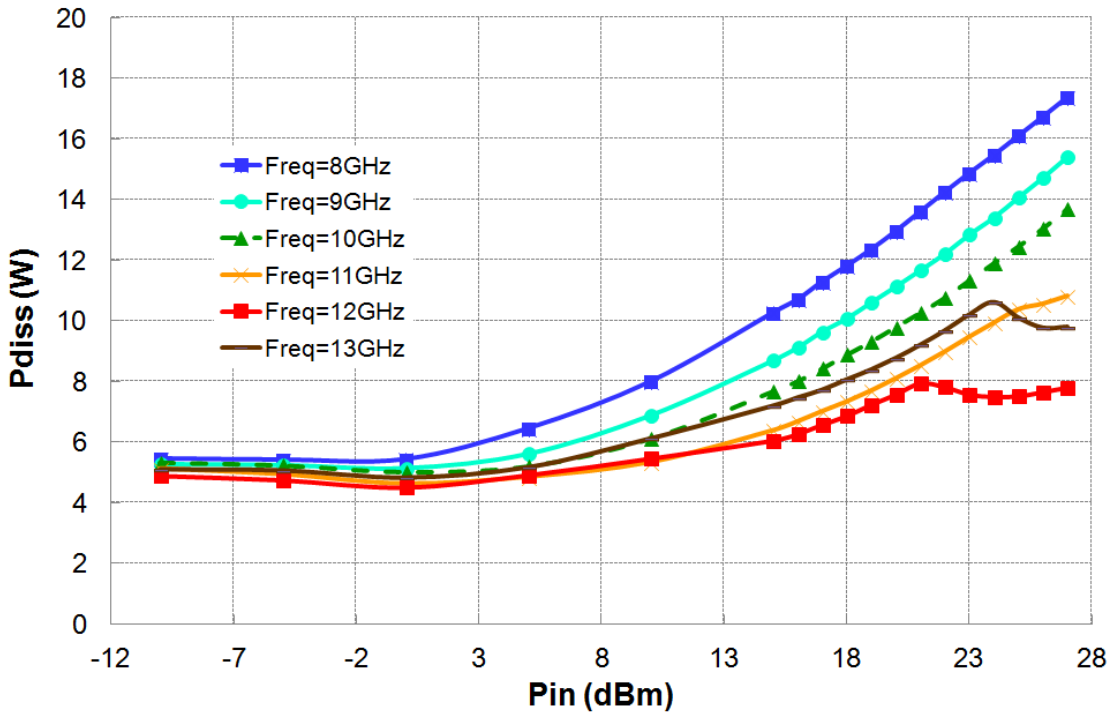
Typical Board Measurements (CW mode)

Tback side = +25°C, Vd = +30V, Idq = 200mA

Drain Current versus Input Power (Temp=+25°C)

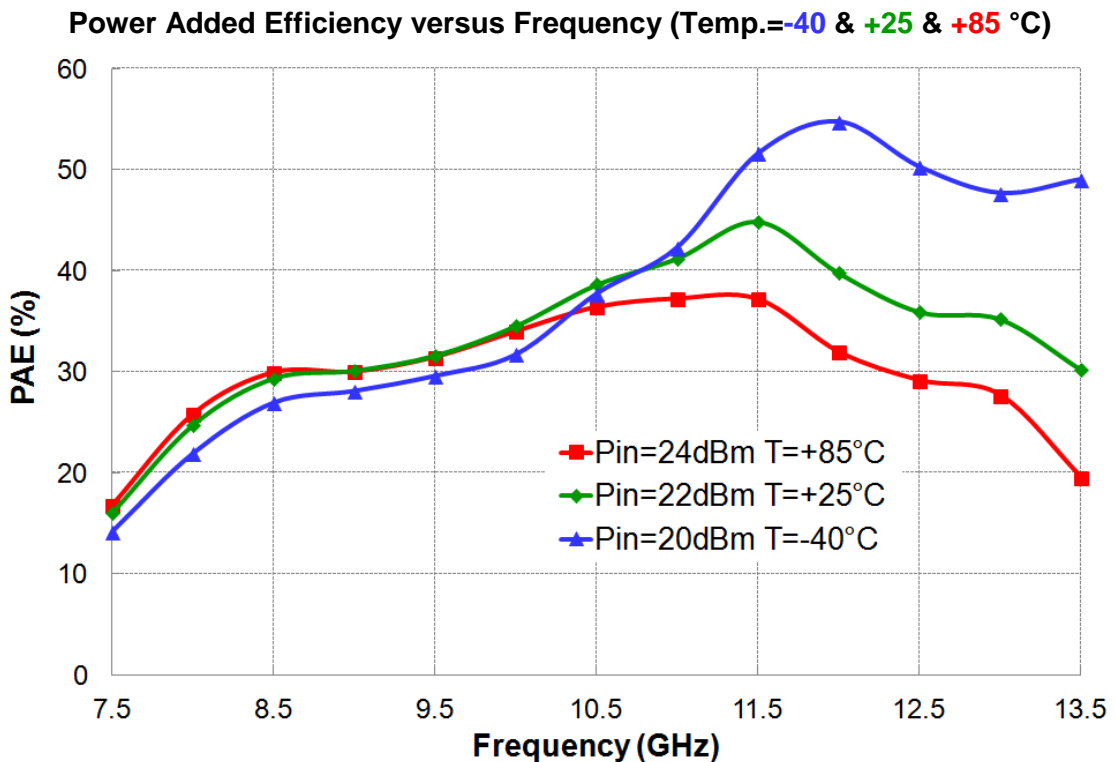
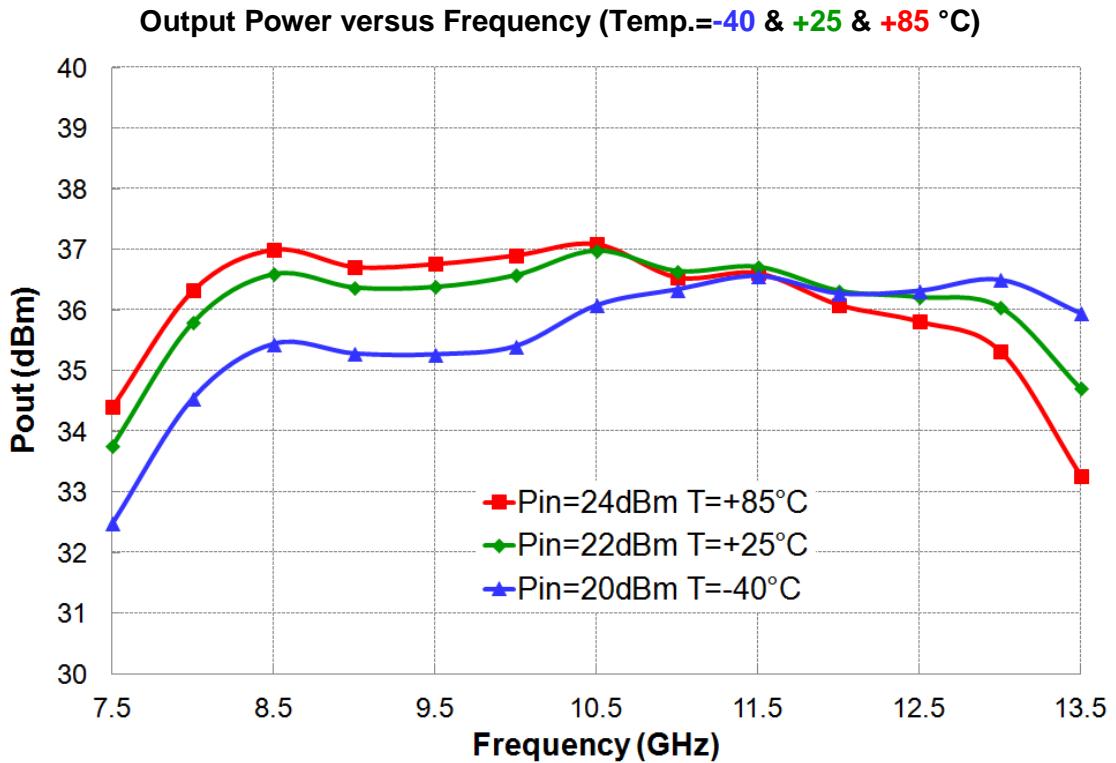


Dissipated Power versus Input Power (Temp=+25°C)



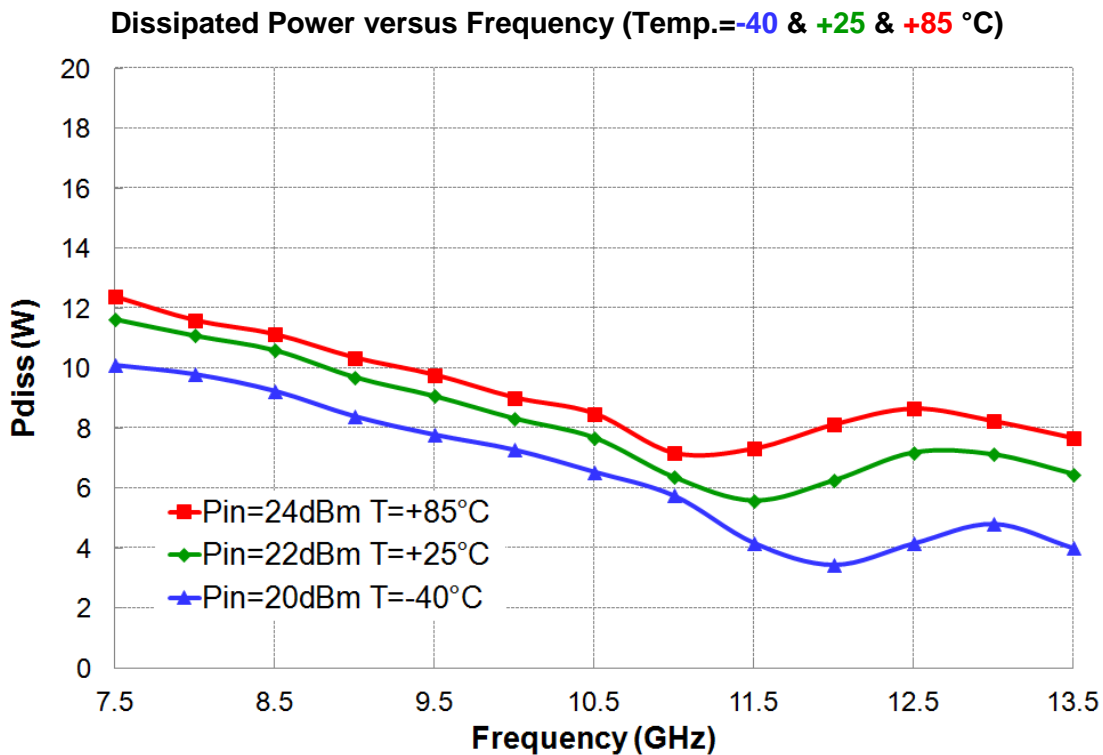
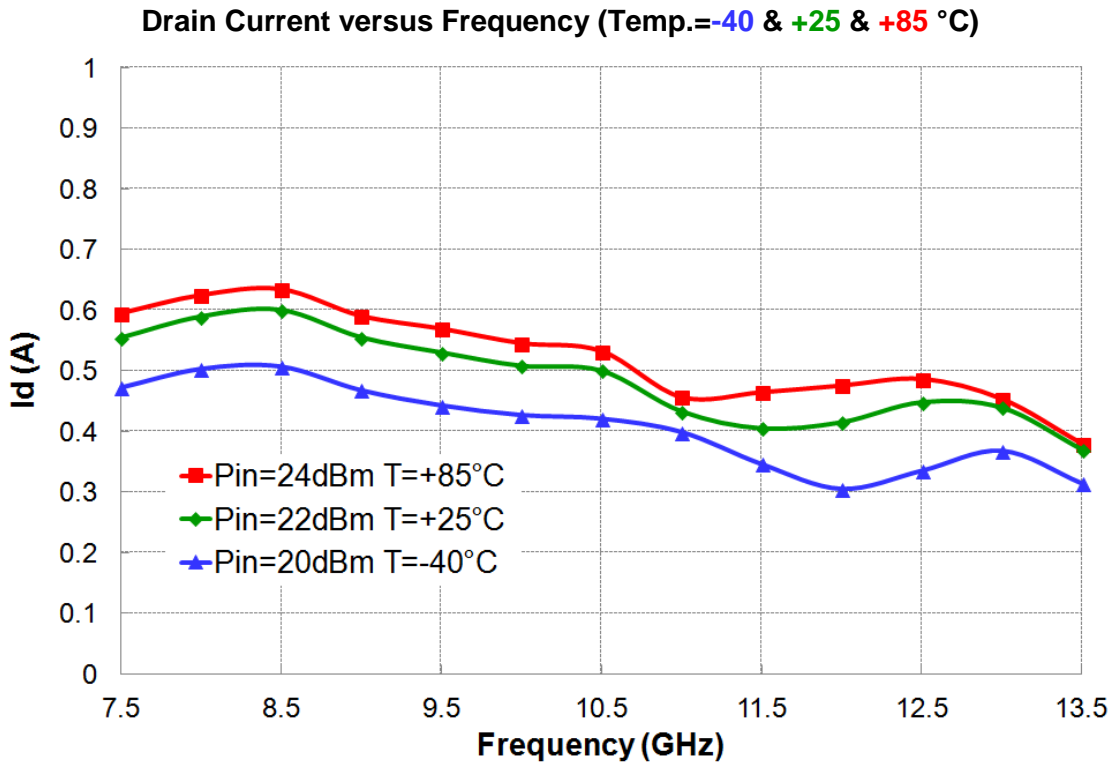
Typical Board Measurements (Pulsed mode)

Vd = +25V, Idq = 200mA @ Tback side = +25°C, Pulse width=25µs, Duty cycle =10%



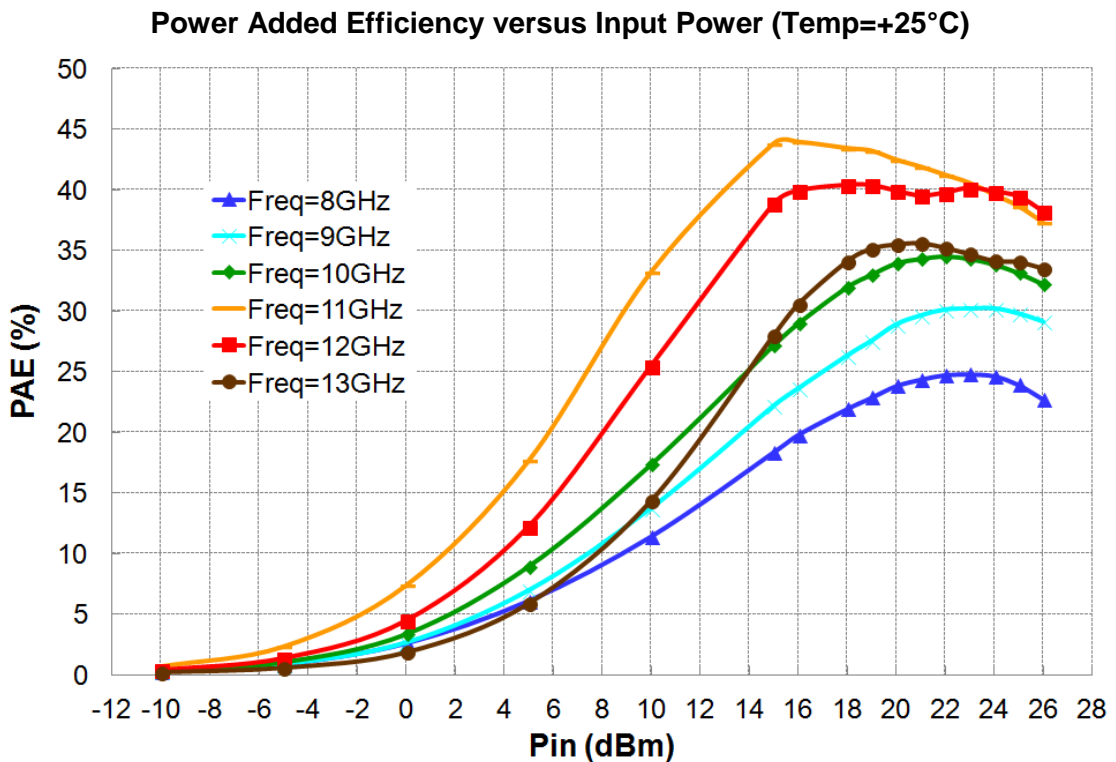
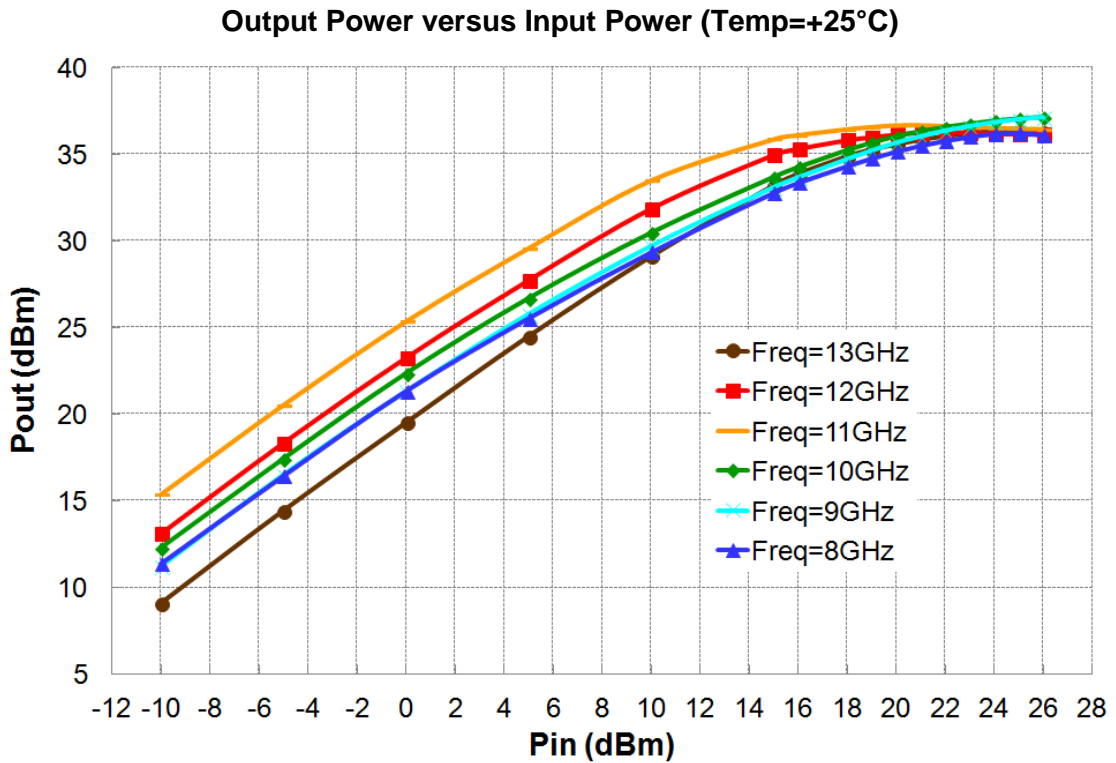
Typical Board Measurements (Pulsed mode)

Vd = +25V, Idq = 200mA @ Tback side = +25°C, Pulse width=25µs, Duty cycle =10%



Typical Board Measurements (Pulsed mode)

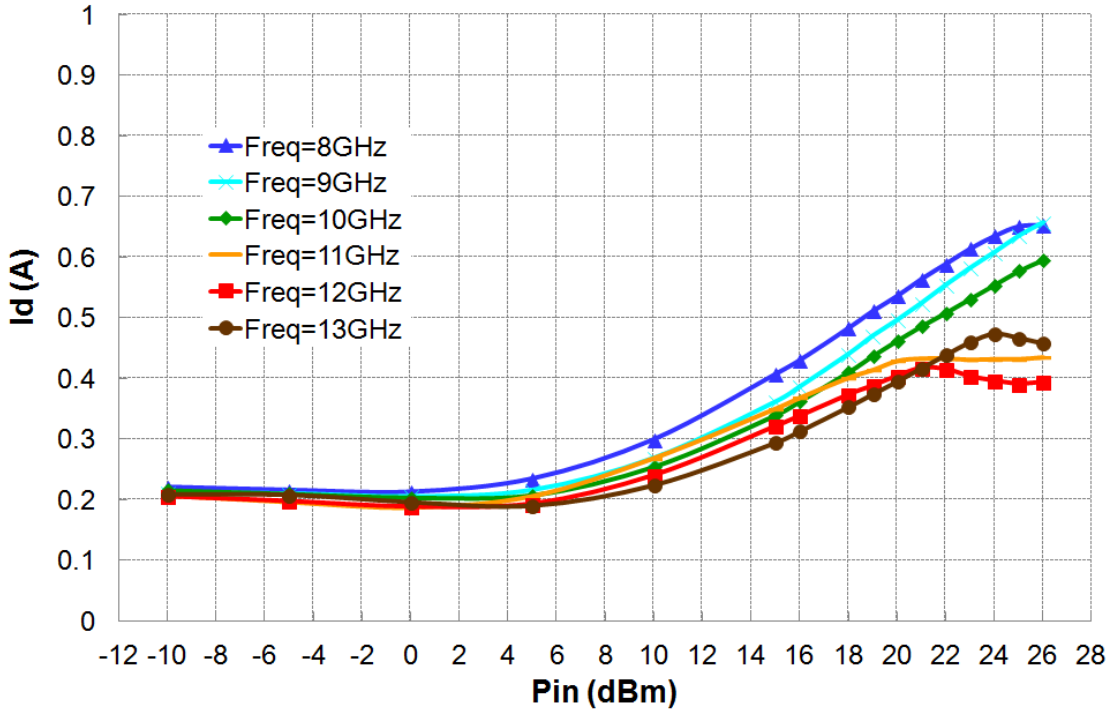
Tback side = +25°C, Vd = +25V, Idq = 200mA, Pulse width=25µs, Duty cycle =10%



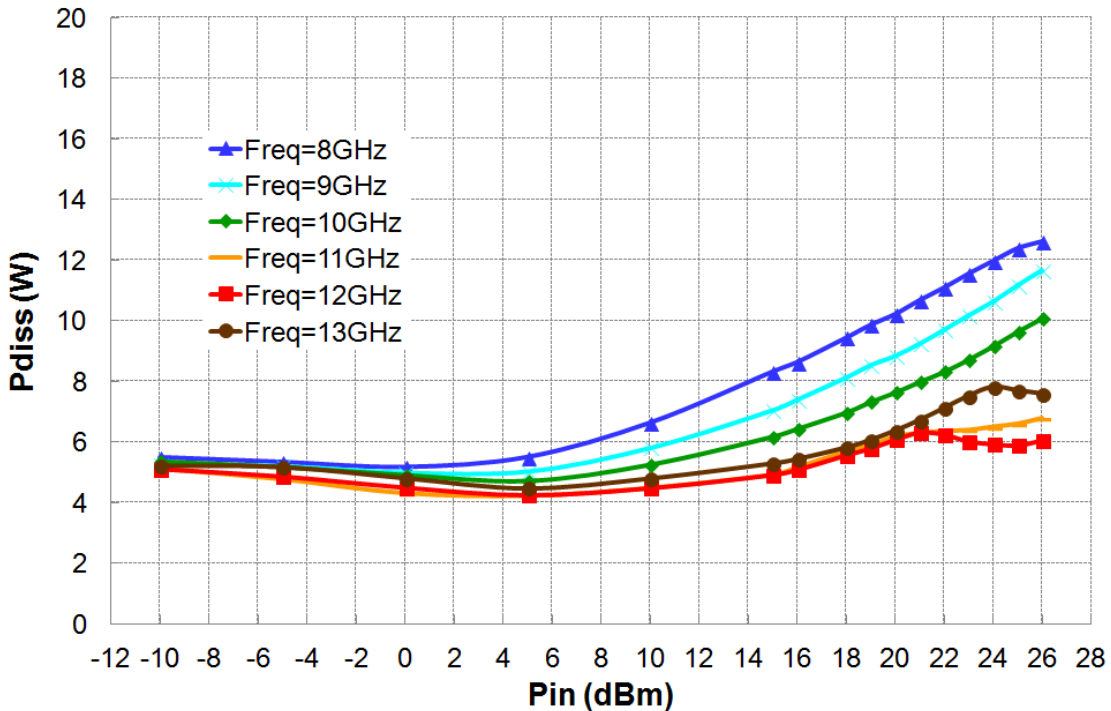
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Drain Current versus Input Power (Temp=+25°C)

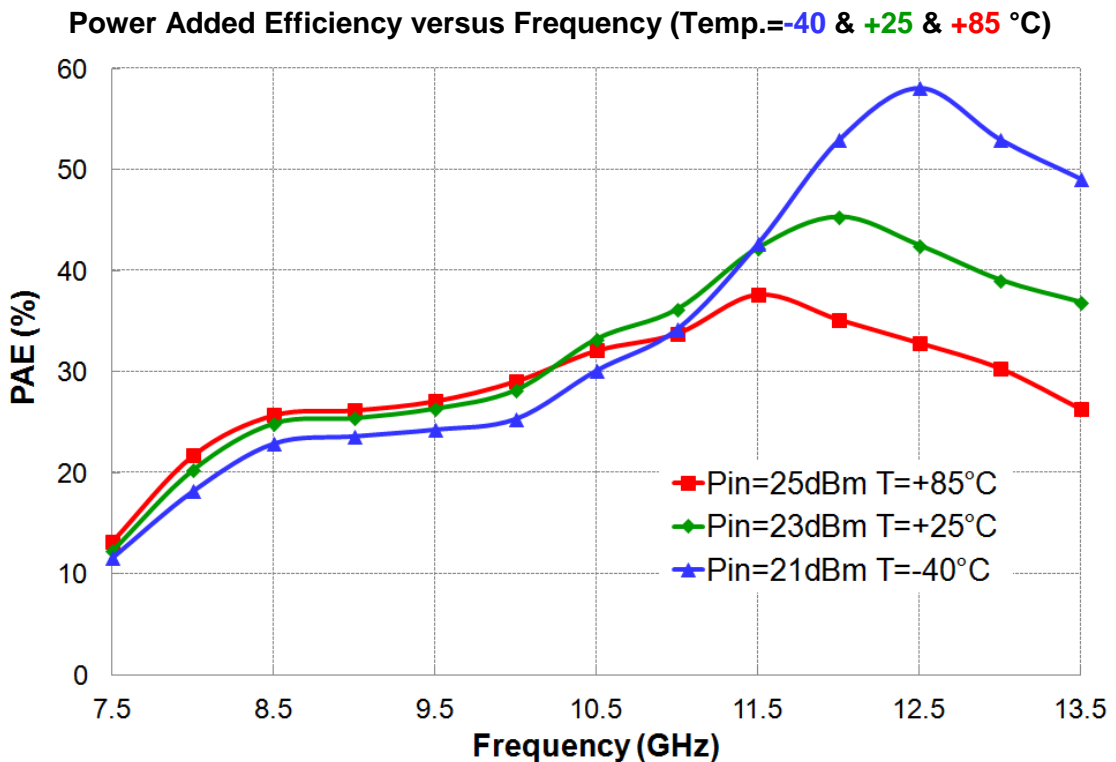
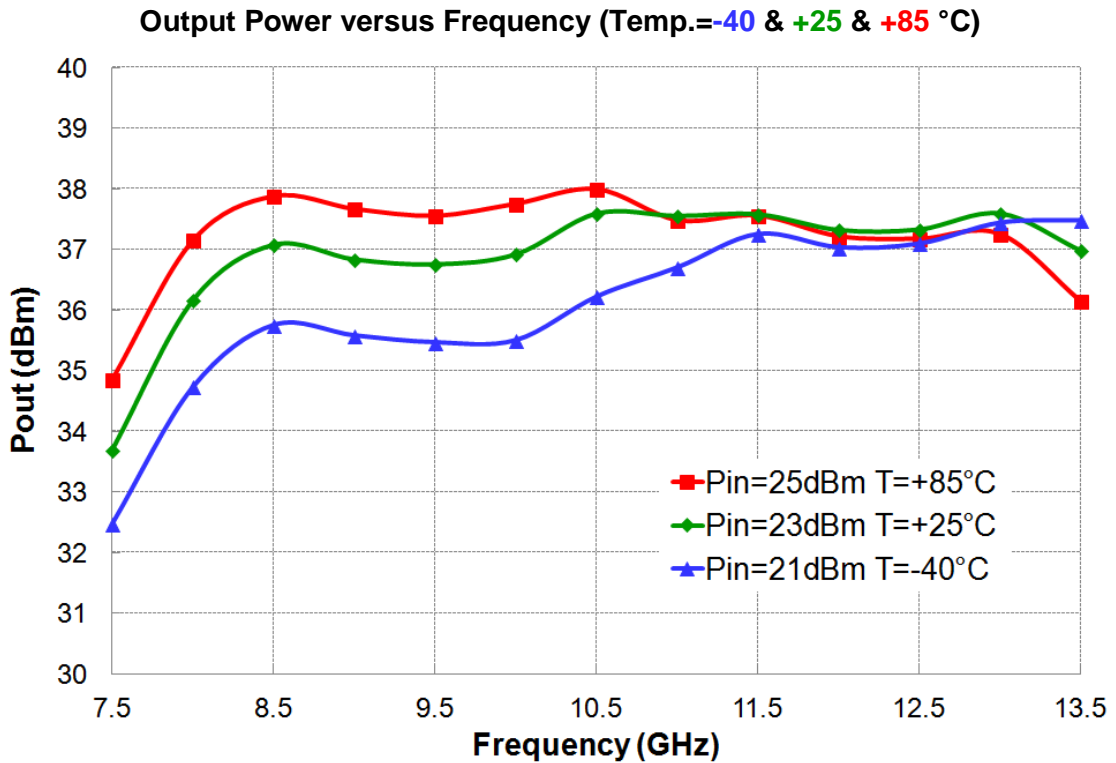


Dissipated Power versus Input Power (Temp=+25°C)



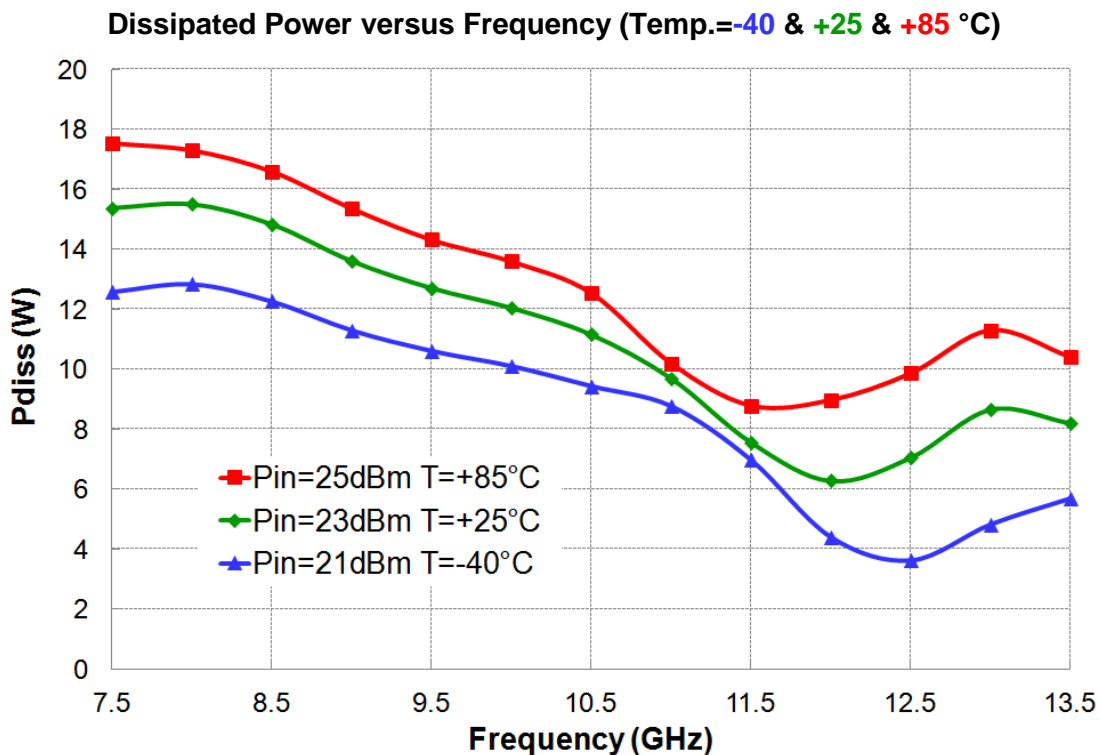
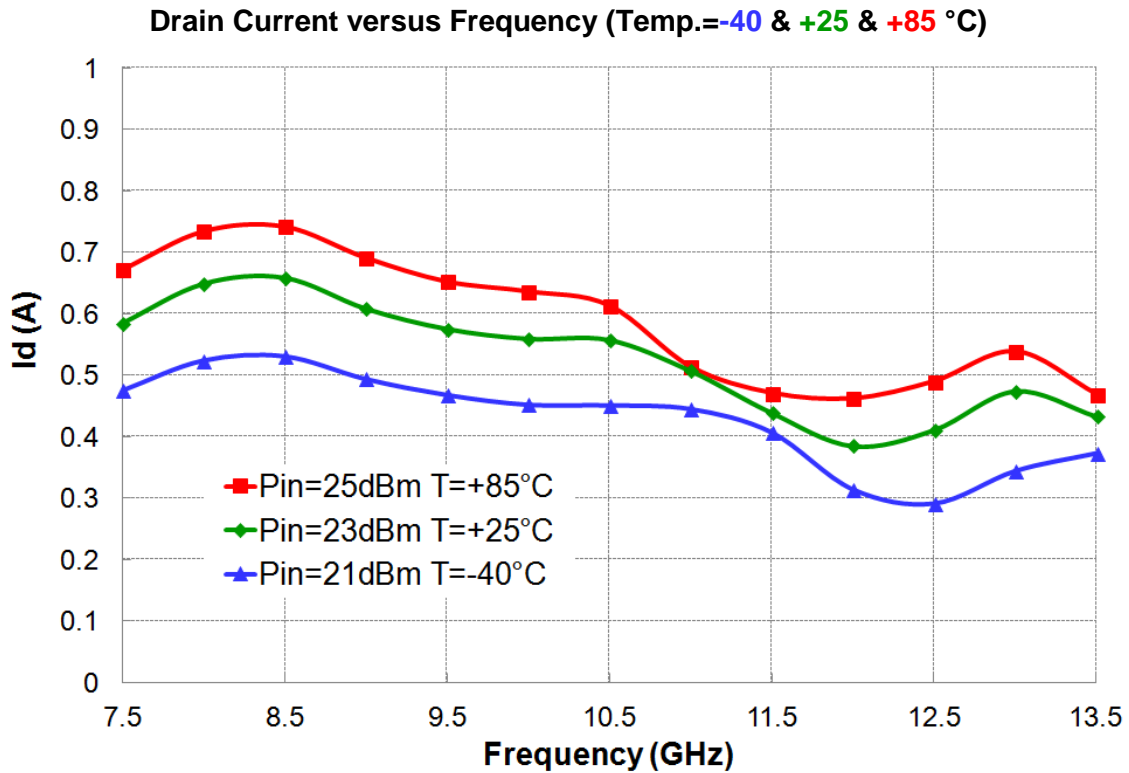
Typical Board Measurements (Pulsed mode)

Vd = +30V, Idq = 200mA @ Tback side = +25°C, Pulse width=25µs, Duty cycle =10%



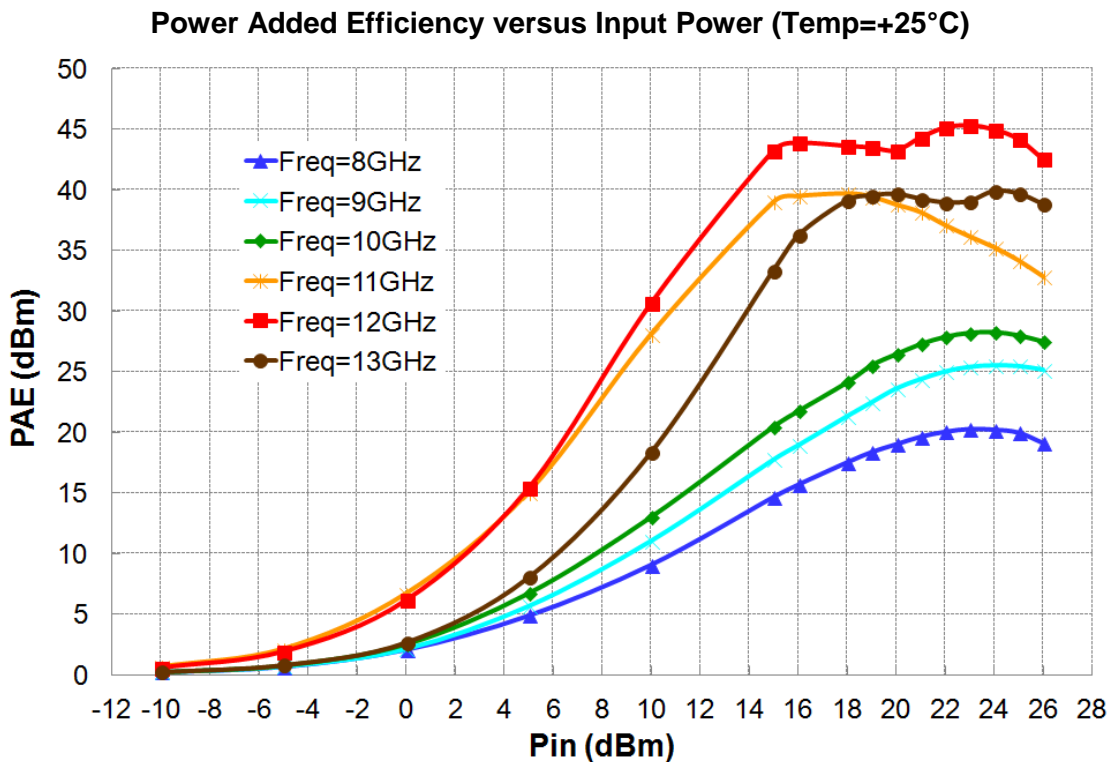
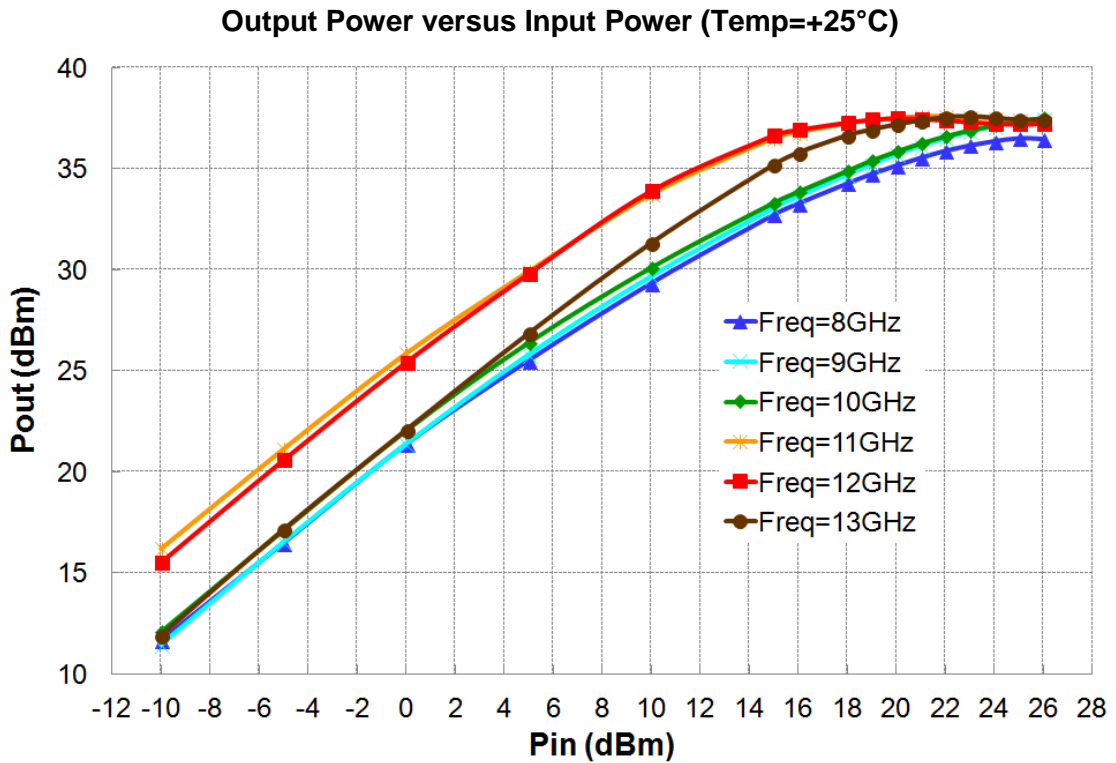
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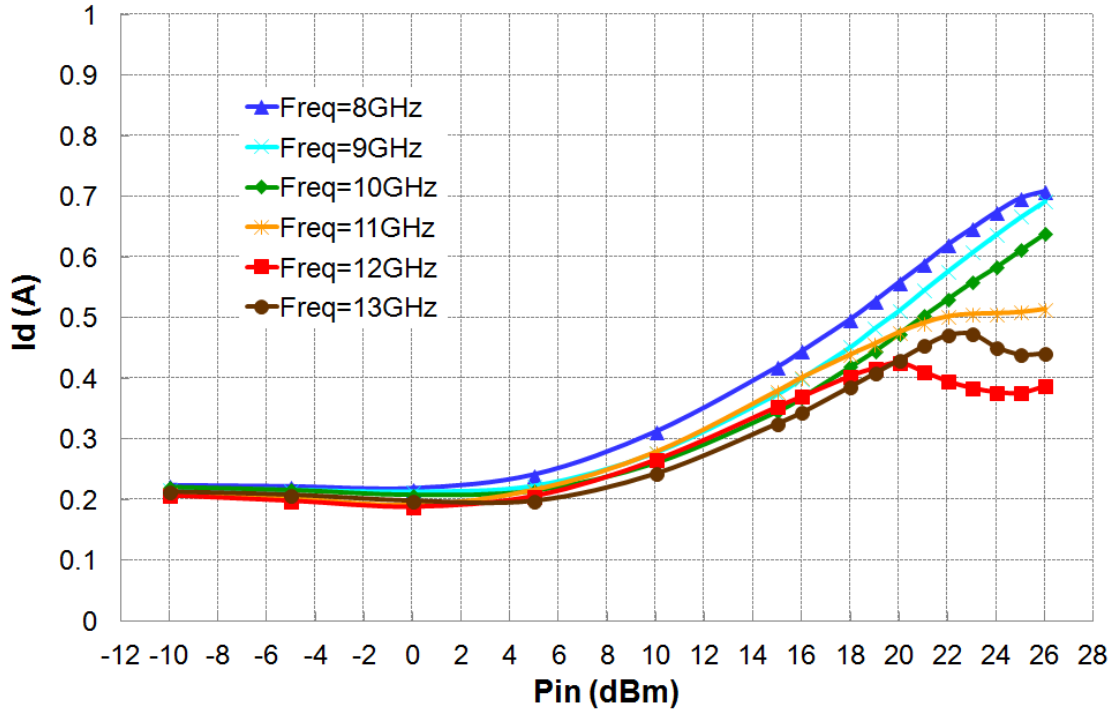
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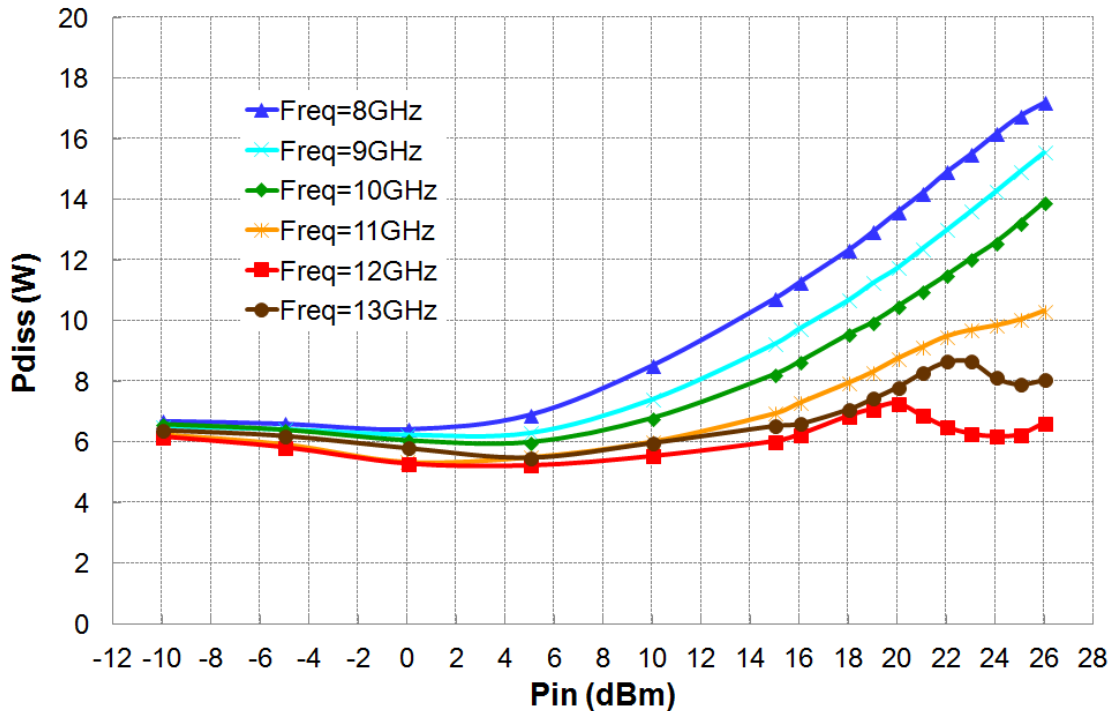
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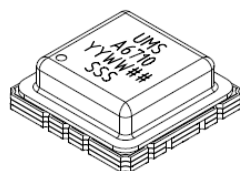
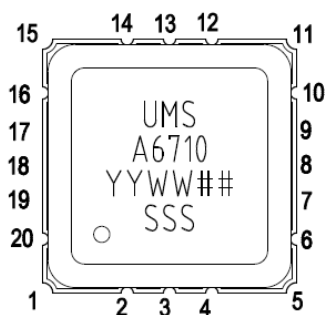
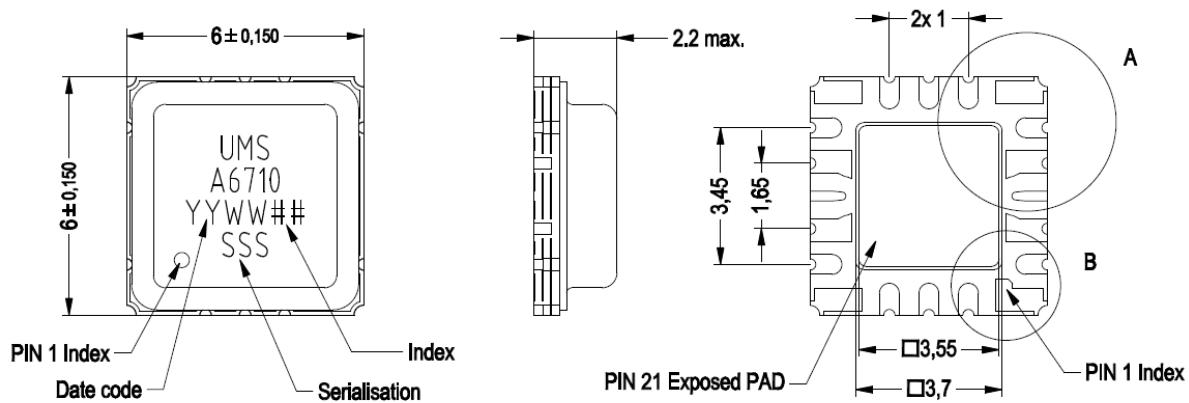
Drain Current versus Input Power (Temp=+25°C)



Drain Current versus Input Power (Temp=+25°C)

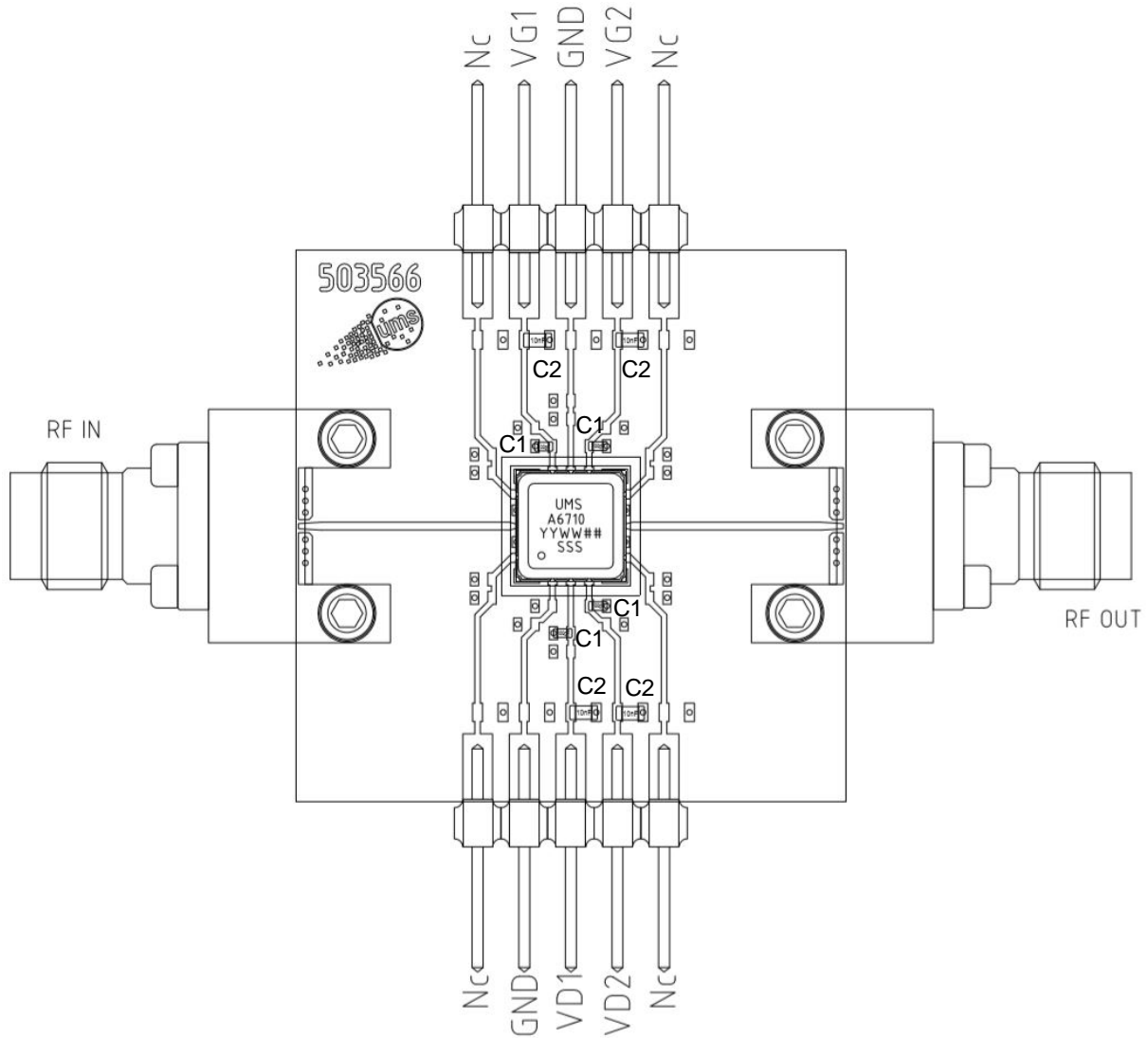


Mechanical data



1- GND	8- RF OUT	15- GND
2- GND	9- GND	16- Nc
3- VD1	10- GND	17- GND
4- VD2	11- GND	18- RF IN
5- GND	12- VG2	19- GND
6- Nc	13- GND	20- Nc
7- GND	14- VG1	21- GND

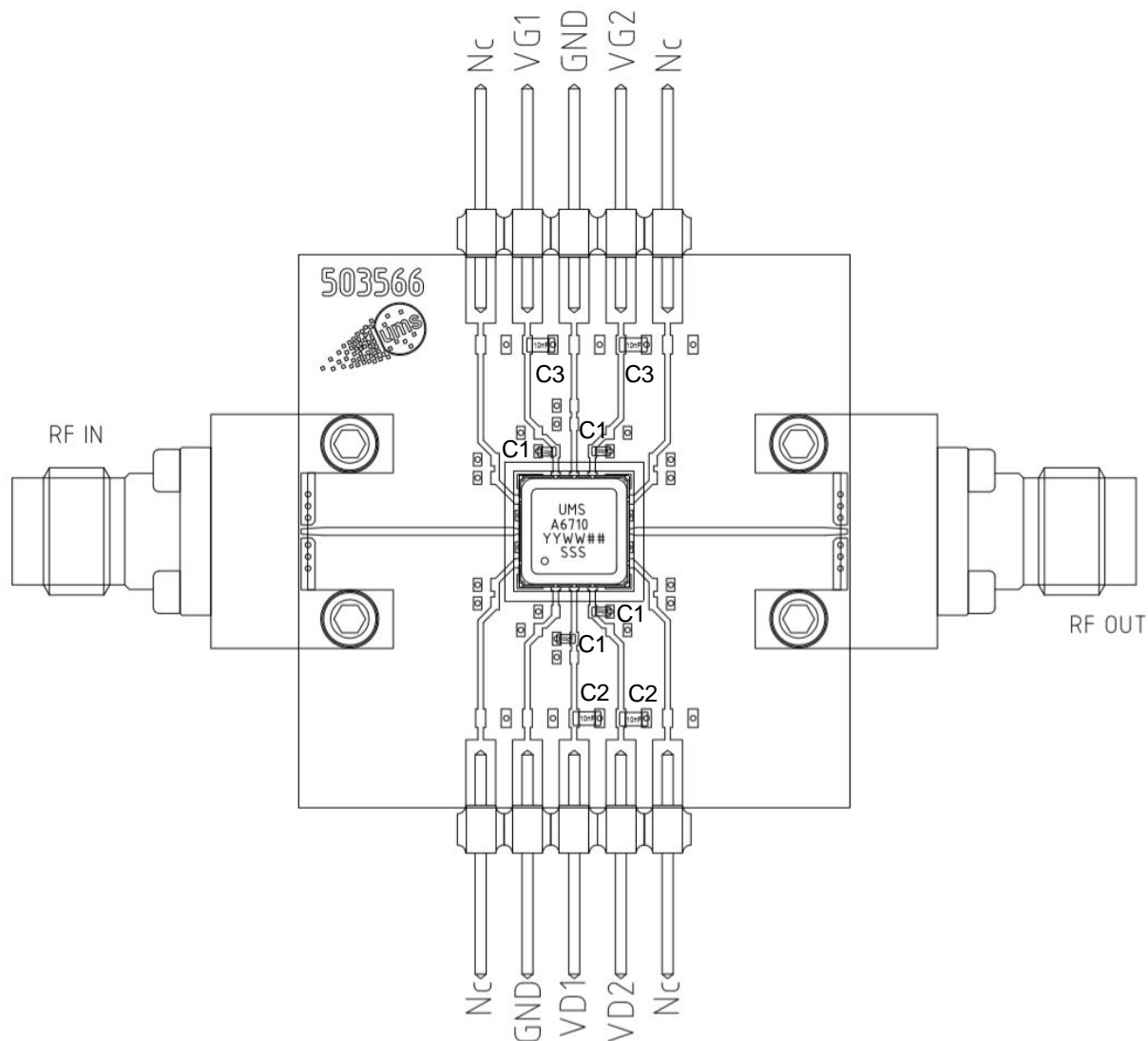
Recommended assembly drawing in CW mode



Bill of Materials

Label	Value	Description
C1	RF	Capa 100pF +-10% 50V
C2	RF	Capa 10nF +-20% 50V

Recommended assembly drawing in gate pulsed mode



Bill of Materials

Label	Value	Description
C1	RF	Capa 120pF +-10% 50V
C2	RF	Capa 10nF +-20% 50V
C3	RF	Capa 0nF (no capacitor)

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017 available at <http://www.ums-gaas.com>.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <http://www.ums-gaas.com>.

Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS package products.

FAB Type Surface Mount Hermetic Package

Refer to the application note AN0024 available at <http://www.ums-gaas.com> for assembly recommendations for the UMS FAB package products.

Ordering Information

Chip form: CHA6710-FAB/XY
Stick: XY = 24

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