25W X-Band High Power Amplifier

GaN Monolithic Microwave IC

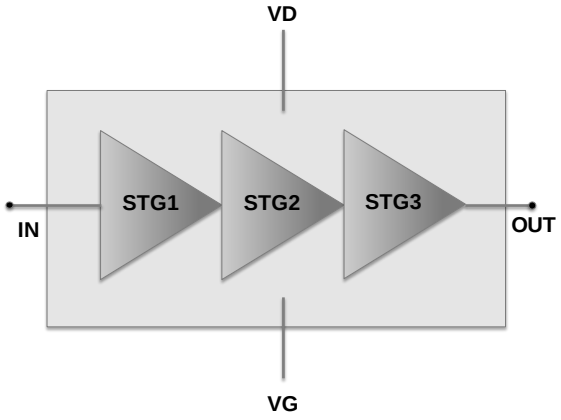
Description

The CHA8212-99F is a three-stage GaN High Power Amplifier in the frequency band 8.5-11.5GHz. This HPA typically provides 25W of output power associated to 36% of Power Added Efficiency. The small signal gain exhibits more than 30dB. The overall power supply is of 28V/0.84A (quiescent current).

This circuit is a very versatile amplifier for high performance systems.

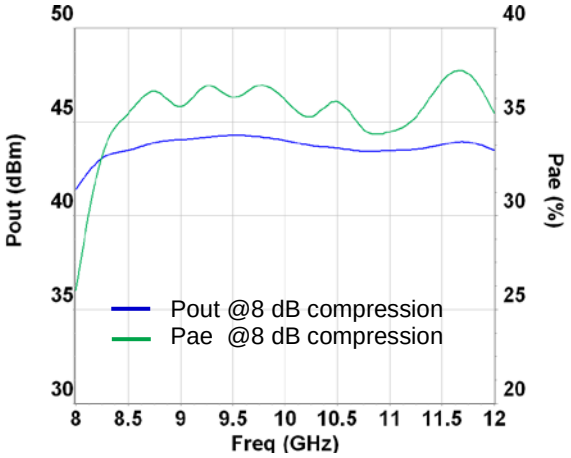
The circuit is dedicated to defence applications and well suited for a wide range of microwave applications and systems.

The part is developed on a robust 0.25µm gate length GaN HEMT process and is available as a bare die.



Main Features

- 8.5-11.5 GHz frequency range
- Linear Gain is 34 dB
- 44dBm Pout for +20dBm input power
- Associated PAE is 36% for +20dBm input power
- Associated Id is 2.5A for +20dBm input power
- DC bias: Vd=28Volts @Idq=0.84A
- Chip size 5.63x4.23x0.1mm



Main Electrical Characteristics

Tb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	8.5		11.5	GHz
Gain	Linear Gain		34		dB
PAE	Power Added Efficiency (Pin=20 dBm)		36		%
Pout	Output Power (Pin=20 dBm)		44		dBm

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Specifications (Pulsed mode)

Tb.= +25°C, Vd = +28V, Idq = 840mA, Pulse width = 25µs, Duty cycle = 10%

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	8.5		11.5	GHz
Gain	Linear Gain		34		dB
Pout	Output Power (Pin = 20dBm)		44		dBm
PAE	Associated Power Added Efficiency (Pin = 20dBm)		36		%
Id	Associated current (Pin = 20dBm)		2.5		A
S11	Input Return Loss		-14		dB
S22	Output Return Loss		-12		dB
Idq	Quiescent Current		0.84		A
Vd	Drain Voltage		28		V
Vg	Gate Voltage		-3.4		V

Absolute Maximum Ratings (1)

Tb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	55	V
Id_stg1	1st stage drain current	0.5	A
Id_stg2	2nd stage drain current	1	A
Id_stg3	3rd stage drain current	3	A
Pin	Maximum peak input power overdrive	26	dBm
Tj	Junction temperature	230	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Temperature Range

Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

These values are representative of measurements done in test fixture with a bonding wire of typically 0.25 to 0.3nH.

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Typical Bias Conditions

Tb.= +25°C

Symbol	Pad Nº	Parameter	Values	Unit
VG12,	24	Pulsed gate voltage tuned for Idq ~ 0.84A	-3.4	V
VG3	9, 17			
VD	4, 7, 11, 15, 19	Drain Voltage	28	V

“Power ON” sequence

1. Bias HPA gate voltage at Vg close to Vpinch-off (example: Vg ≈ -5V).
2. Apply Vd bias voltage (Example: Vd = 28V).
3. Increase slowly Vgs up to quiescent bias drain current Ids0 (pulsed applied on the gate: 840mA).
4. Apply RF signal

“Power OFF” sequence

1. Turn off RF signal
2. Bias HPA gate voltage at Vg close to Vpinch-off (example: Vg ≈ -5V)
3. Set Vd to 0V.
4. Turn off Vd supply.
5. Turn off Vg supply.

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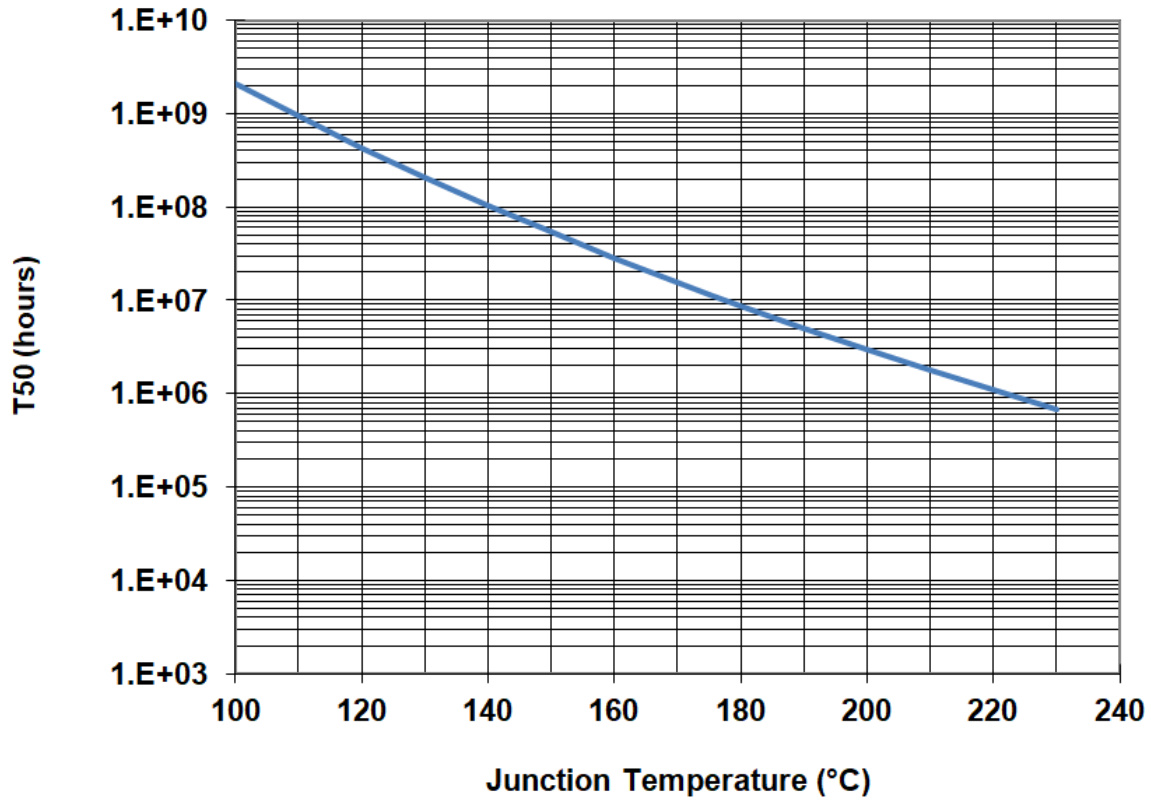
Device thermal information

The device thermal performances below are based on UMS rules to evaluate the junction temperature.
This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHA8212-99F is manufactured (GaN HEMT 0.25µm).
The temperature Tb_{chip} is defined as the chip backside temperature and $Tb_{carrier}$ is defined as the carrier backside temperature. The thermal resistance (Rth_eq) is given for the full circuit, and assumes CW and pulsed operation mode are given in the table.

Thermal Resistance(1)	Rth_eq	Tb_{chip} = 85°C, Vd = 28V, Id_drive = 2.74A Pin = 25dBm, Pout = 44.3dBm Pdiss = 50W CW	1.54	°C/W
Junction Temperature	Tj		162	°C
Median Life	T50		$2.83^{E}7$	Hrs

(1) Thermal resistance measured at the back of the chip

Median Life Time versus Junction Temperature



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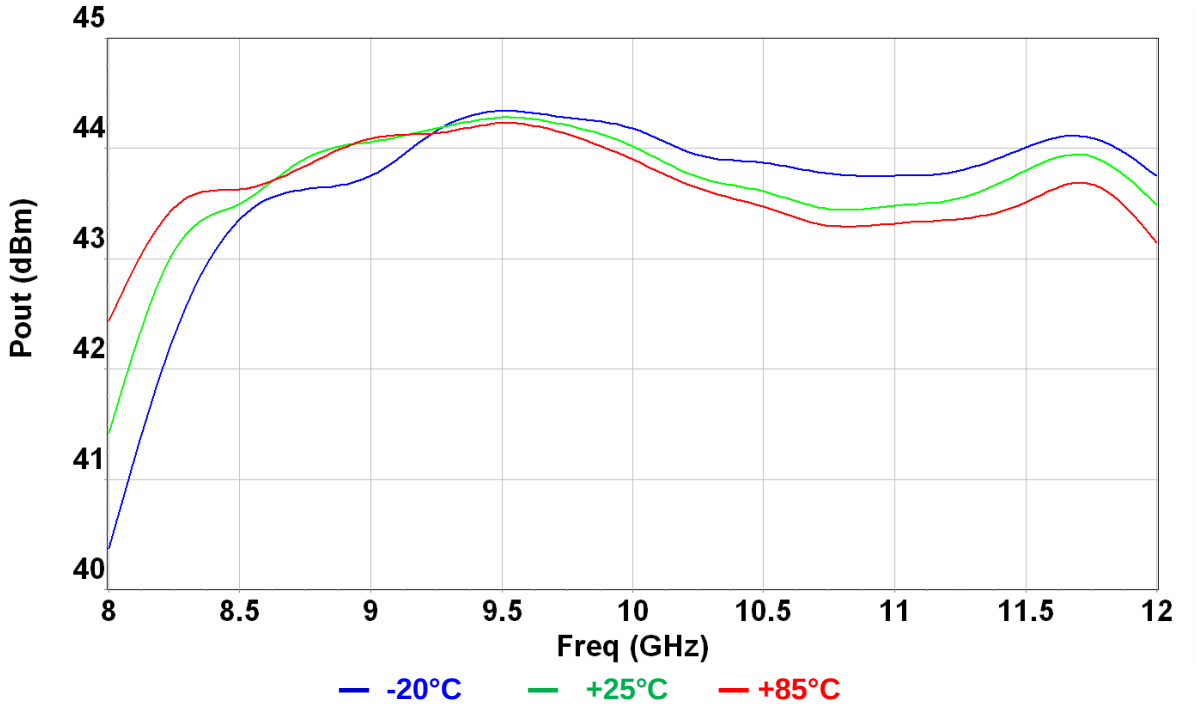
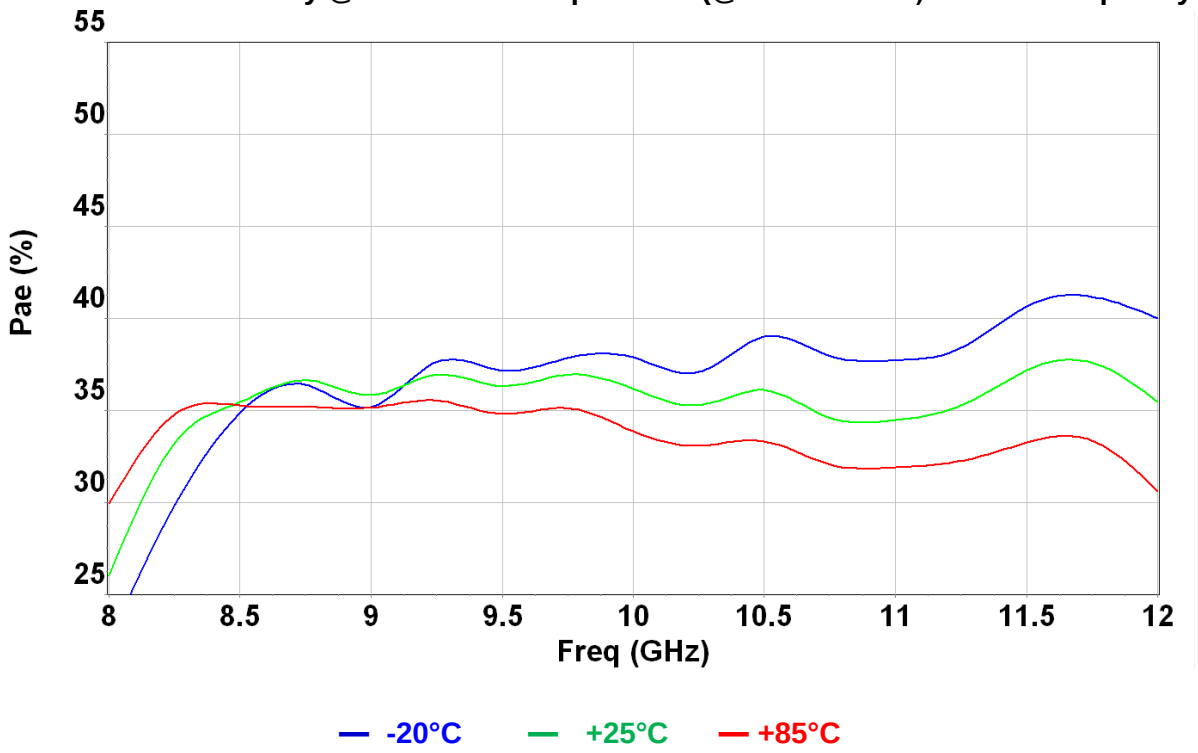
Typical Test Fixture Measurements: Non-linear performances

Tb=+25°C/+85°C/-20°C, Vd = +28V, Idq = 840mA @25°C,
Pulse width = 25µs, Duty cycle = 10%

Output Power @ 8 dB Gain compression (@Pin ≈ 20dBm) versus Frequency



Power Added Efficiency @ 8 dB Gain compression (@Pin ≈ 20dBm) versus Frequency



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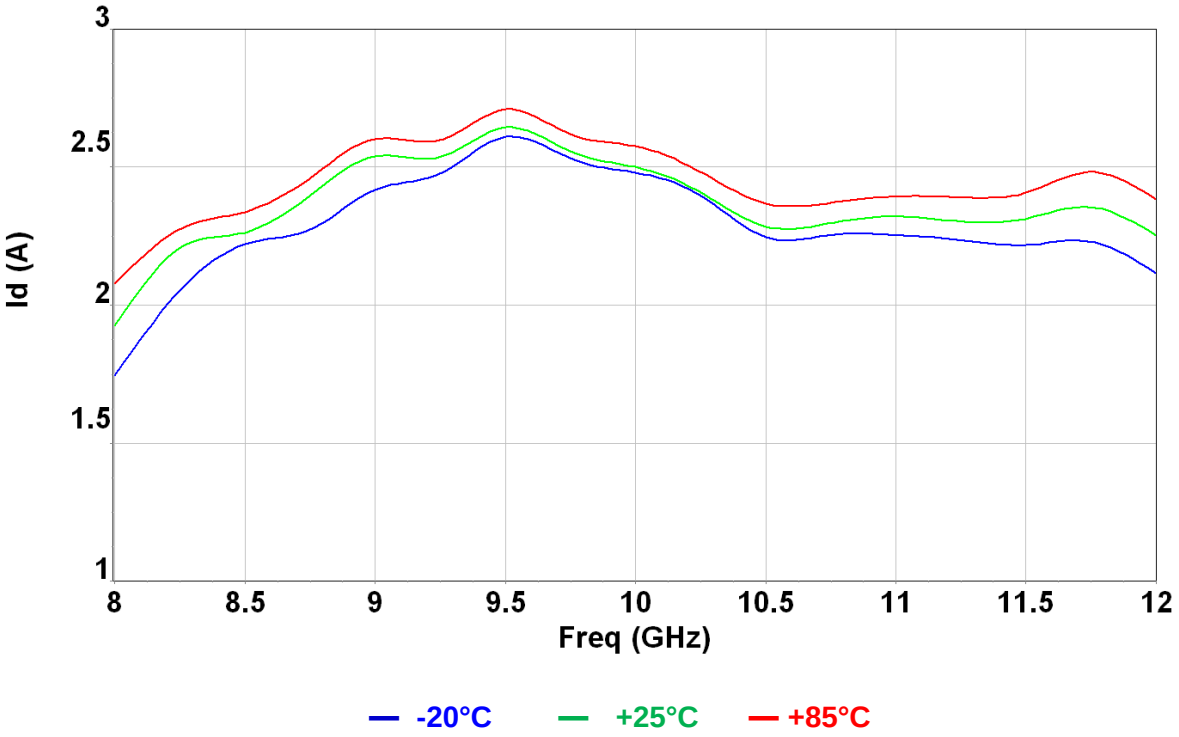
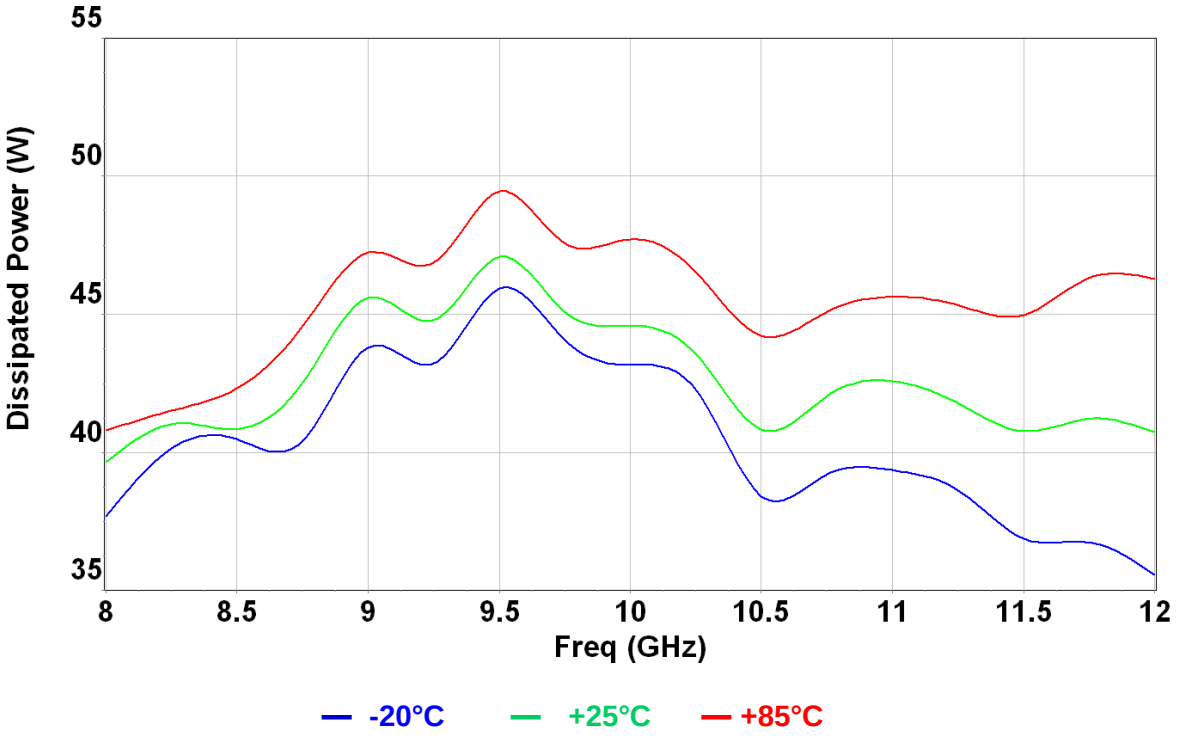
Typical Test Fixture Measurements: Non-linear performances

Tb.= +25°C/+85°C/ -20°C, Vd = +28V, Id = 840mA @25°C,
Pulse width = 25µs, Duty cycle = 10%

Drain Current @ 8 dB Gain compression (@Pin ≈ 20dBm) versus Frequency



Dissipated Power @ 8 dB Gain compression (@Pin ≈ 20dBm) versus Frequency



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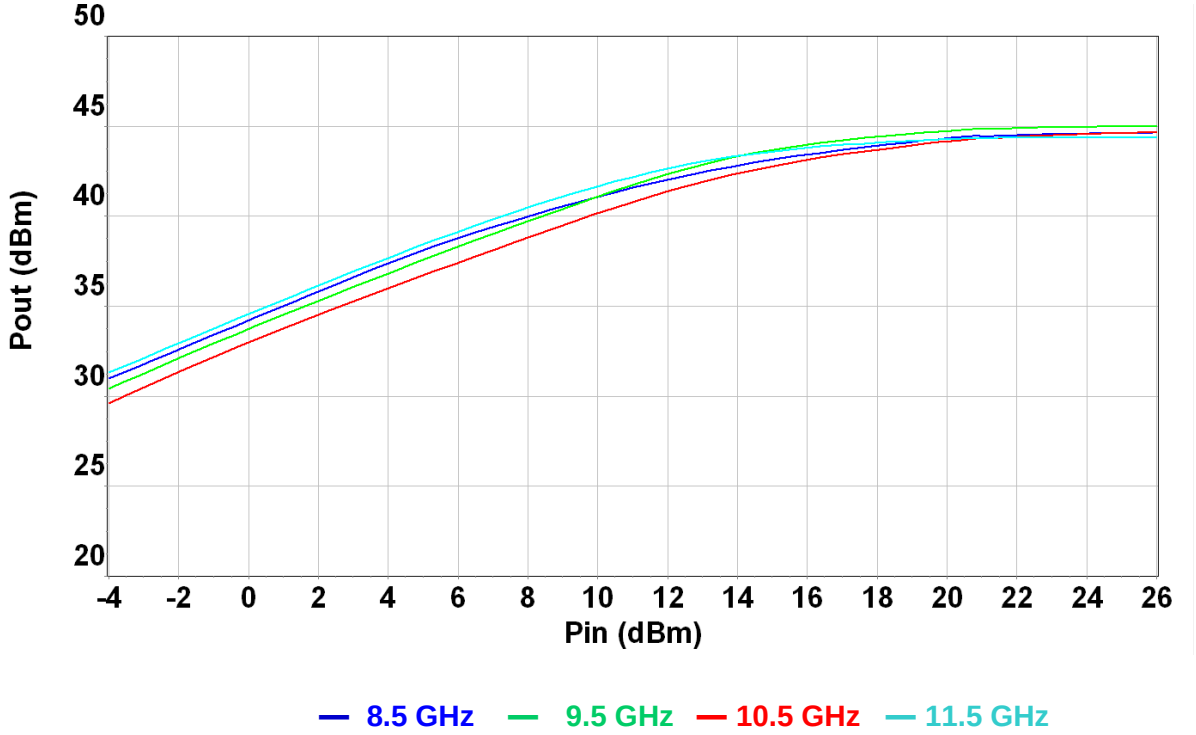
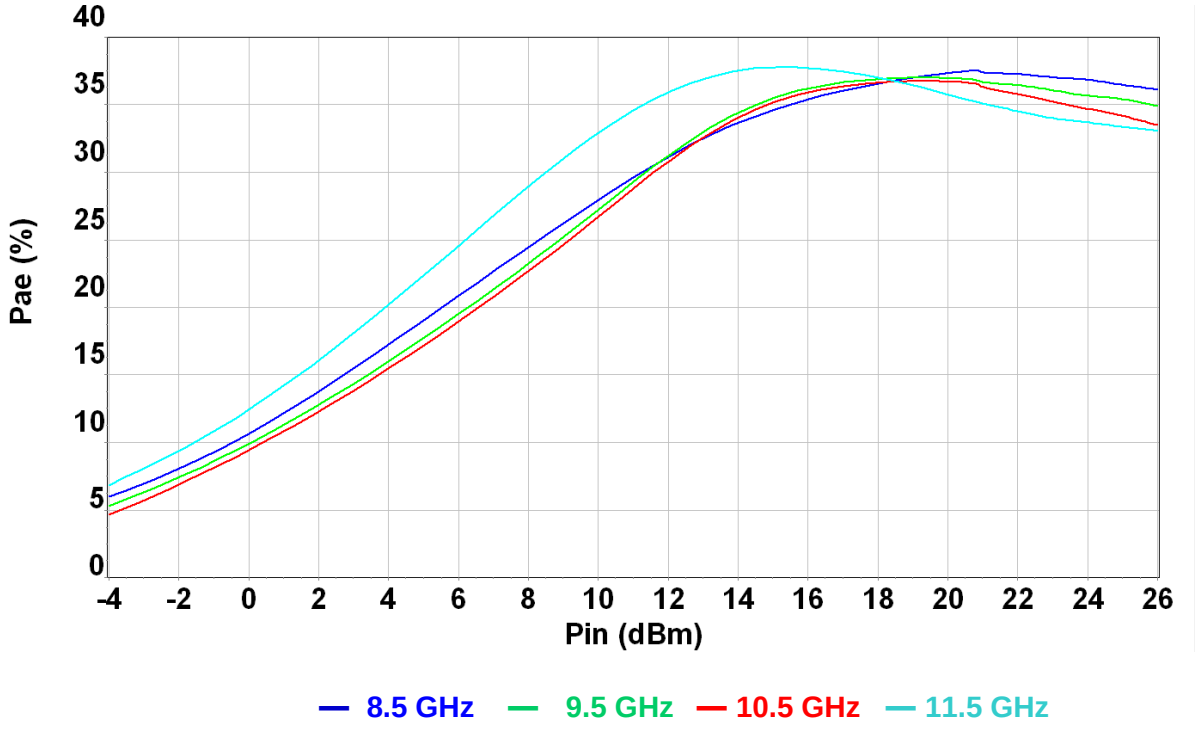
Typical Test Fixture Measurements: Non-linear performances

Tb.= +25°C, Vd = +28V, Id = 840mA, Pulse width = 25µs, Duty cycle = 10%

Output Power versus Input Power



Power Added Efficiency versus Input Power



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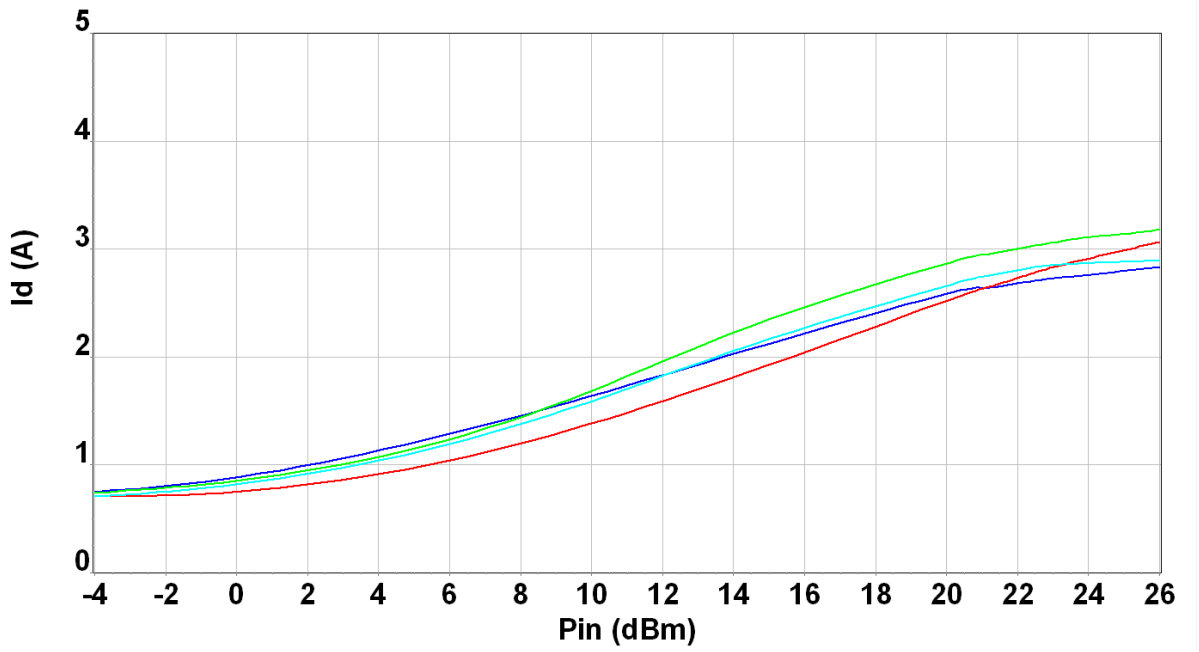
Typical Test Fixture Measurements: Non-linear performances

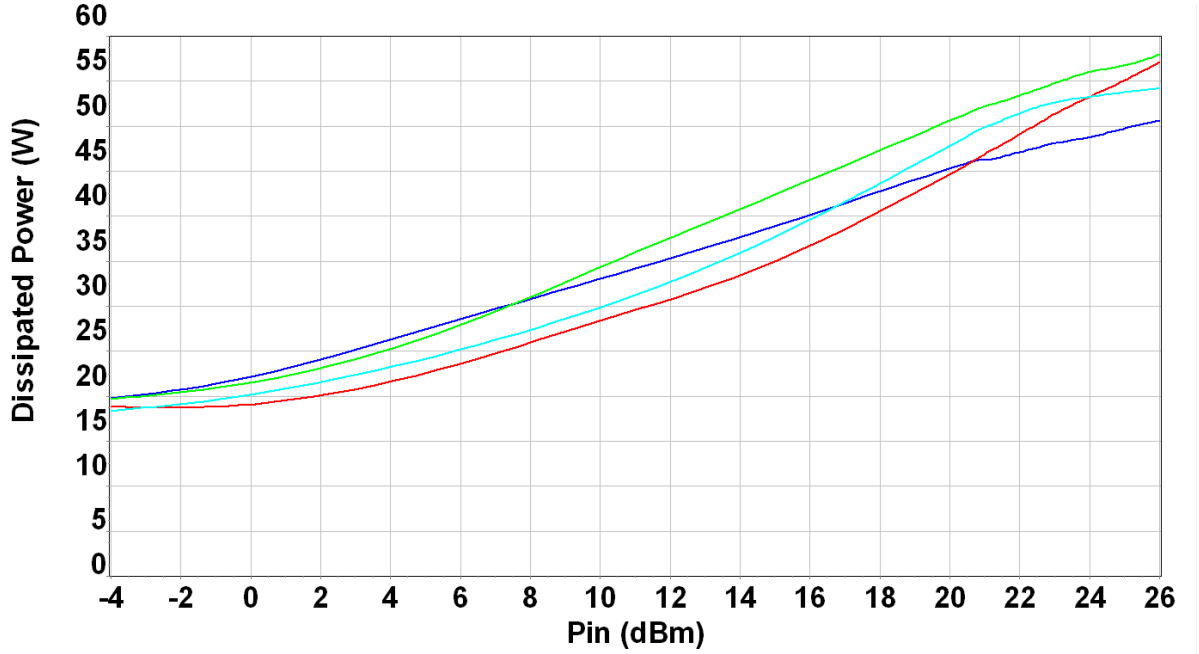
Tb.= 25°C, Vd = +28V, Id = 840mA, Pulse width = 25µs, Duty cycle = 10%

Drain Current versus Input Power



— 8.5 GHz — 9.5 GHz — 10.5 GHz — 11.5 GHz

Dissipated Power versus Input Power



— 8.5 GHz — 9.5 GHz — 10.5 GHz — 11.5 GHz

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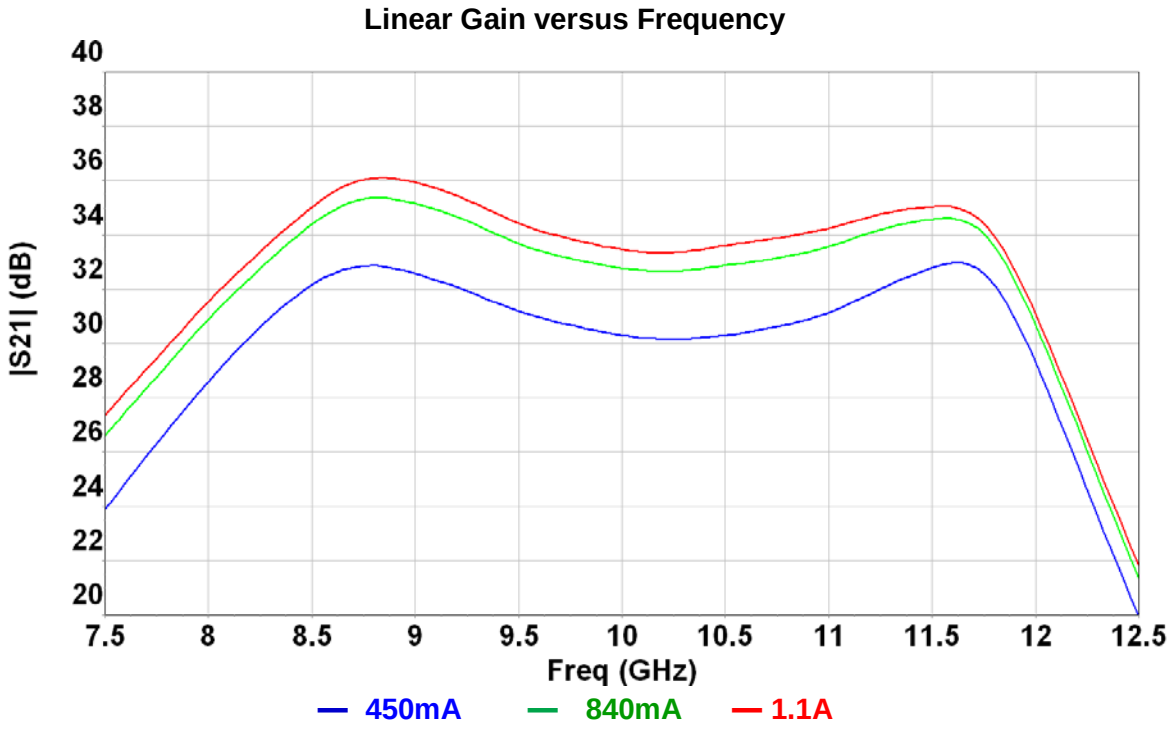
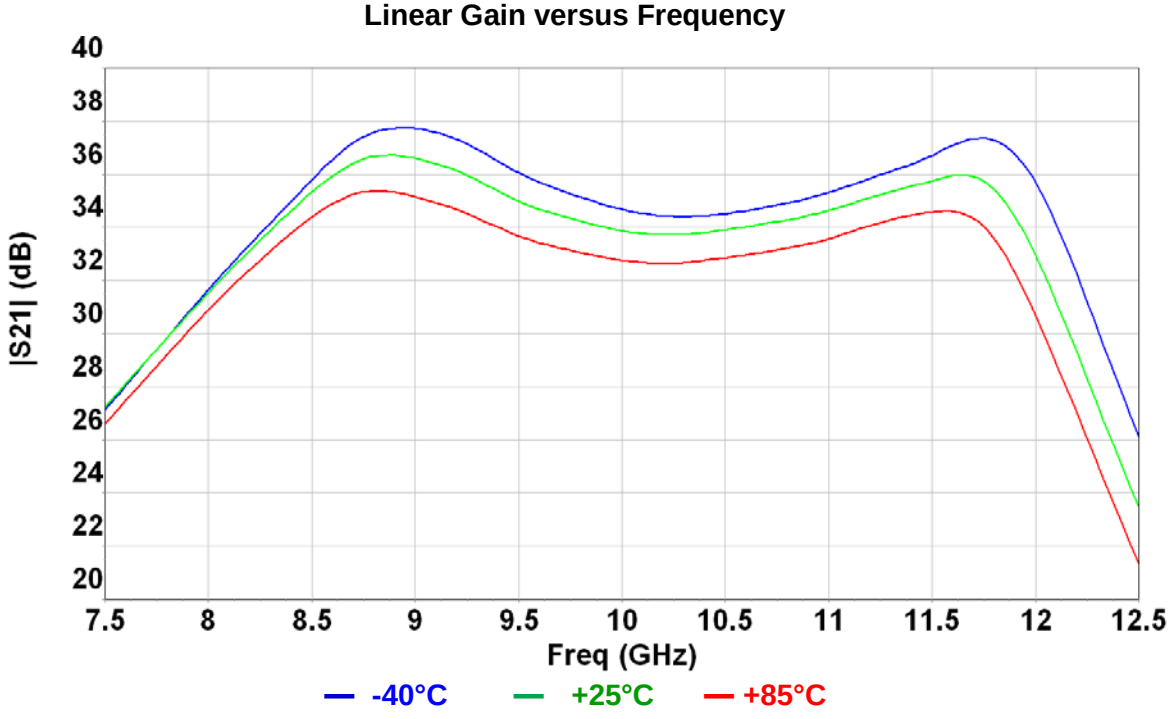
Typical Test Fixture Measurements: Small Signal Performances

Tb.= 25°C, Vd = +28V, Id = 450mA, 840mA & 1.1A, Pulse width = 25µs, Duty cycle = 10%



Vd = +28V, Id = 840mA (fixed @25°C)
Pulse width = 25µs, Duty cycle = 10%



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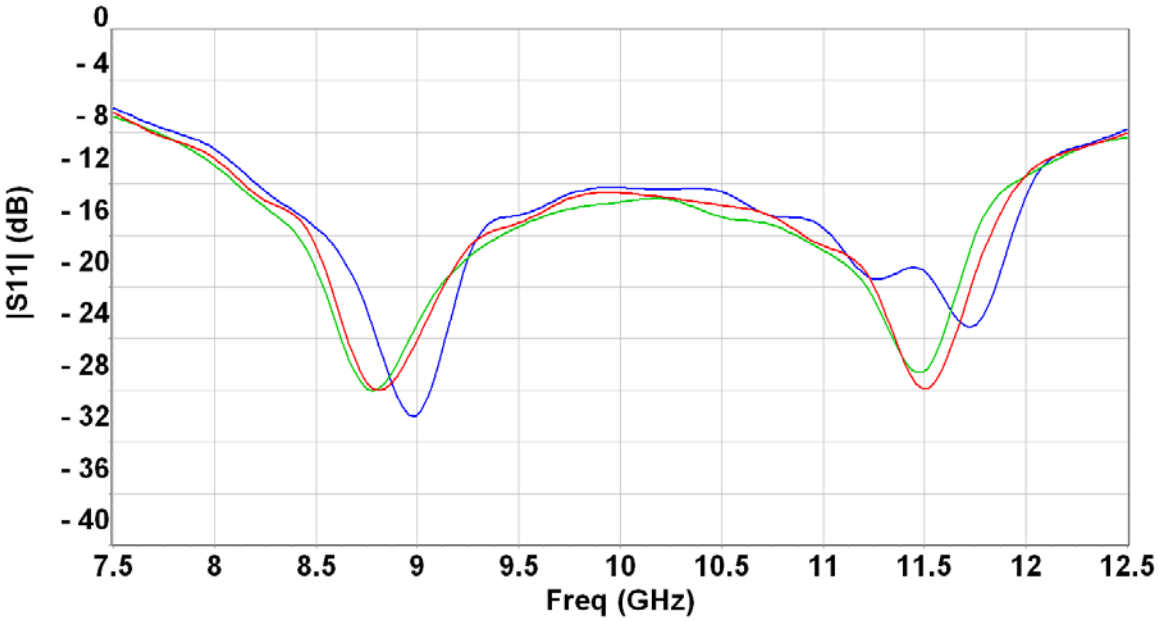
Typical Test Fixture Measurements: Small Signal Performances

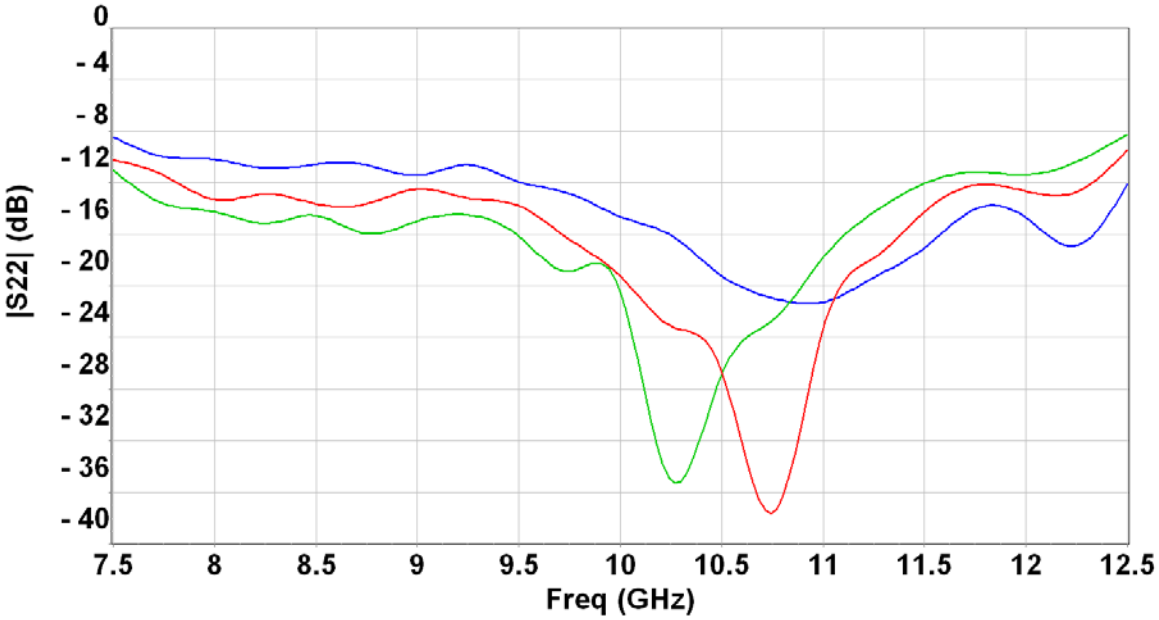
Tb.= +25°C/+85°C/ -40°C, Vd = +28V, Id = 840mA @25°C,
Pulse width = 25µs, Duty cycle = 10%

Input Return Loss versus Frequency



— -40°C — +25°C — +85°C

Output Return Loss versus Frequency



— -40°C — +25°C — +85°C

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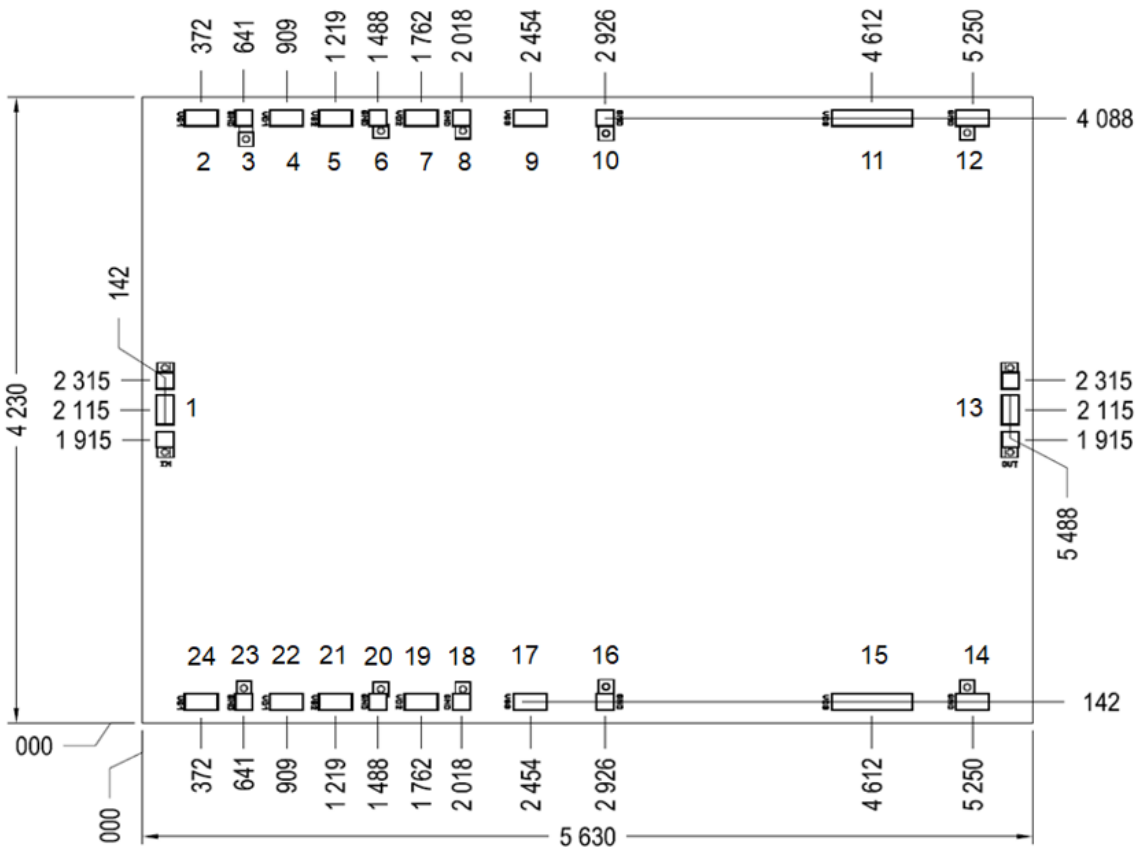
Mechanical data



Chip size = 5630x4230 ±50µm
Chip thickness = 100µm ±10µm

RF pads (1, 13) = 208 x 118µm²
DC pads (2, 4, 5, 7, 9, 17, 19, 21, 22, 24) = 218 x 118µm²
DC pads (11, 15) = 518 x 118µm²
Chip width and length are given with a tolerance of ±50µm

PAD Number	Name	Description
1	IN	Input RF port
3, 6, 8, 10, 12, 14, 16, 18, 20, 23	GND	Ground (NC)
2, 5, 21, 22	NC	Isolated pads (fabrication purpose), not to be used
24	VG1	Negative supply voltage (gate of stage 1)
24	VG2	Negative supply voltage (gate of stage 2)
9, 17	VG3	Negative supply voltage (gate of stage 3)
4	VD1	Positive supply voltage (drain of stage 1)
7, 19	VD2	Positive supply voltage (drain of stage 2)
11, 15	VD3	Positive supply voltage (drain of stage 3)
13	OUT	Output RF port

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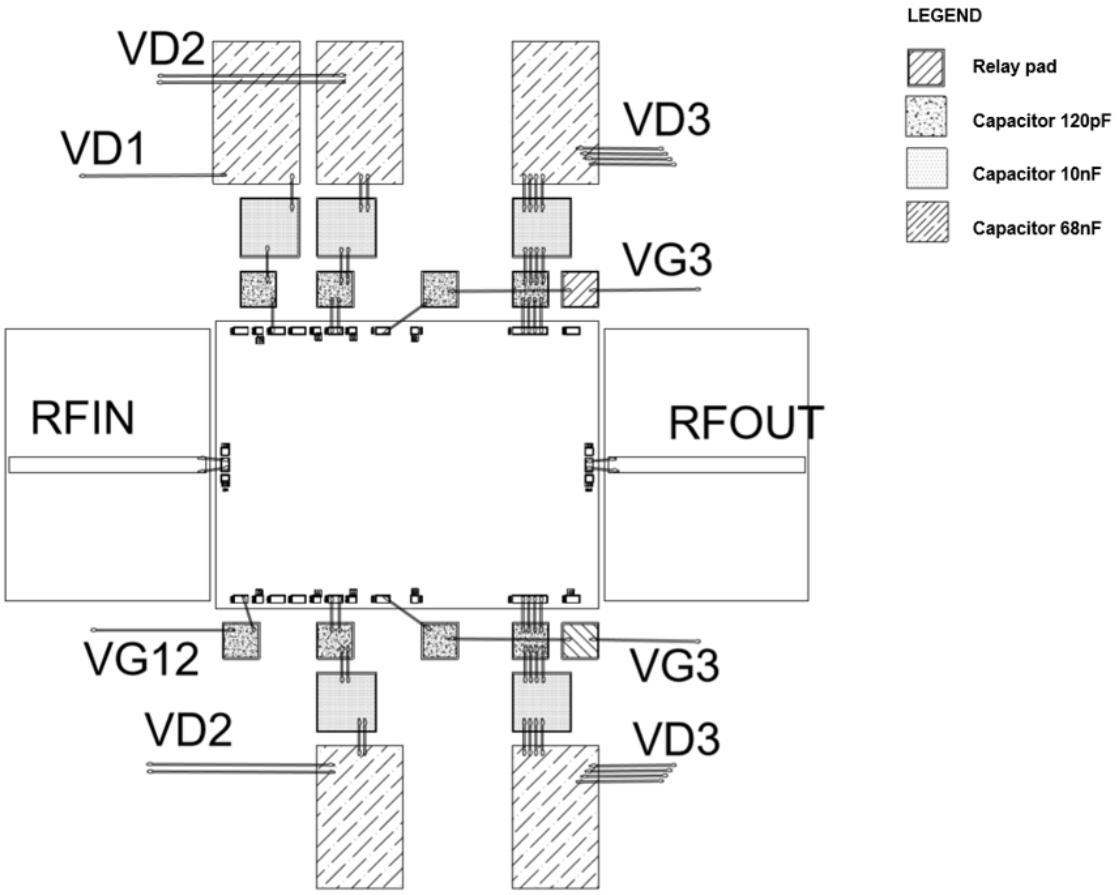
Recommended assembly plan



3 levels of decoupling capacitor have been used:
First level of capacitor is 120pF, second level is 10nF and third level is 68nF.

Note: Supply feed should be bypassed. 25µm diameter gold wire is to be preferred.
This biasing network proposed is compliant with a DC pulse applied on the gate.

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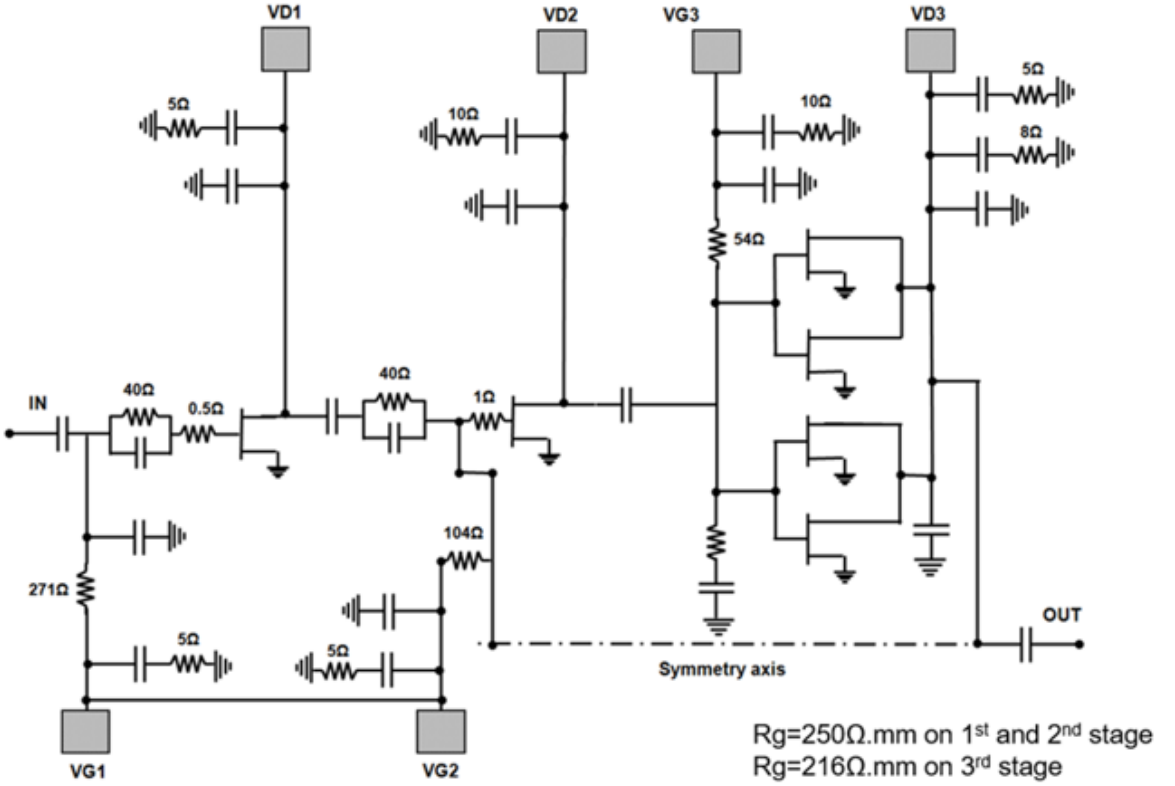
Simplified DC schematic



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Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Ordering Information

Chip form:	CHA8212-99F/00

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