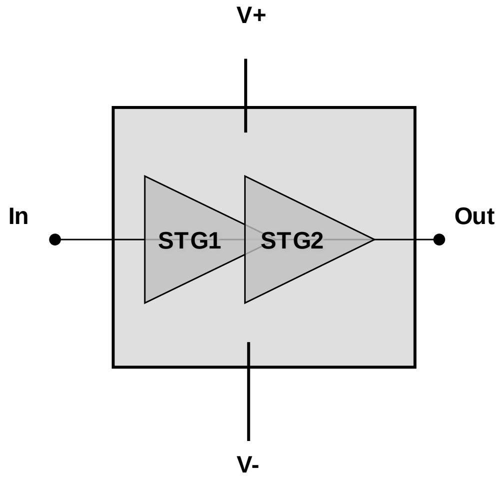
CHA8352-99F

20W Ku-Band High Power Amplifier

GaN Monolithic Microwave IC

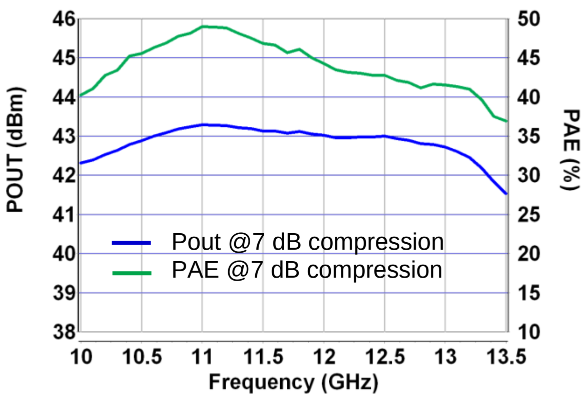
Description

The CHA8352-99F is a two-stage GaN High Power Amplifier in the frequency band 10.7-12.75GHz. This HPA typically provides 20W of output power associated to 45% of Power Added Efficiency. The small signal gain exhibits more than 25dB. The overall power supply is of 20V/0.5A (quiescent current).
This circuit is a very versatile amplifier for high performance systems.
The circuit is dedicated to space applications and well suited for a wide range of microwave applications and systems.
The part is developed on a robust 0.15µm gate length GaN on SiC HEMT process and is available as a bare die.



Main Features

- ■ 10.7-12.75 GHz frequency range
- ■ Linear Gain is 25 dB
- ■ 43dBm Pout for +23dBm input power
- ■ Associated PAE is more than 45% for +23dBm input power
- ■ Associated Id is 2.2A for +23dBm input power
- ■ DC bias: Vd=20Volts @Idq=0.5A
- ■ Chip size 5.3x3.5x0.07mm



Main Electrical Characteristics

Tb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	10.7		12.75	GHz
Gain	Linear Gain		25		dB
PAE	Power Added Efficiency (Pin=23 dBm)		45		%
Pout	Output Power (Pin=23 dBm)		43		dBm

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Specifications (CW mode)

Tb.= +25°C, Vd = +20V, Idq = 500mA,

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	10.7		12.75	GHz
Gain	Linear Gain		25		dB
Pout	Output Power (Pin = 23dBm)		43		dBm
PAE	Associated Power Added Efficiency (Pin = 23dBm)		45		%
Id	Associated current (Pin = 23dBm)		2.3		A
S11	Input Return Loss		18		dB
S22	Output Return Loss		17		dB
Idq	Quiescent Current		0.5		A
Vd	Drain Voltage		20		V
Vg	Gate Voltage		-2.9		V

These values are representative of measurements done in test fixture with a bonding wire of typically 0.25 to 0.3nH.

Recommended Operating Ratings

Tb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	20V	V
Id_stg1	1st stage drain current (North and South)	0.66	A
Id_stg2	2nd stage drain current (North and South)	2.9	A
Pin	Maximum peak input power overdrive	25	dBm
Tj	Maximum Junction temperature (1)	200	°C

(1) value provided for Tb=85°C

Absolute Maximum Ratings (2)

Tb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	27	V
Id_stg1	1st stage drain current (North and South)	0.9	A
Id_stg2	2nd stage drain current (North and South)	3.6	A
Pin	Maximum peak input power overdrive	28	dBm

(2) Operation of this device above anyone of these parameters may cause permanent damage.

Temperature Range

Tb	Operating temperature range (chip backside temperature reference)	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

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Typical Bias Conditions

Tb.= +25°C

Symbol	Pad Nº	Parameter	Values	Unit
VG1	2, 18	Gate voltage tuned for Idq ~ 0.84A	-2.9	V
VG2	6, 14			
VD	4, 8, 12, 16	Drain Voltage	20	V

"Power ON" sequence

1. Bias HPA gate voltage at Vg close to Vpinch-off (example: Vg ≈ -5V).
2. Apply Vd bias voltage (Example: Vd = 20V).
3. Increase slowly Vgs up to quiescent bias drain current Ids0 (applied on the gate: 500mA).
4. Apply RF signal

"Power OFF" sequence

1. Turn off RF signal
2. Bias HPA gate voltage at Vg close to Vpinch-off (example: Vg ≈ -5V)
3. Set Vd to 0V.
4. Turn off Vd supply.
5. Turn off Vg supply.

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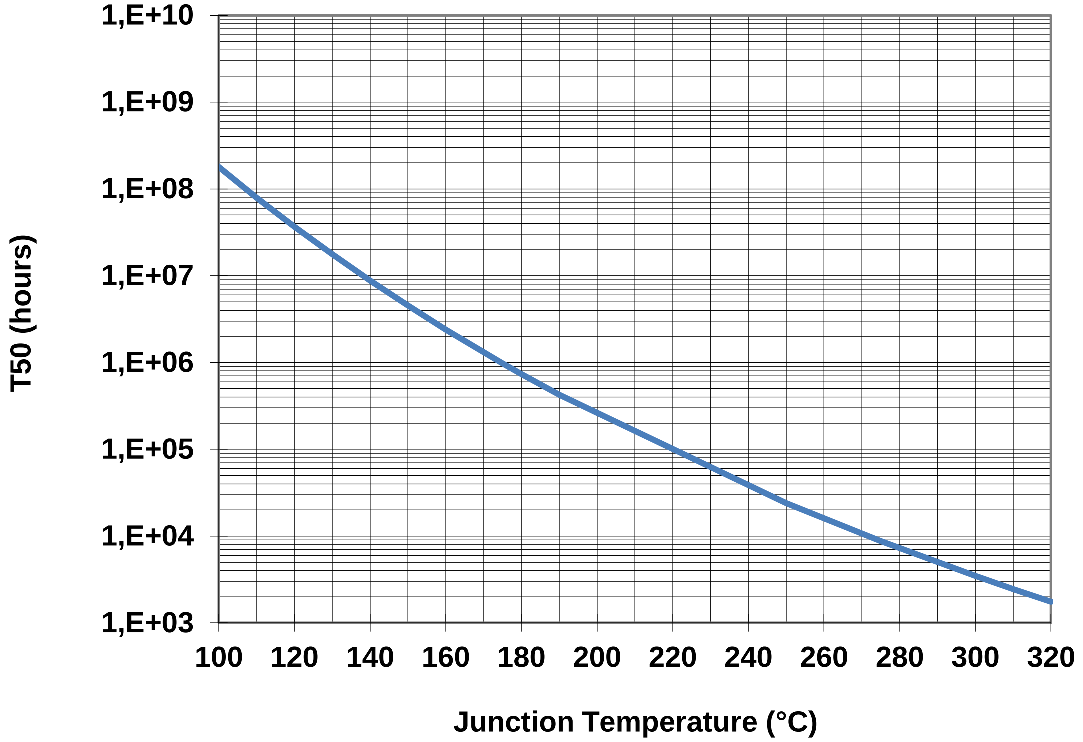
Device thermal information

The device thermal performances below are based on UMS rules to evaluate the junction temperature.
This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHA8352-99F is manufactured (GaN HEMT 0.15µm).
The temperature Tb_{chip} is defined as the chip backside temperature. The thermal resistance (Rth_eq) is given for the full circuit, and assumes CW mode is given in the table.

Thermal Resistance[1]	Rth_eq	Tb_{chip} = 85°C, Vd = 20V, Id_drive = 2.2A Pin = 27dBm, Pout = 42.5dBm Pdiss = 26.7W CW	1.98	°C/W
Junction Temperature	Tj		138	°C
Median Life	T50		1E07	Hrs

[1] Thermal resistance measured at the back of the chip

Median Life Time versus Junction Temperature



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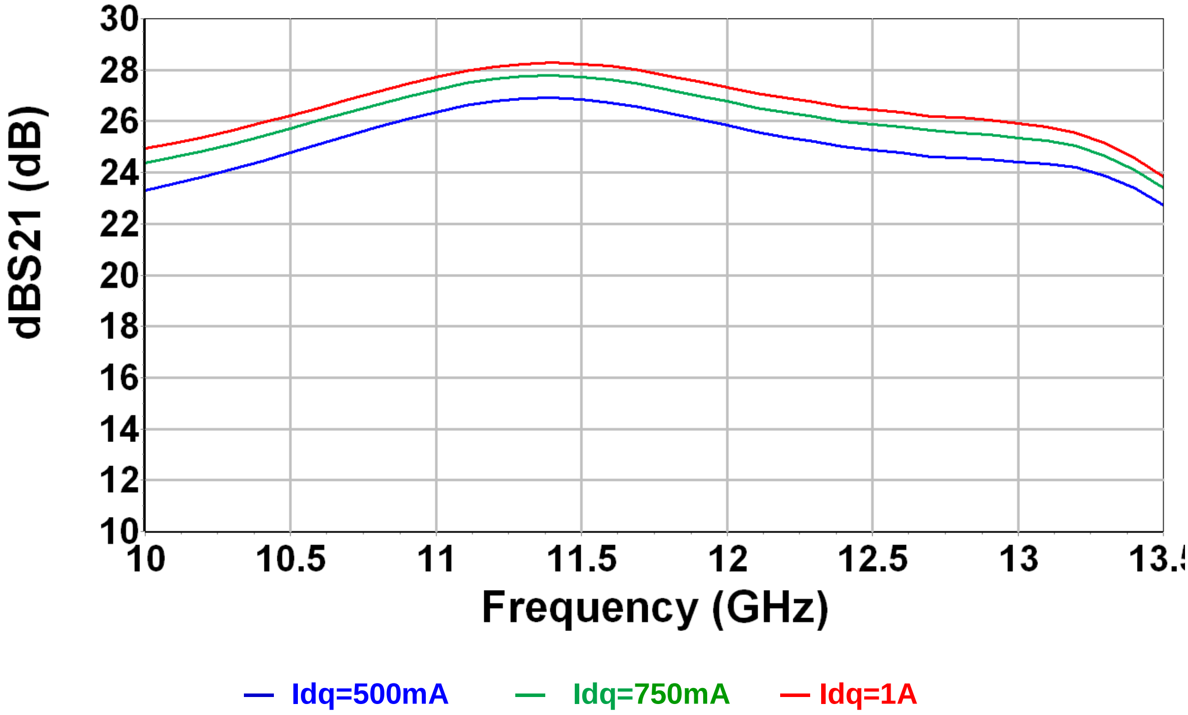
Typical Test Fixture Measurements: Small Signal Performances

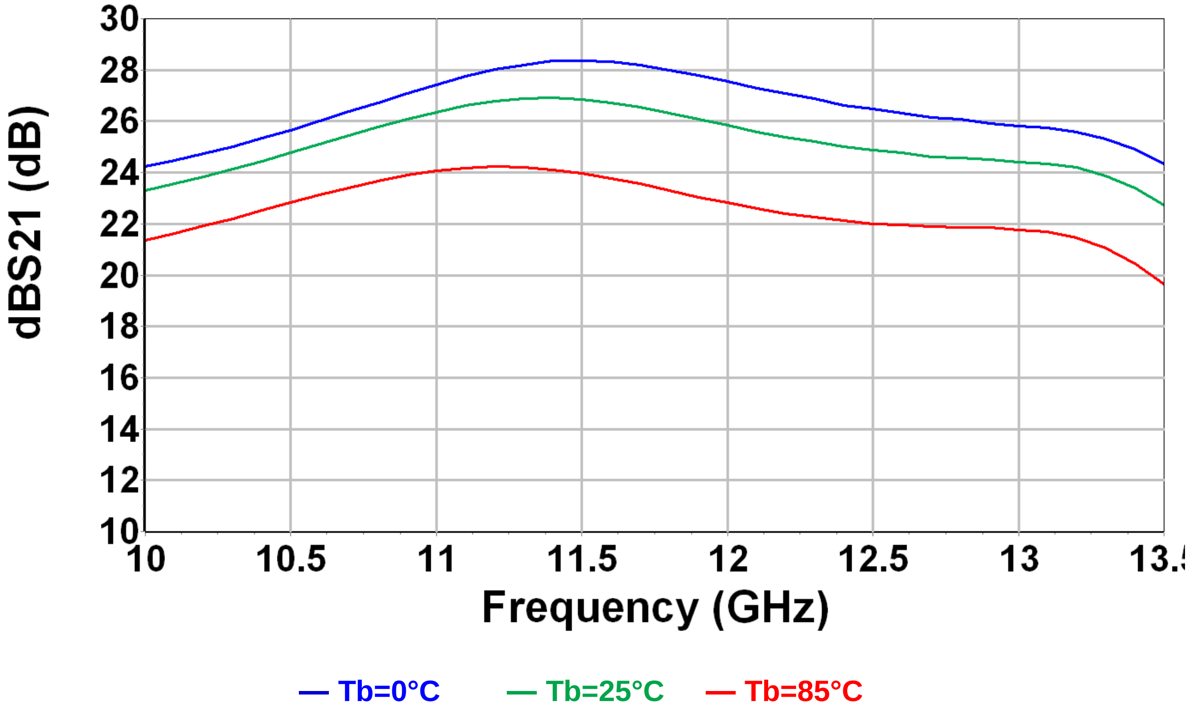
CW measurements: Tb.= 25°C, Vd = +20V

Linear Gain versus Frequency



Tb= +25°C/+85°C/ 0°C , Vd = +20V, Idq = 500mA (kept constant versus temperature)

Linear Gain versus Frequency



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Typical Test Fixture Measurements: Small Signal Performances

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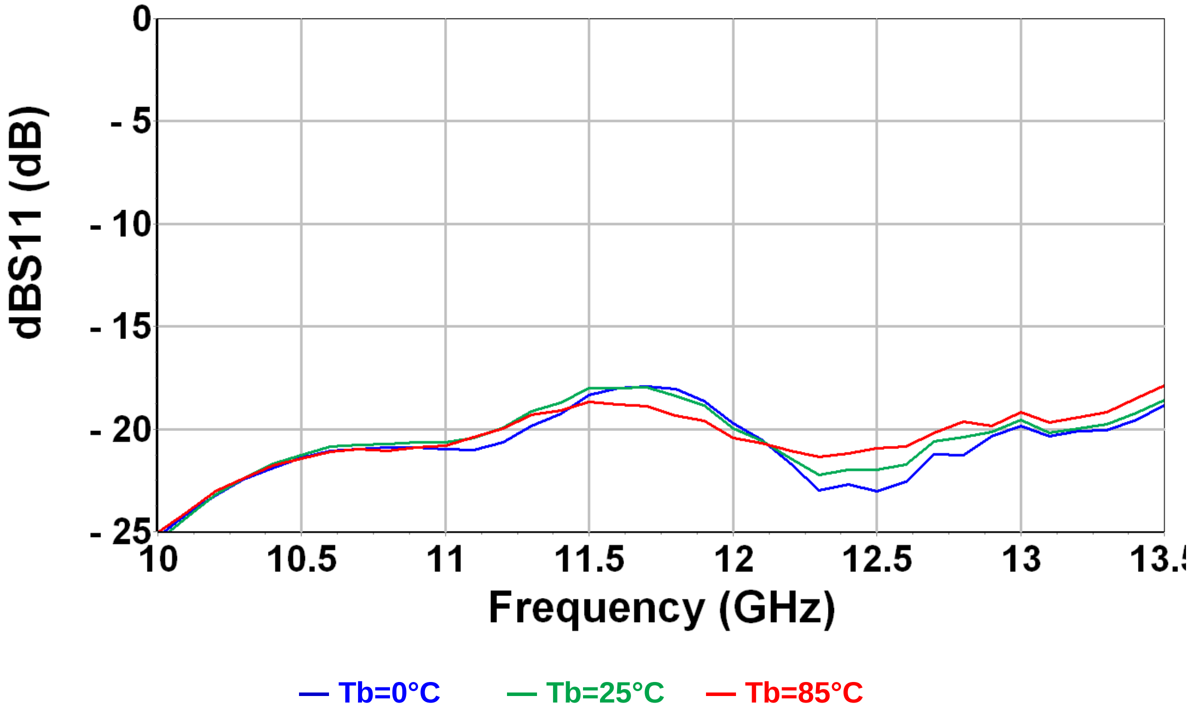
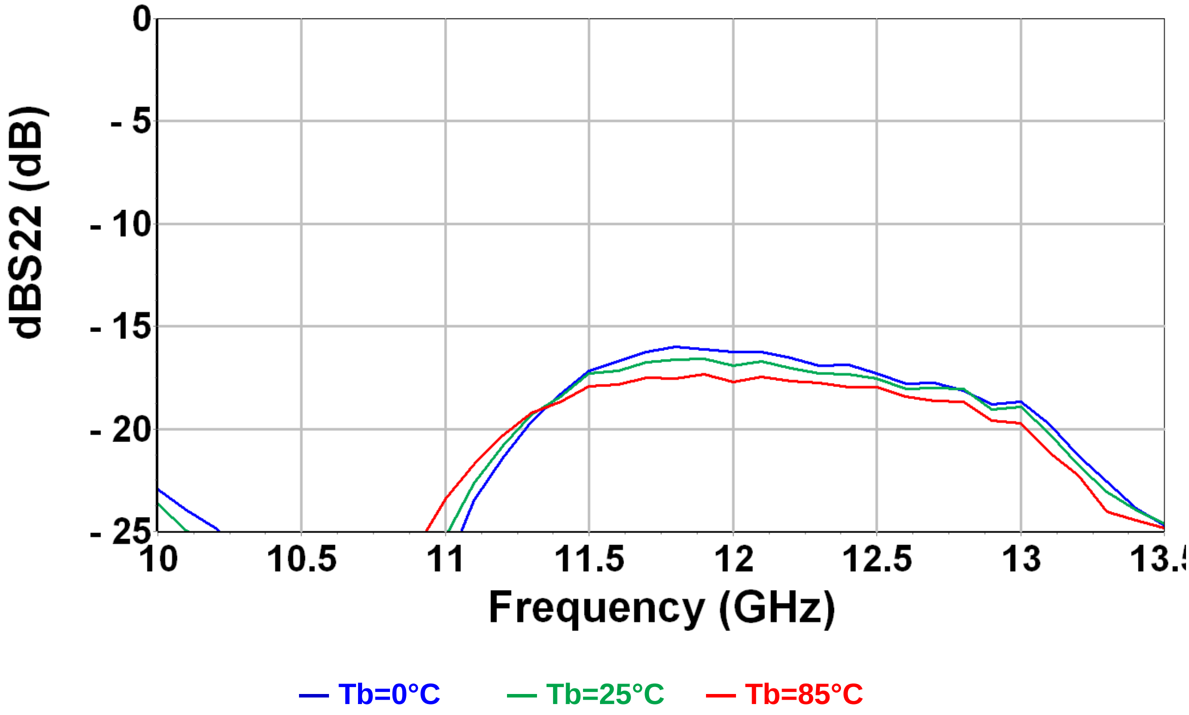
Input Return Loss versus Frequency



Output Return Loss versus Frequency



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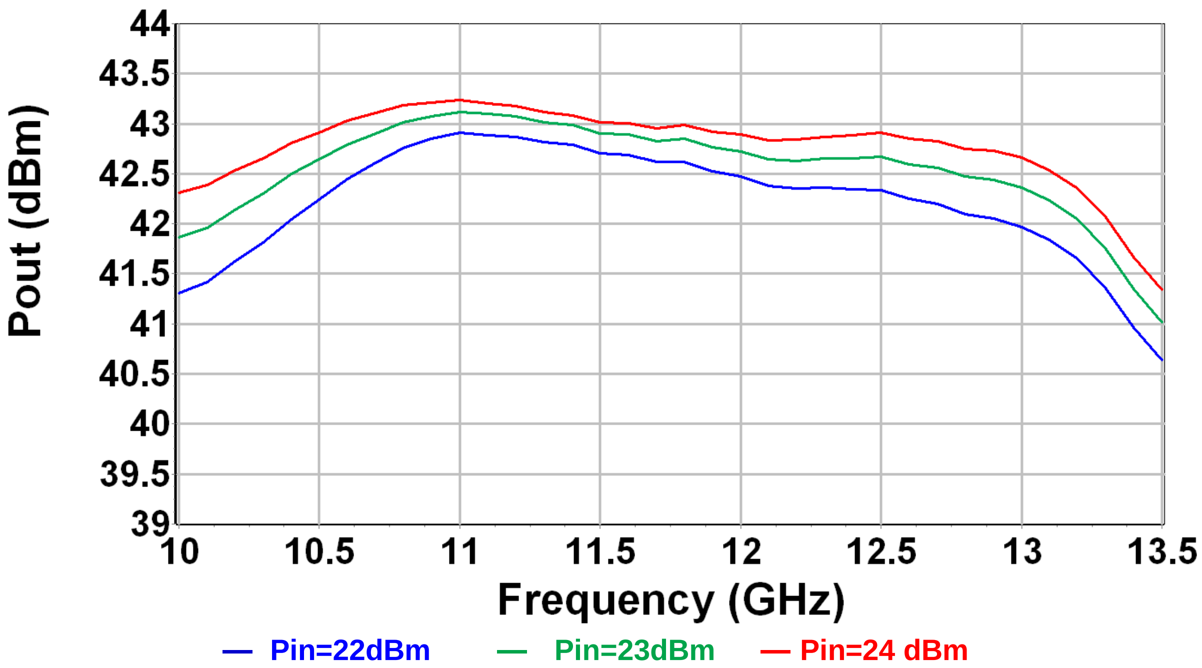
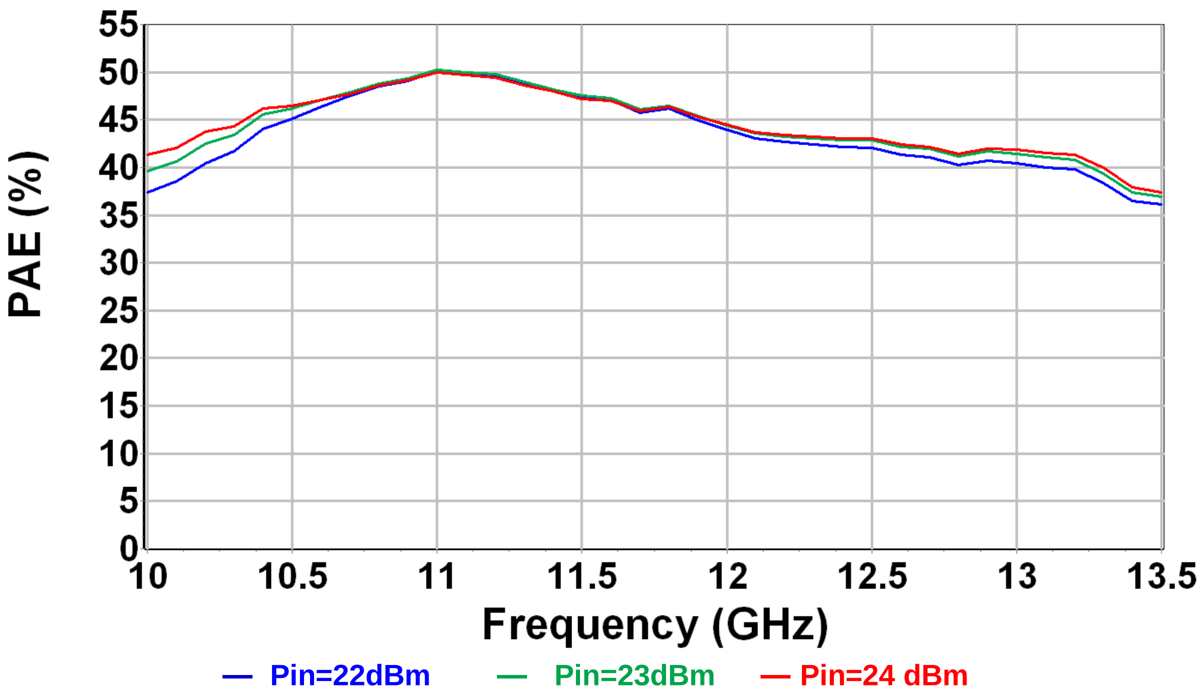
Typical Test Fixture Measurements: Non-linear performances

CW measurements: Tb=+25°C, Vd = +20V, Idq = 500mA

Output Power versus Frequency



Power Added Efficiency versus Frequency



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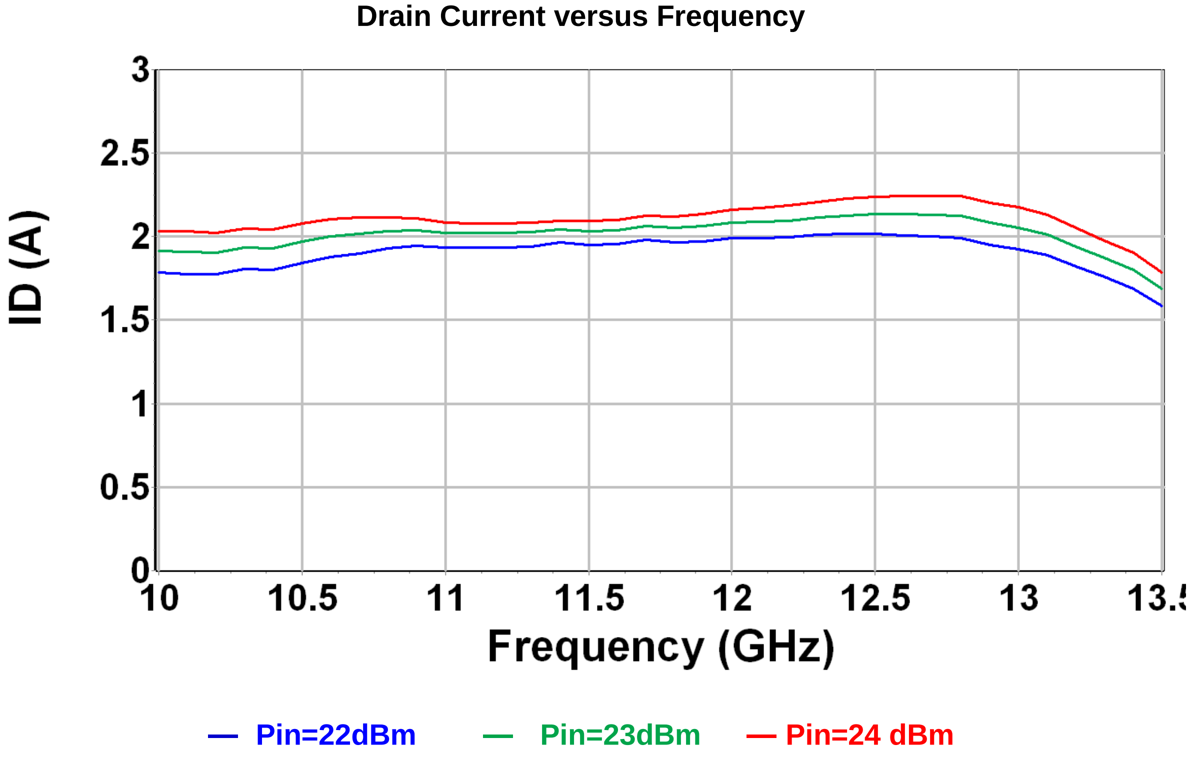

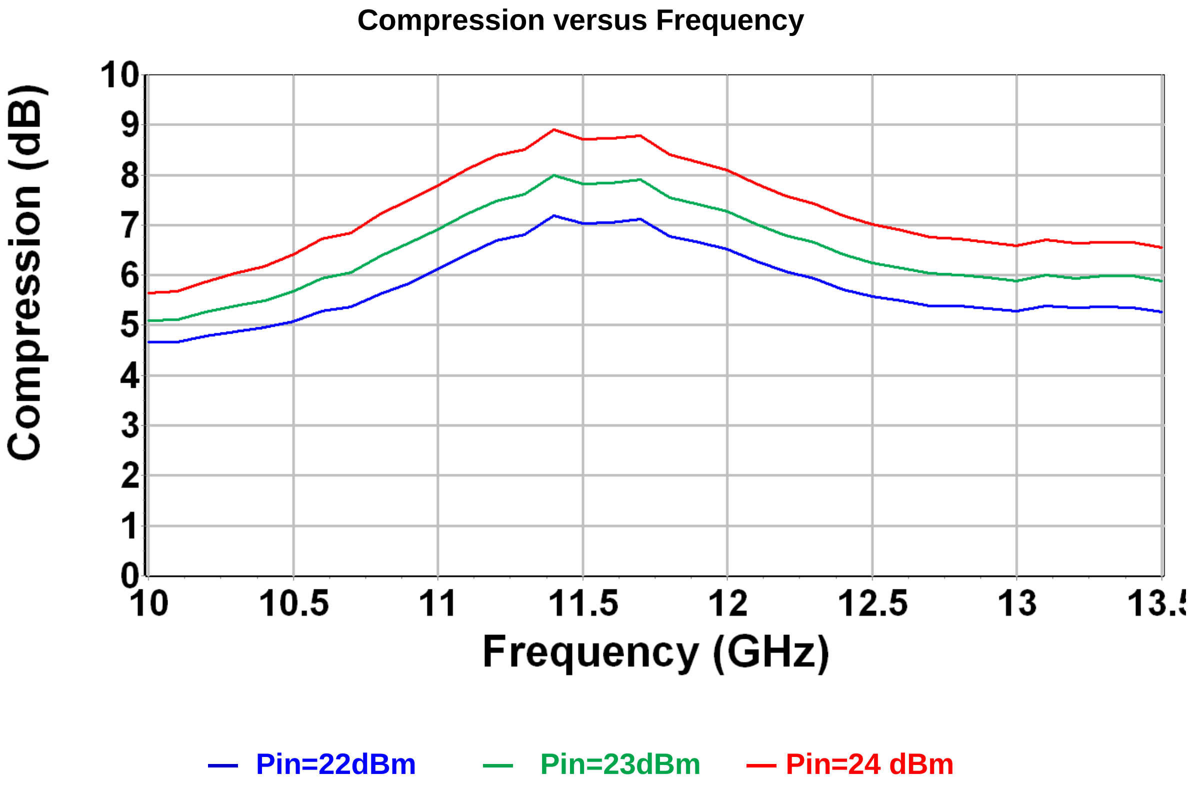

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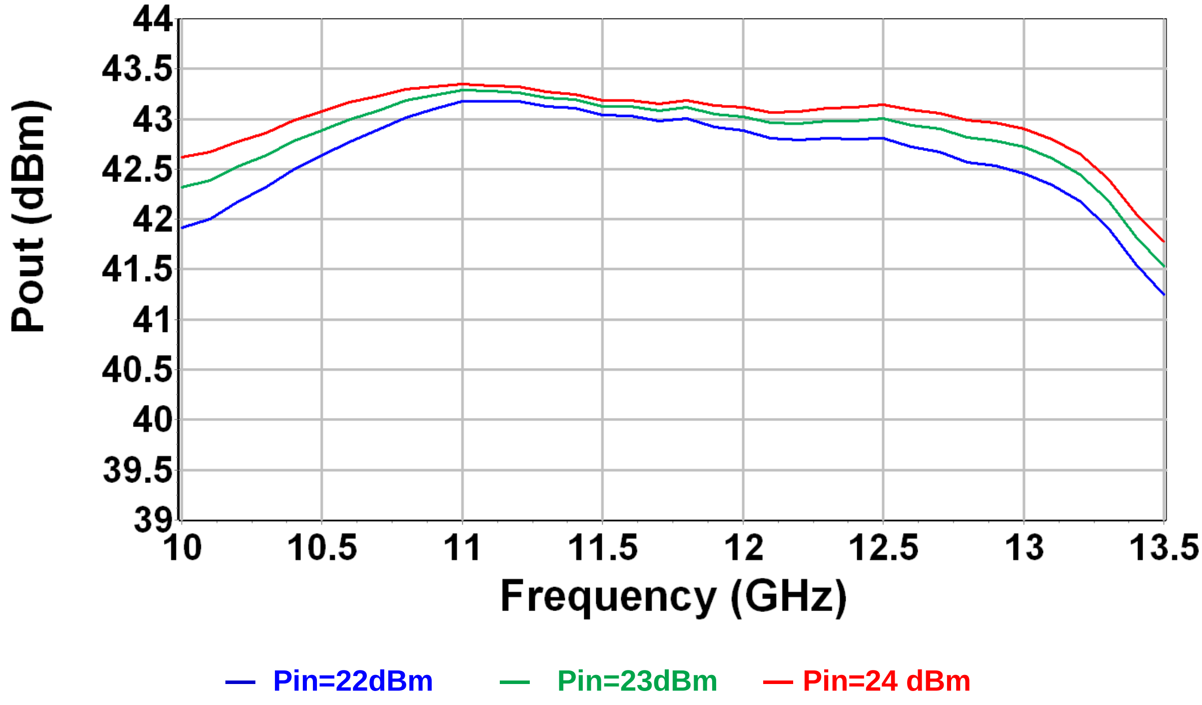
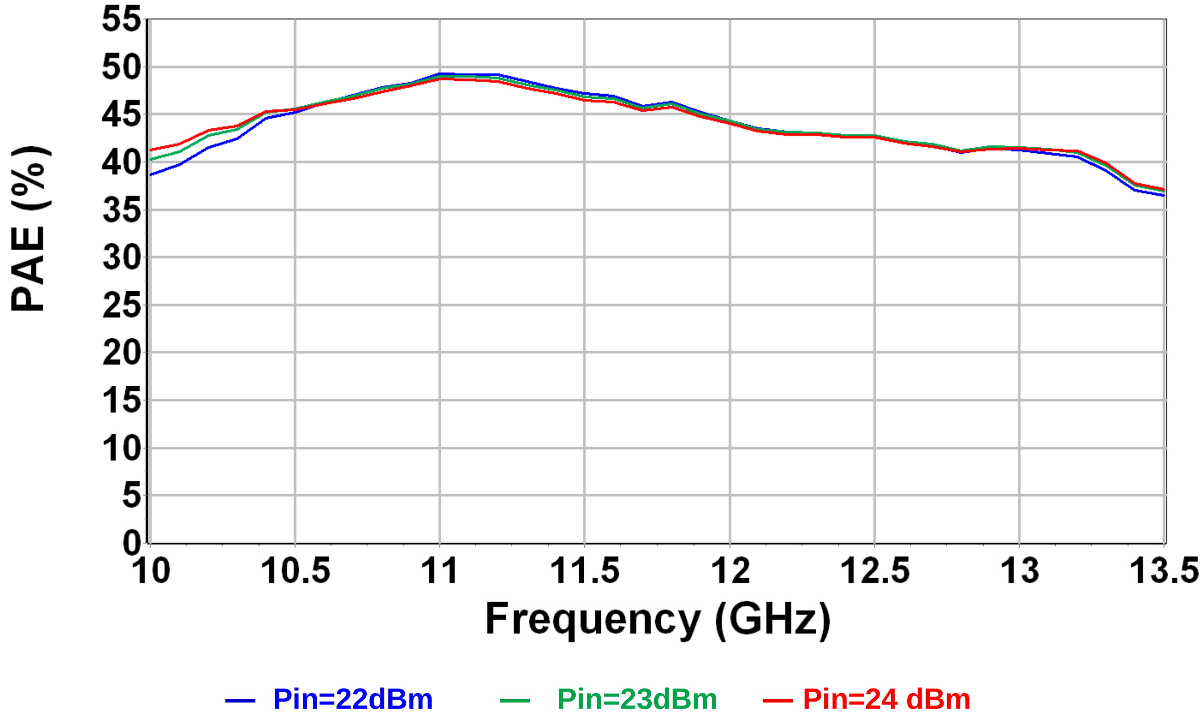
Typical Test Fixture Measurements: Non-linear performances

CW measurements: Tb=+25°C, Vd = +20V, Idq = 1000mA,

Output Power versus Frequency



Power Added Efficiency versus Frequency



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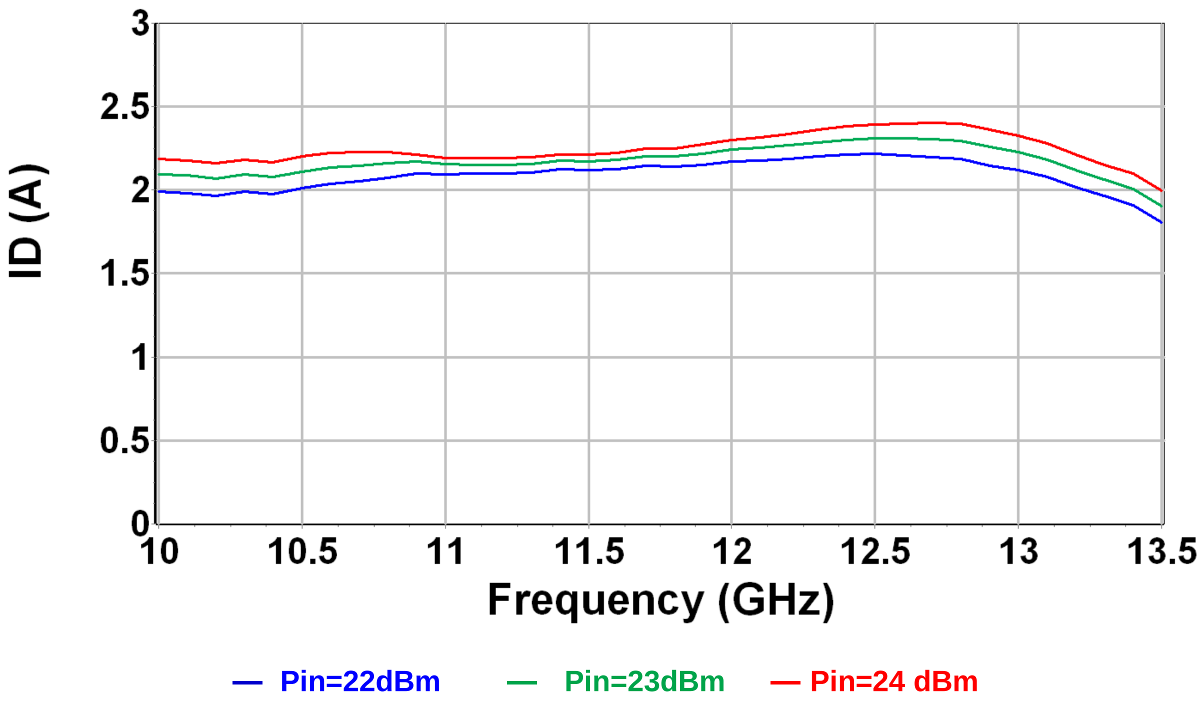
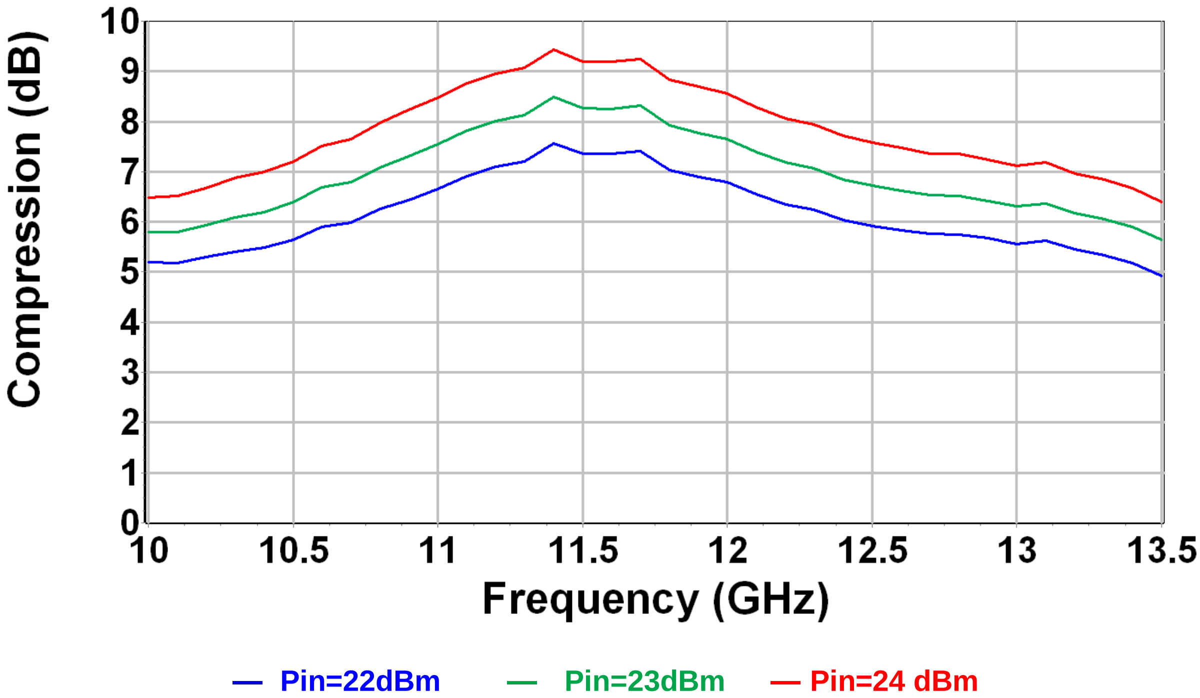
Drain Current versus Frequency



Compression versus Frequency



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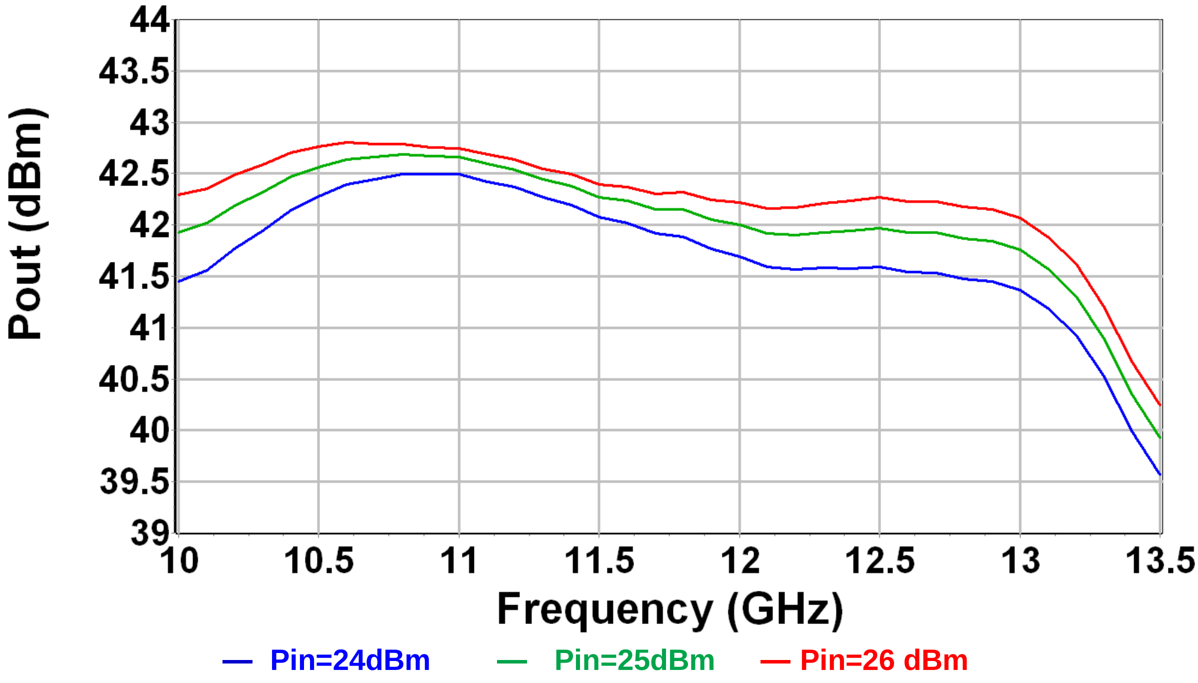
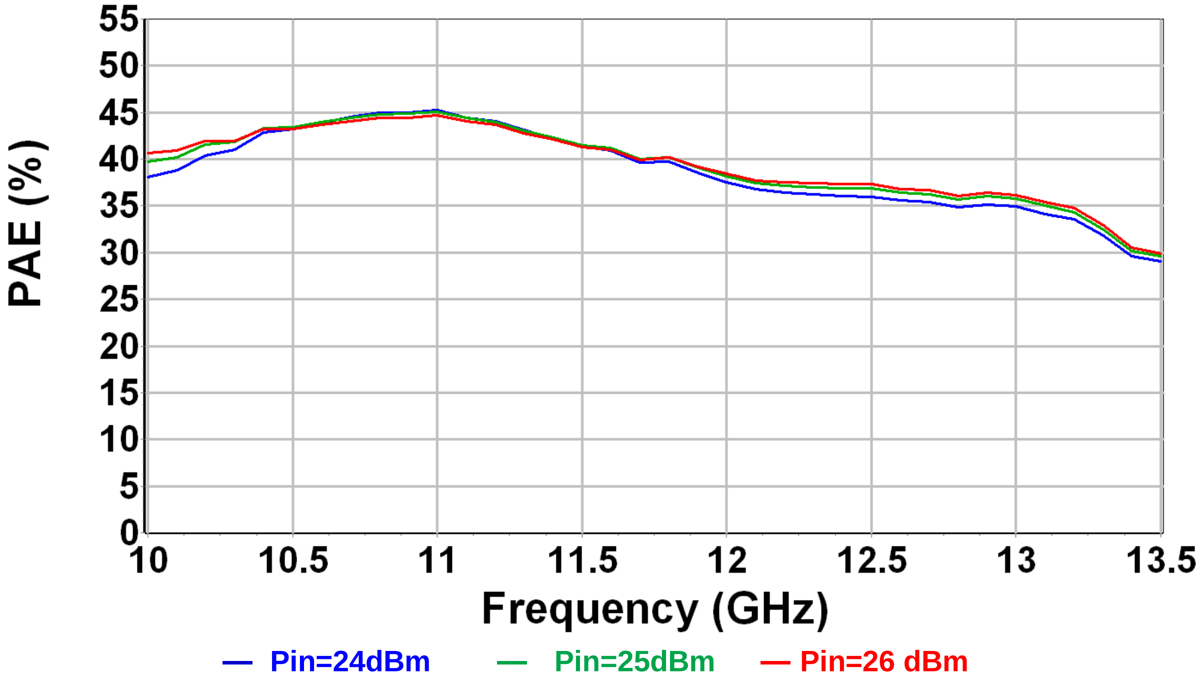
Typical Test Fixture Measurements: Non-linear performances

CW measurements: Tb=+85°C, Vd = +20V, Idq = 500mA

Output Power versus Frequency



Power Added Efficiency versus Frequency



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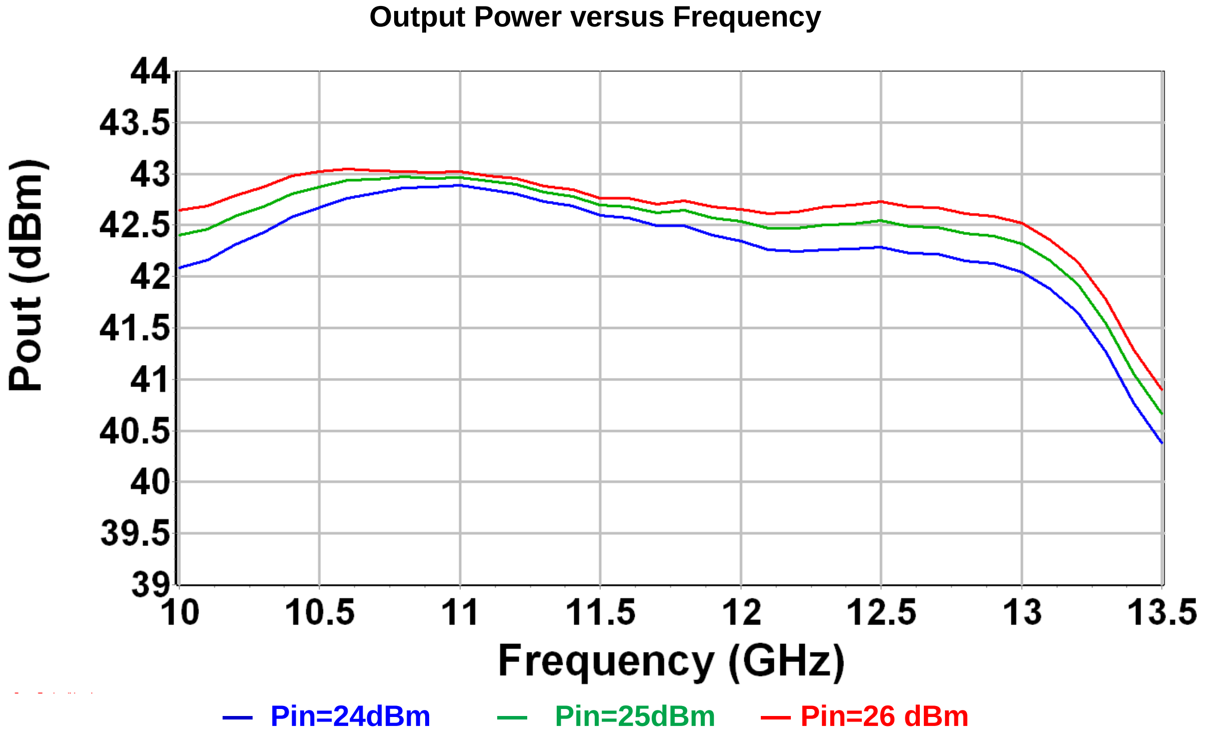

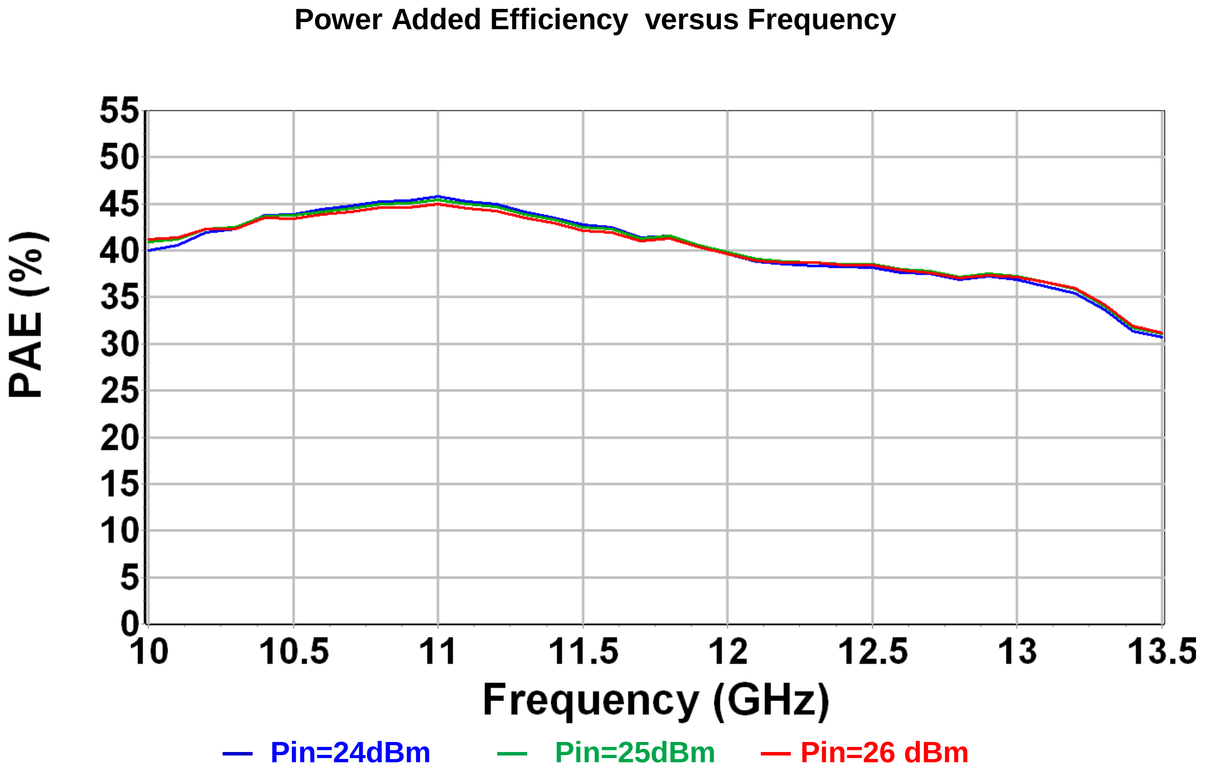

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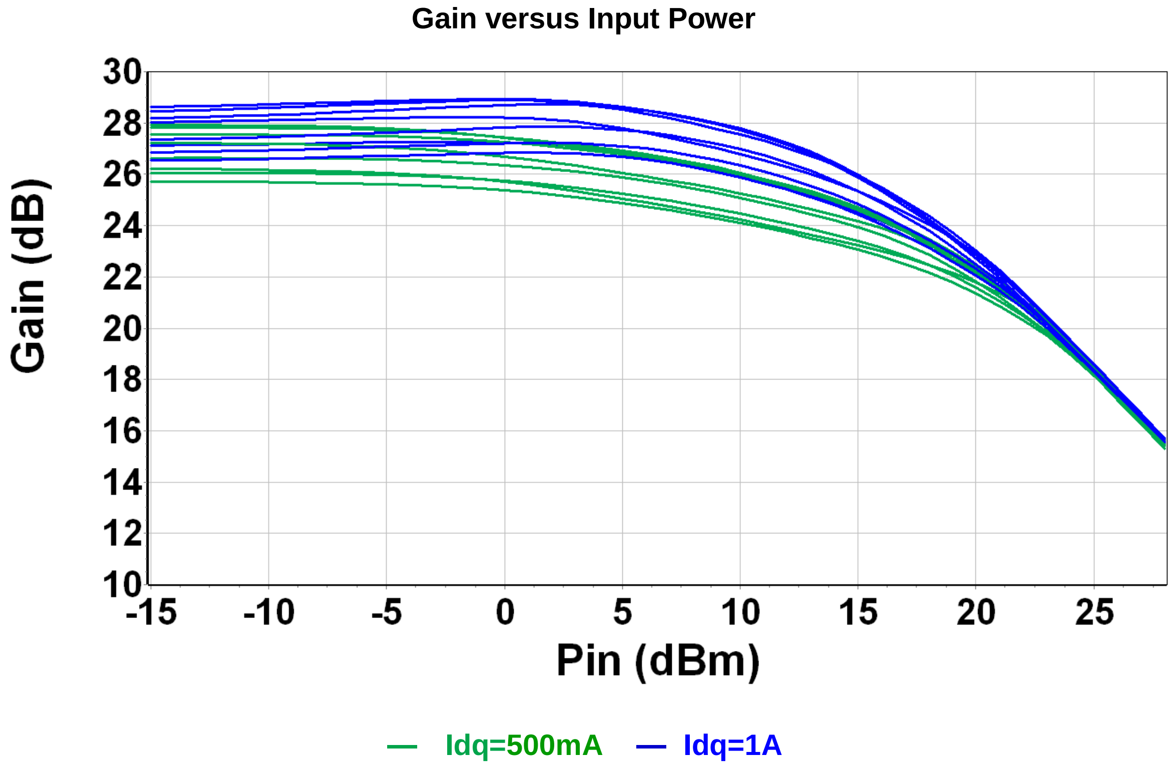
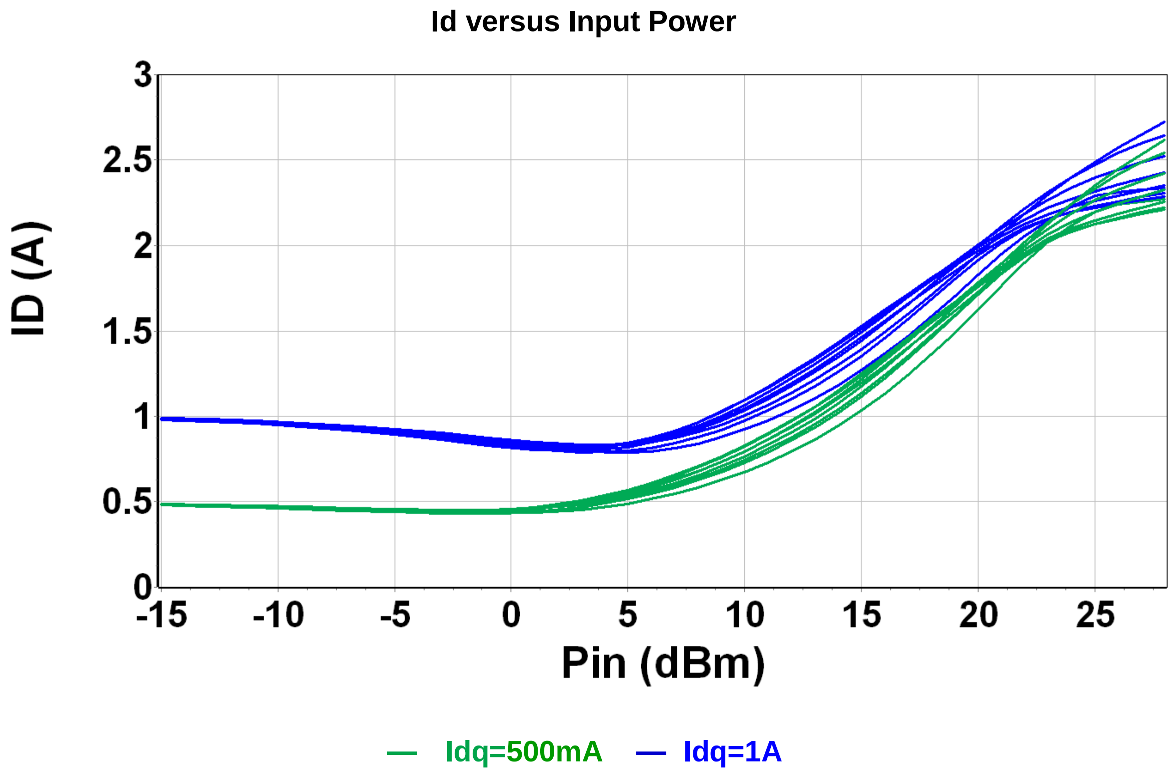
Typical Test Fixture Measurements: Non-linear Performances

CW measurements: Tb.= 25°C, Vd = +20V, Pin range : -15 to 28 dBm
Frequency range: 10.7-12.8 GHz step 0.3 GHz





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Typical Test Fixture Measurements: Non-linear Performances

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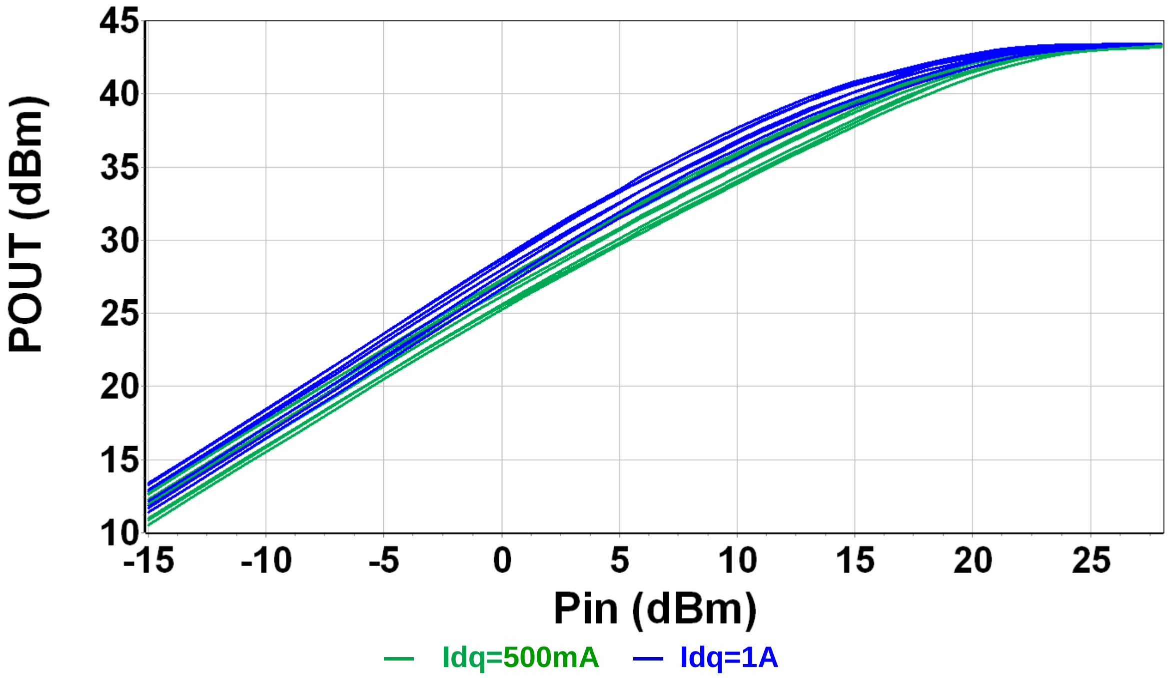
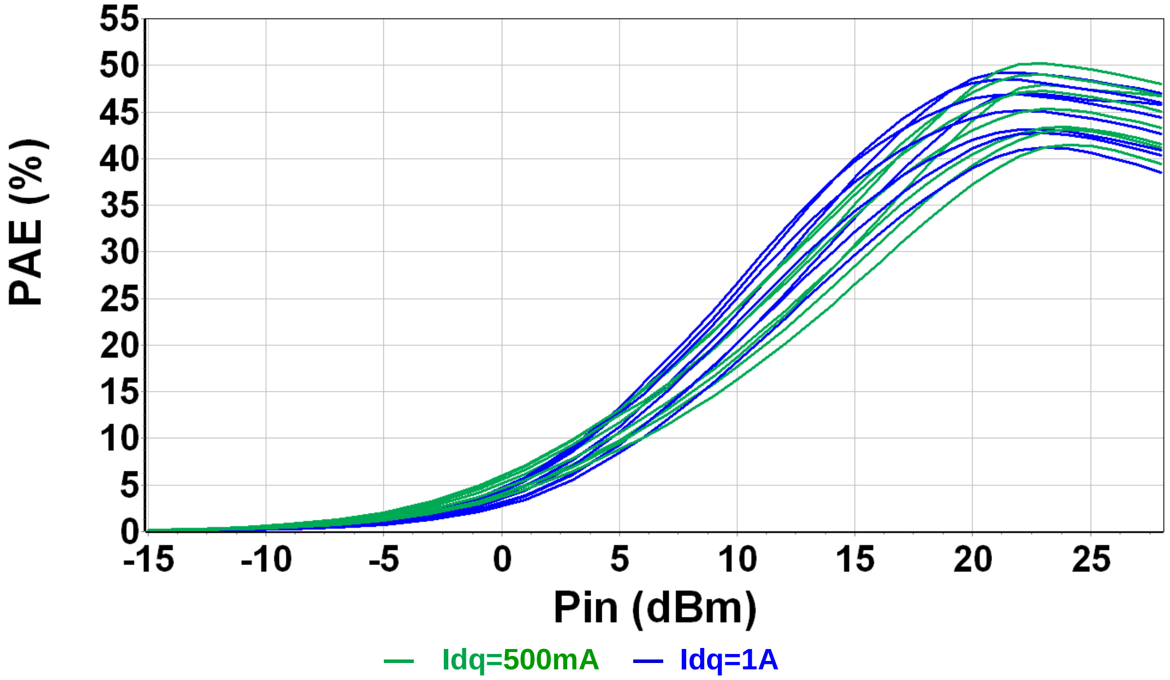
Pout versus Input Power



PAE versus Input Power



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Typical Test Fixture Measurements: Non-linear Performances

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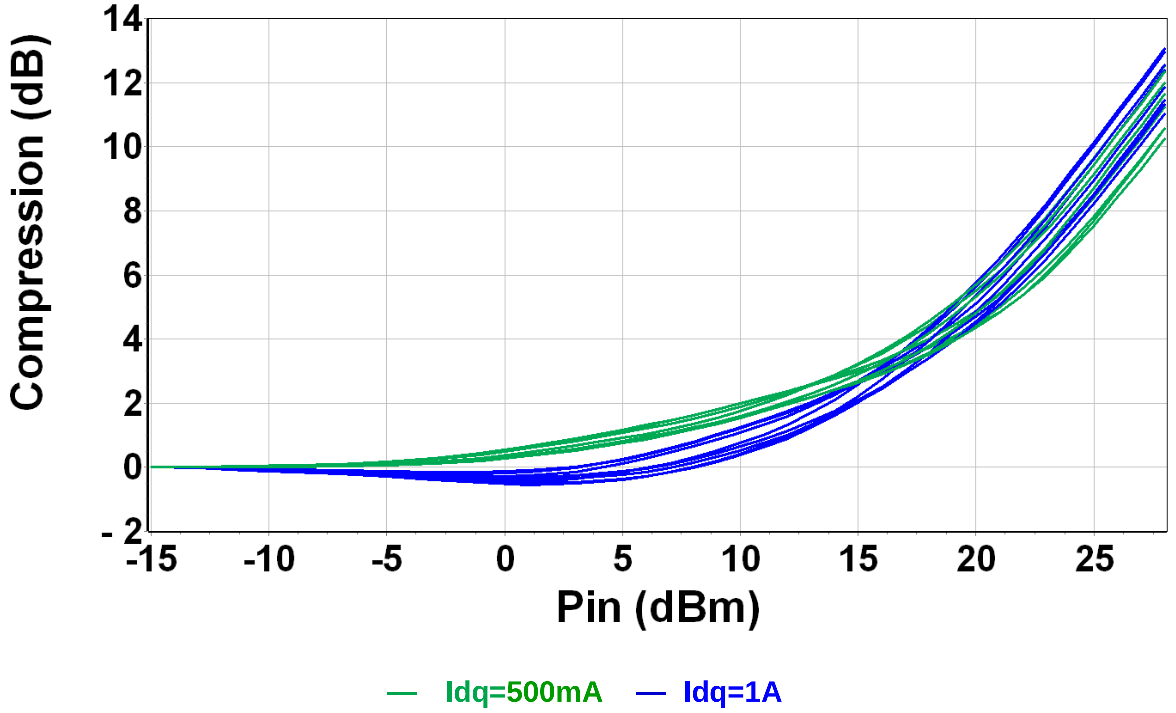
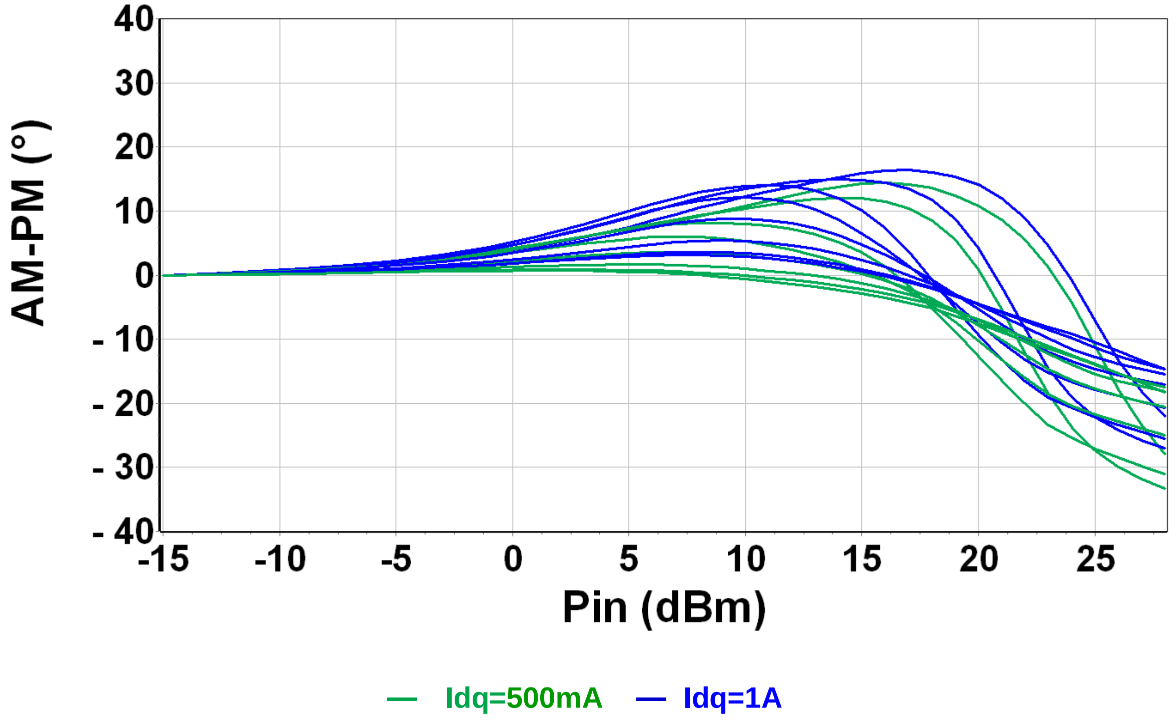
AM-AM versus Input Power



AM-PM versus Input Power



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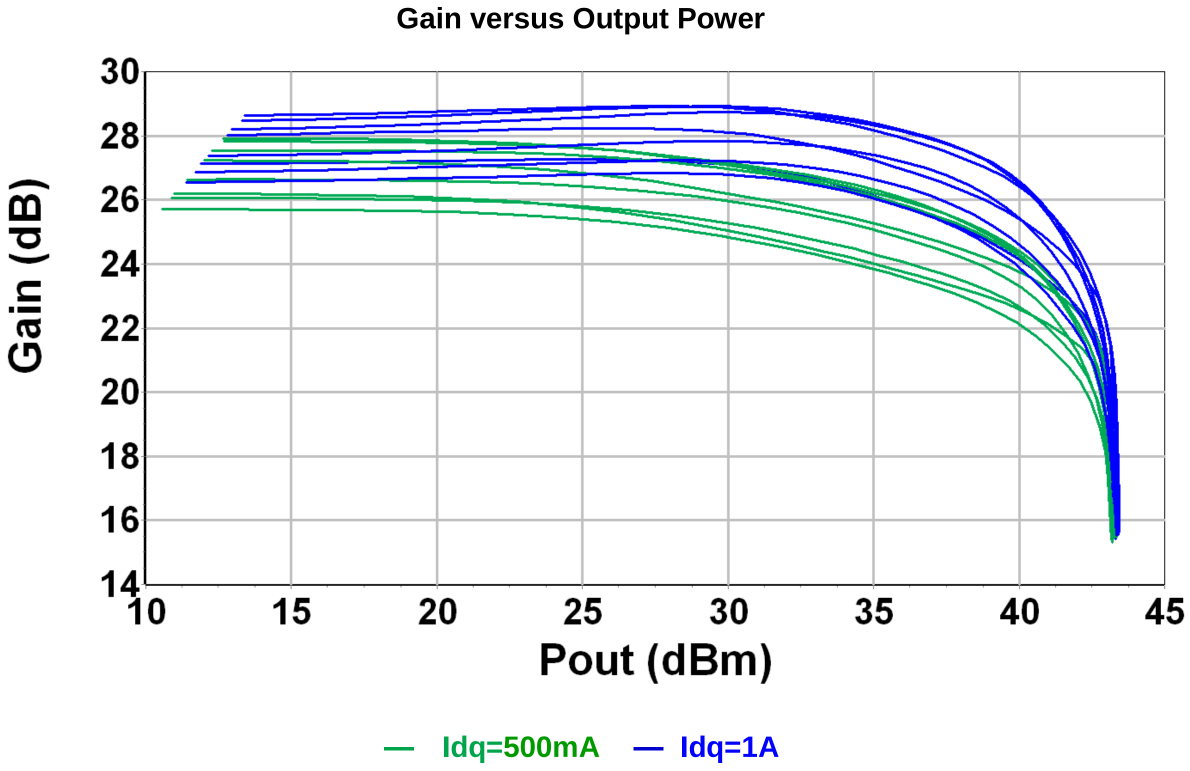

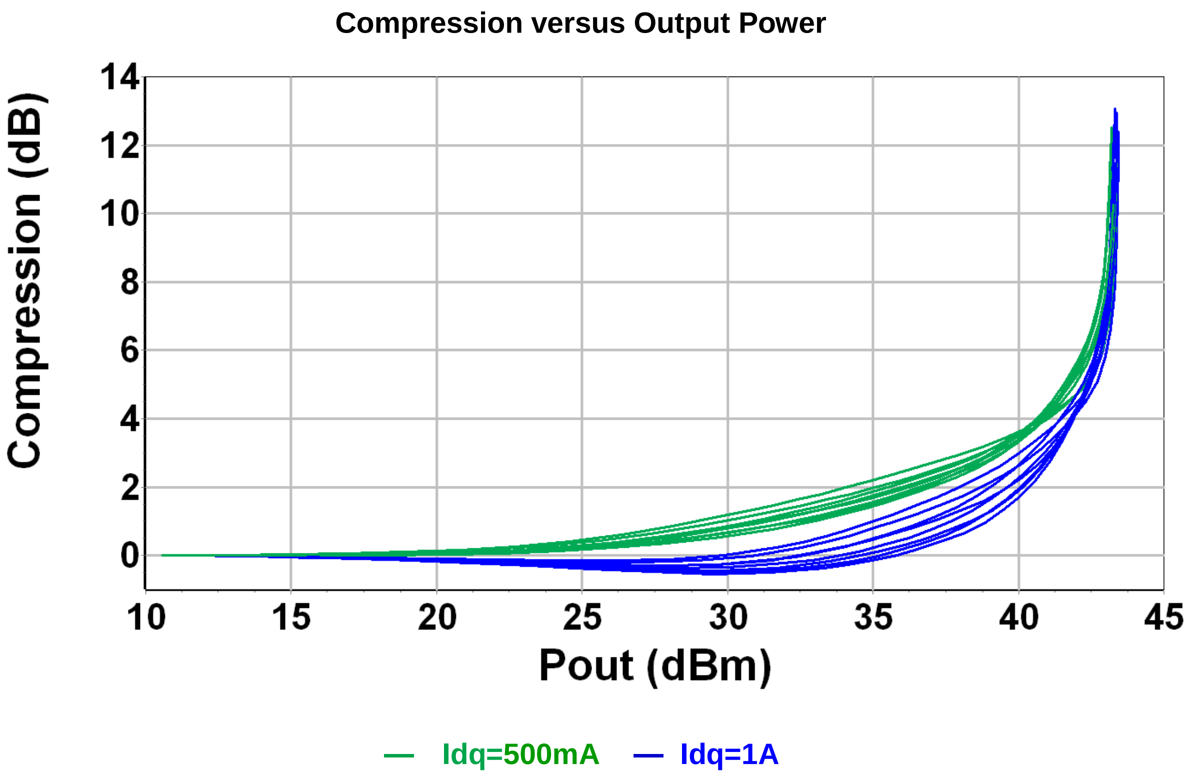

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Typical Test Fixture Measurements: Non-linear Performances

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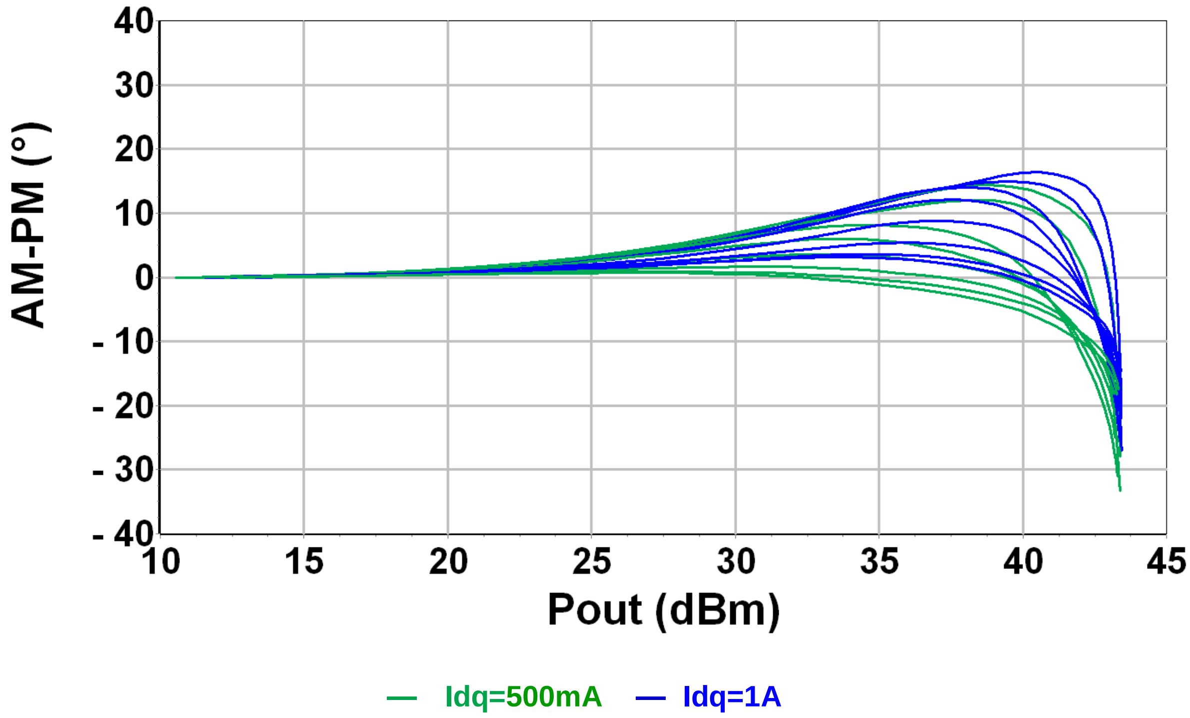
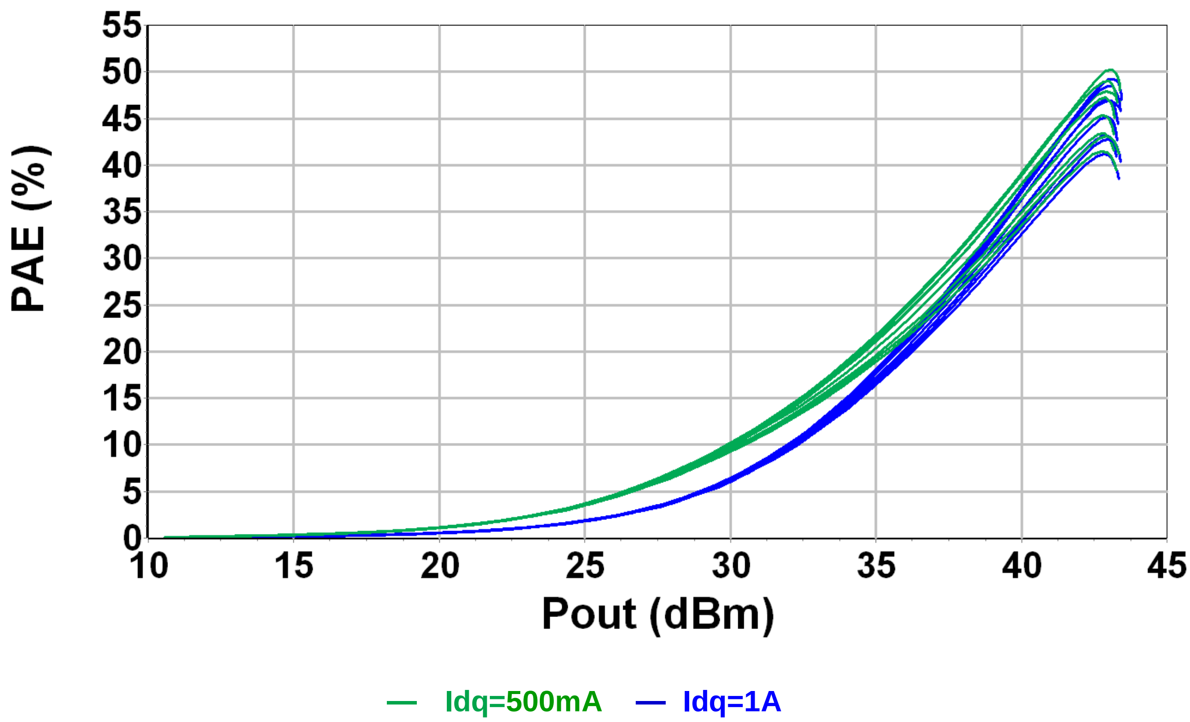
AM-PM conversion versus Output Power



Power Added Efficiency versus Output Power



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Typical Test Fixture Measurements: Non-linear Performances

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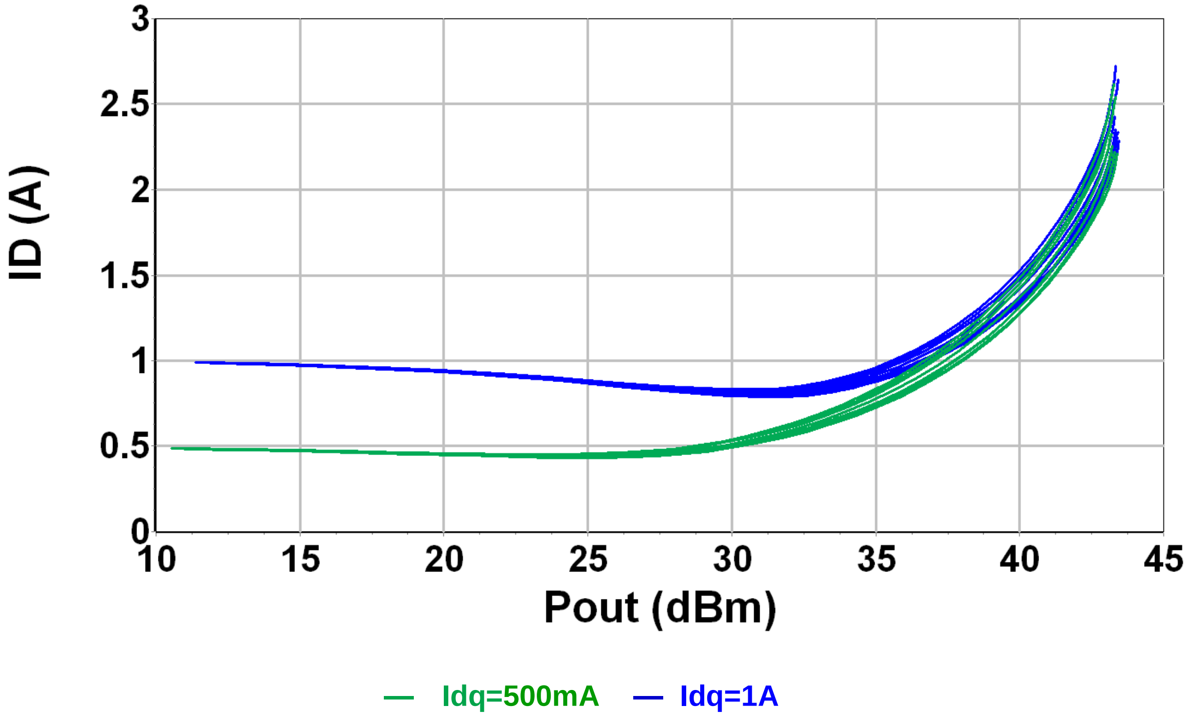
Drain current versus Output Power



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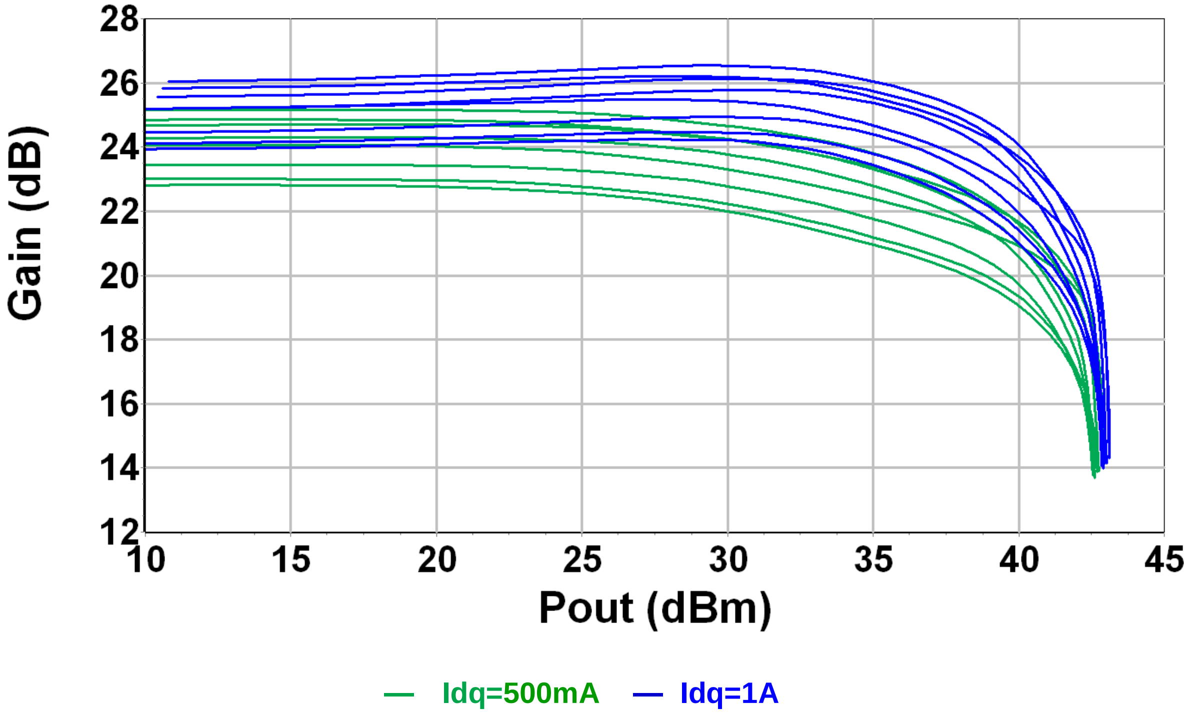
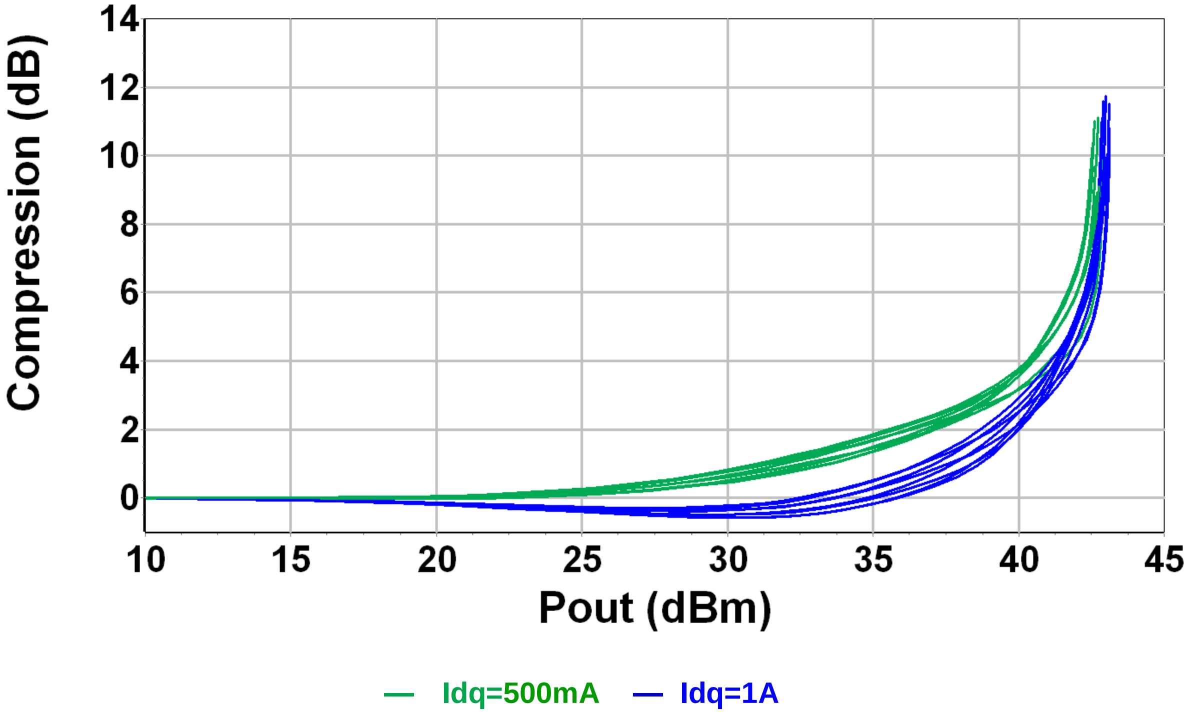
Typical Test Fixture Measurements: Non-linear Performances

CW measurements: Tb.= 85°C, Vd = +20V
Frequency range: 10.7-12.8 GHz step 0.3 GHz

Gain versus Output Power



Compression versus Output Power



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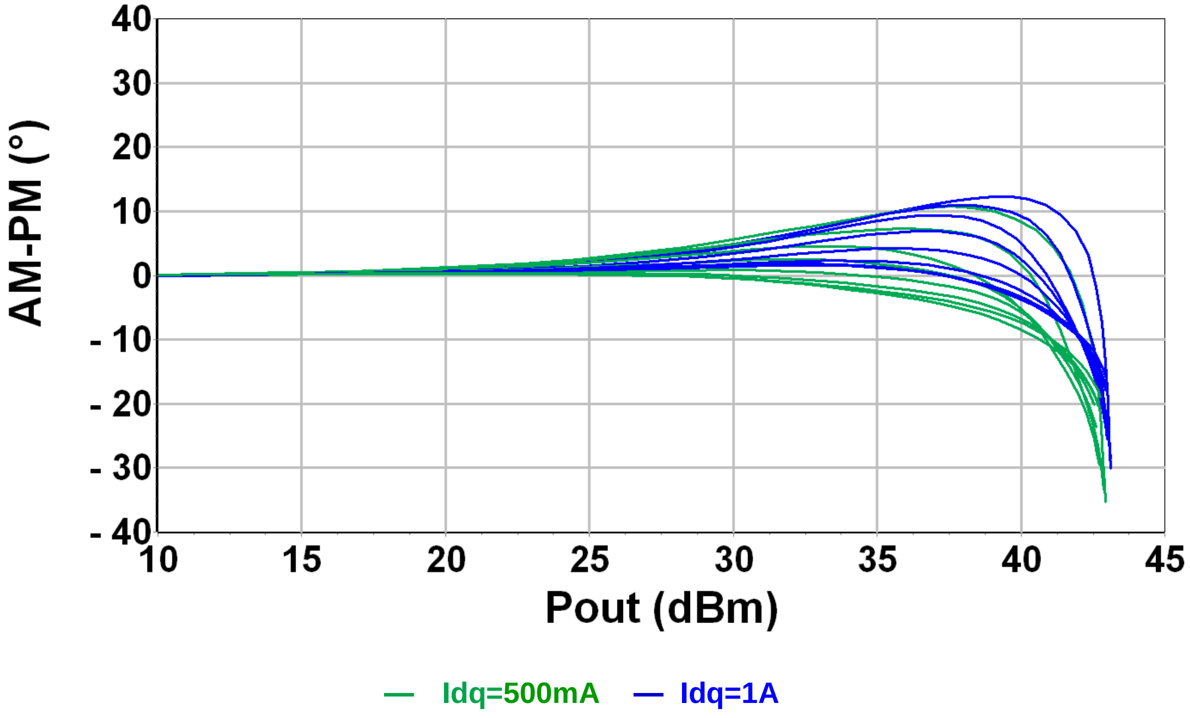
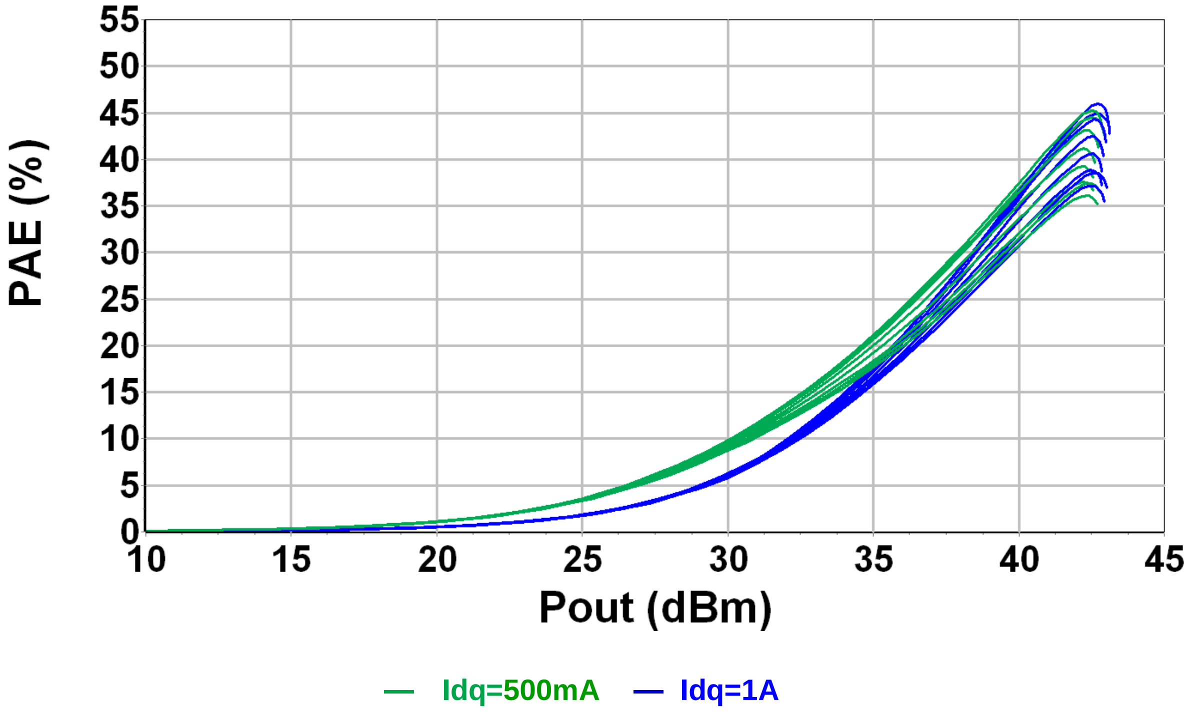
AM-PM conversion versus Output Power



Power Added Efficiency versus Output Power



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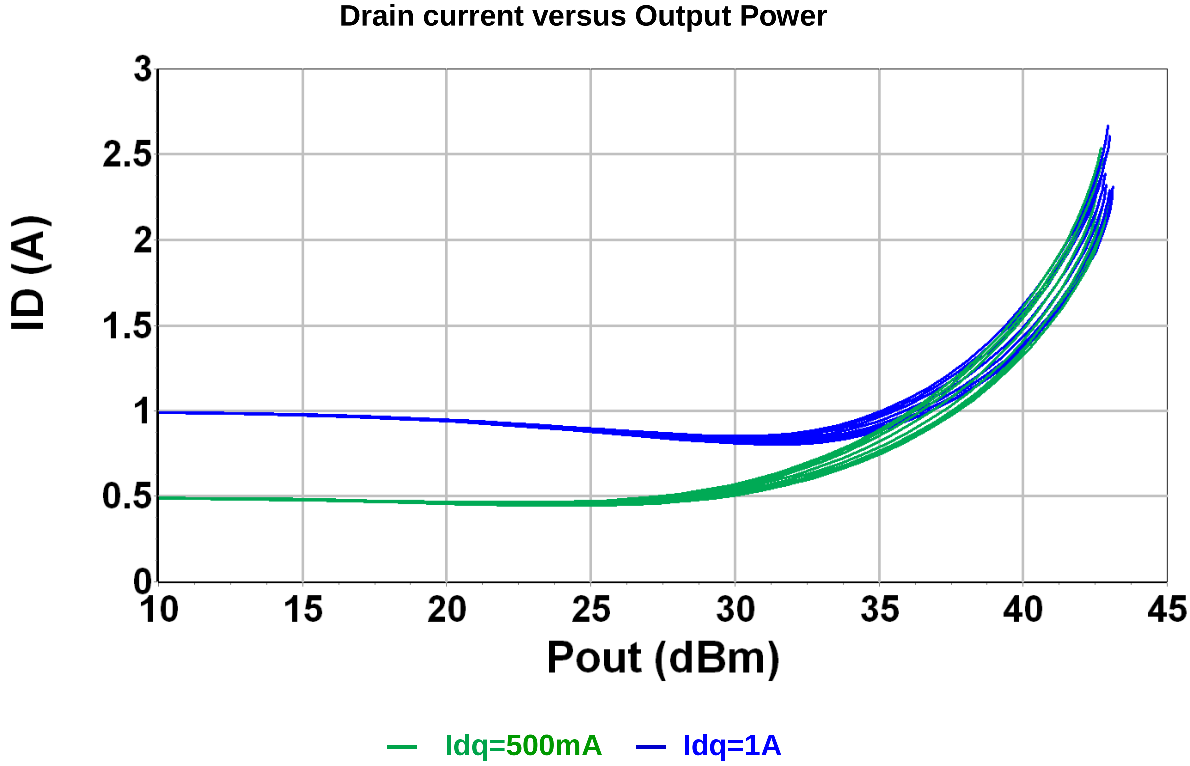

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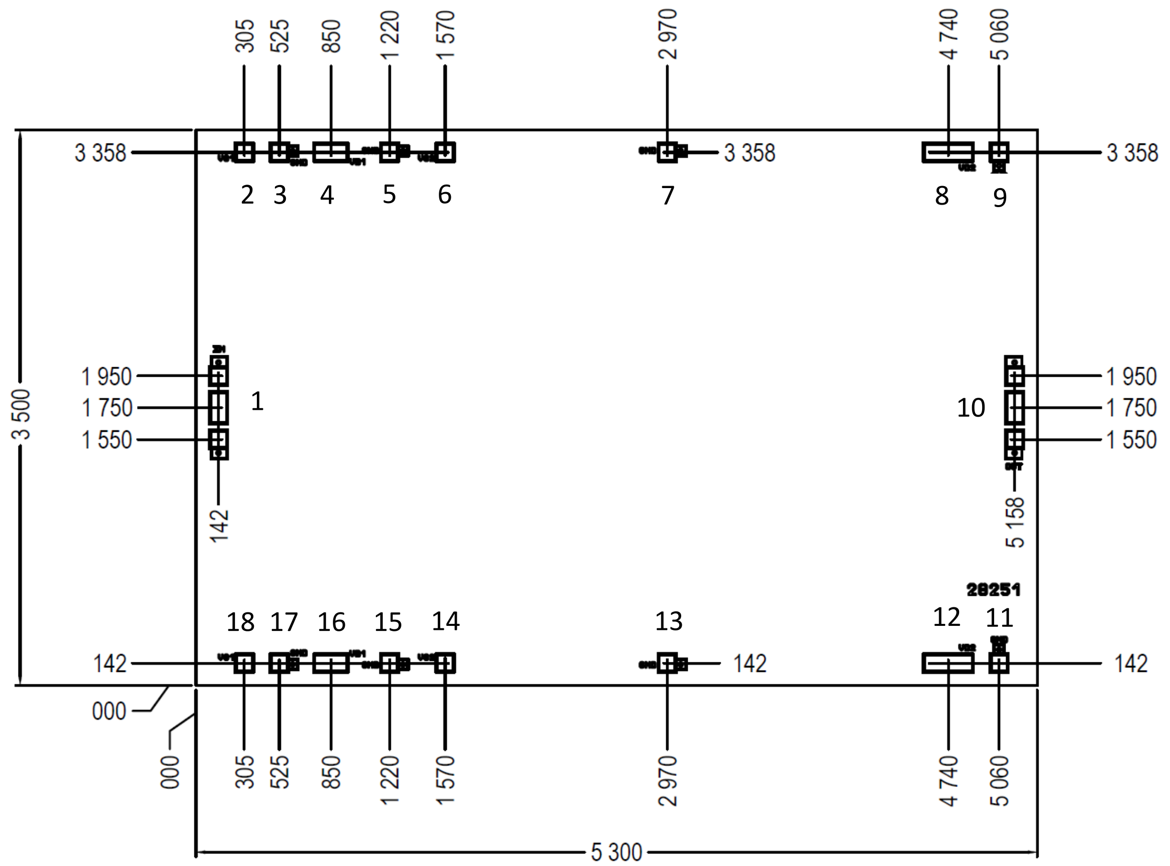
Chip Mechanical data



Chip size = 5300µmx3500µm ±50µm
Chip thickness = 70µm ±10µm

Chip width and length are given with a tolerance of ±50µm
RF pads (1, 10) = 208 x 118µm²

DC pads (2, 3, 5, 6, 7, 9, 11, 13, 14, 15, 17, 18) = 118 x 118µm²
DC pads (4, 16) = 218 x 118µm²
DC pads (8, 12) = 318 x 118µm²

PAD Number	Name	Description
1	IN	RF input
3, 5, 7, 9, 11, 13, 15, 17	GND	Ground (Not connected)
2, 18	VG1	Gate voltage of 1st stage
6, 14	VG2	Gate voltage of 2nd stage
4, 16	VD1	Drain voltage of 1st stage
8, 12	VD2	Drain voltage of 2nd stage
10	OUT	RF output

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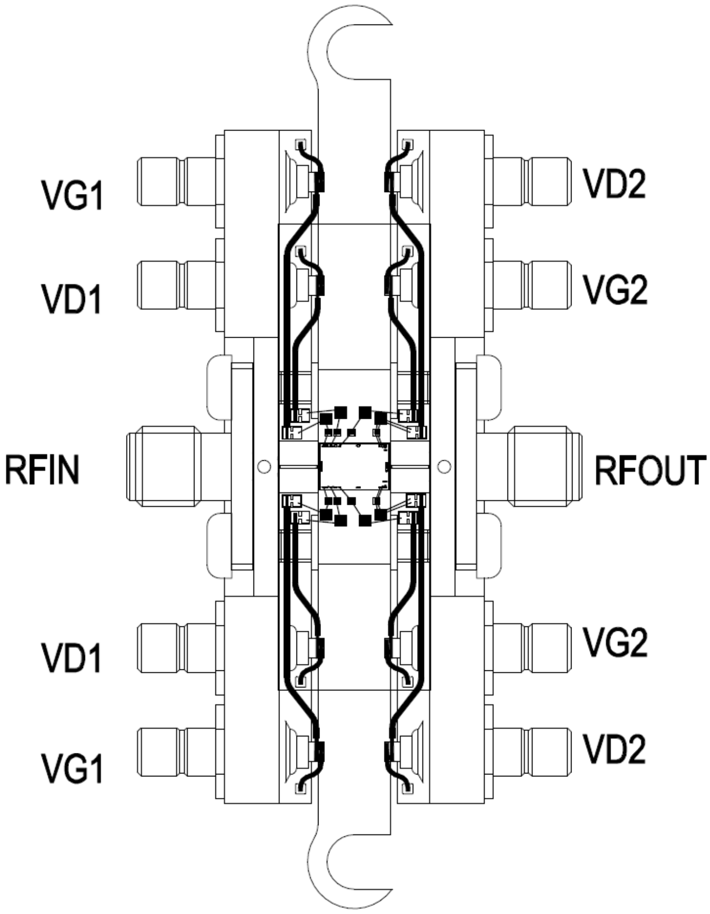
Recommended Test Jig



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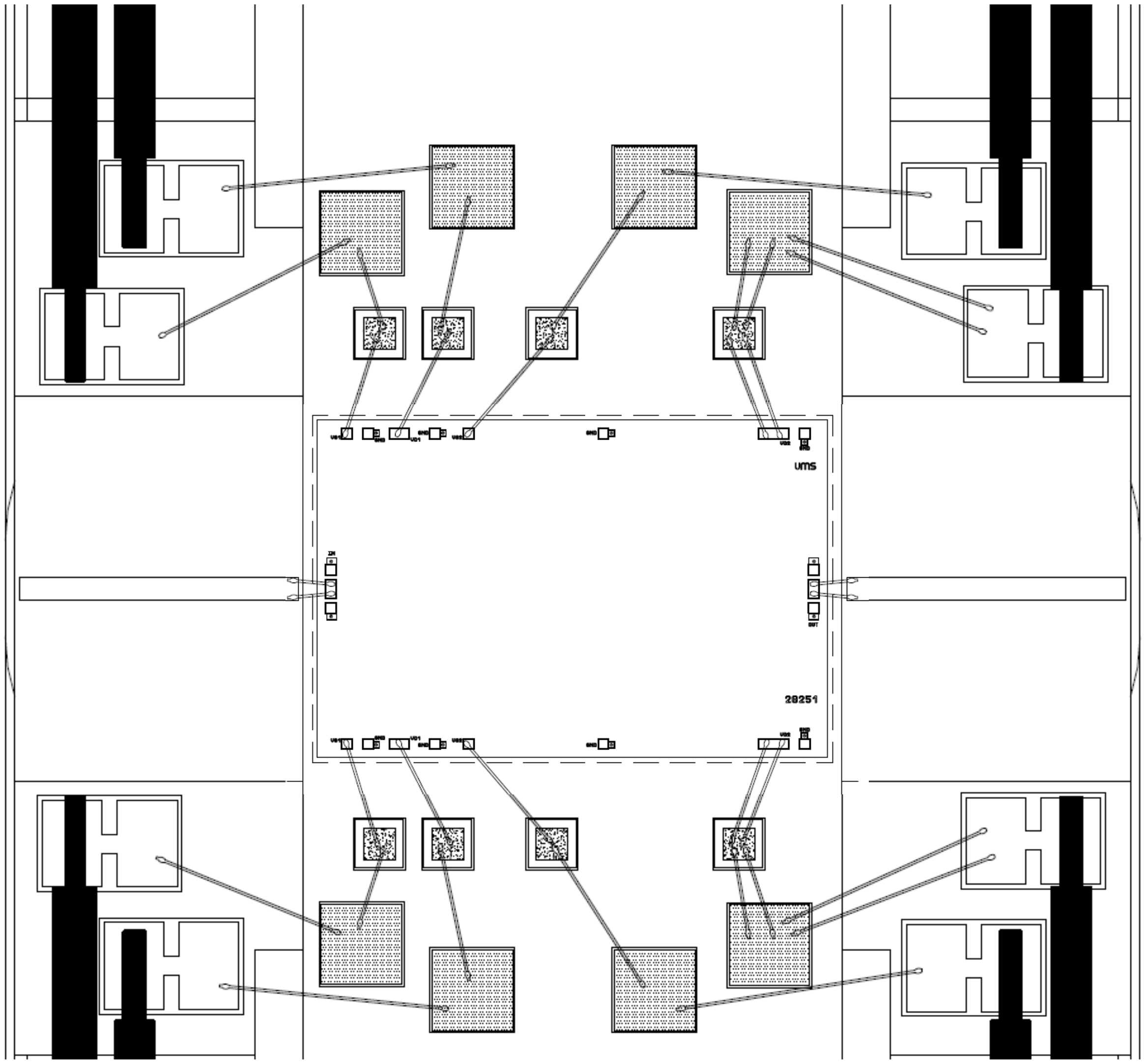
Recommended assembly plan



3 levels of decoupling capacitor have been used:
First level of capacitor is 120pF, second level is 10nF and third level is 4.7µF. Only 120pF and 10nF capacitors could be seen on the previous assembly drawing (close to the chip)

Note: Supply feed should be bypassed. 25µm diameter gold wire is to be preferred.

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Notes:

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Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended reflow process assembly

Refer to the application note AN0001 available at https://www.ums-rf.com for die attach.

Ordering Information

Chip form:	CHA8352-99F/00

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