CHA6550-98F

17-23.6GHz Power Amplifier

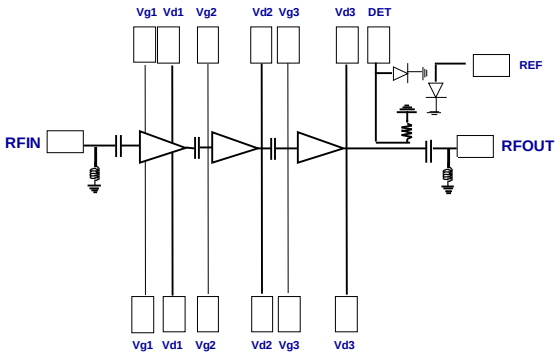
GaAs Monolithic Microwave IC bare die

Description

The CHA6550-98F is a three stage monolithic GaAs high power amplifier circuit, which integrates differential mode power detector at the output. Gain control up to 15dB is achievable thanks to gate voltage.

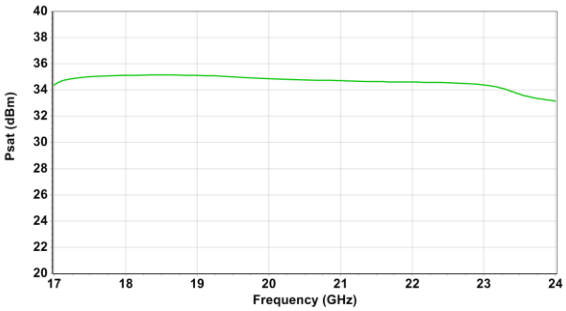
It is a field proven solution for Point to Point telecommunication systems, also suitable for other applications such as SATCOM. The circuit is highly linear and compatible with the last generation of Digital Pre-Distortion. Its versatile biasing condition helps to tune the performances.

The circuit is manufactured with a pHEMT space evaluated process, 0.15µm gate length.



Main Features

- Broadband performances: 17-23.6GHz
- 34dBm saturated power
- 39dBm OIP3
- 22dB gain
- Gain control up to 15dB
- DC bias: Vd = 6Volt @ Id=1.3A
- Chip size 3.46x3.61x0.07 mm



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	17		23.6	GHz
Gain	Linear Gain		22		dB
Psat	Saturated output power		34		dBm
OIP3	Output IP3		39		dBm

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Electrical Characteristics

Tamb.= +25°C, Vd = +6.0V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	17		23.6	GHz
Gain	Small Signal Gain		22		dB
ΔG	Gain variation in temperature		± 0.03		dB/°C
Psat	Saturated Output Power		34		dBm
OIP3	Output IP3		39		dBm
PAE	PAE at saturation		20		%
CG	Gain control range		15		dB
NF	Noise figure		5.7		dB
Rlin	Input Return Loss		13		dB
Rlout	Output Return Loss		11.5		dB
Dr	Detection dynamic range(for output power detection up to Psat)		30		dB
Vdetect	Voltage detection V_{REF}- V_{DET} up to Psat		10 to 1500		mV
Vg	DC gate Voltage		-0.65		V
Idq	Total drain current		1.3		A

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	8	V
Id	Drain bias quiescent current	1600	mA
Vg	Gate bias voltage	-2 to 0	V
Pin	Maximum Input Power	+15	dBm
Tj	Junction temperature	175	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Temperature Range

Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

Typical Bias Conditions

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd1	DC Drain voltage 1st stage	6.0	V
Vd2	DC Drain voltage 2nd stage	6.0	V
Vd3	DC Drain voltage 3rd stage	6.0	V
Vg1	DC Gate voltage 1st stage	-0.65	V
Vg2	DC Gate voltage 2nd stage	-0.65	V
Vg3	DC Gate voltage 3rd stage	-0.65	V

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Typical on-wafer Sij parameters (Pulsed mode)

Tamb.= +25°C, Vd = +6.0V, Id = 1300mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
1	-0.280	173.1	-75.886	-134.2	-72.509	-86.5	-0.184	172.7
2	-0.314	166.1	-71.499	59.1	-69.300	2.9	-0.208	165.7
3	-0.373	158.8	-64.883	-112.6	-78.386	-156.2	-0.307	158.1
4	-0.428	150.6	-85.011	-115.5	-66.754	77.4	-0.354	149.8
5	-0.510	141.8	-61.758	-31.5	-52.802	-12.6	-0.535	140.8
6	-0.962	130.7	-65.526	-39.6	-43.019	-110.9	-1.248	131.3
7	-1.803	121.5	-65.435	-72.2	-41.164	144.8	-2.023	122.1
8	-2.688	110.0	-73.091	-62.8	-42.560	63.3	-2.614	116.6
9	-4.157	105.4	-60.582	40.7	-46.895	1.6	-2.992	106.4
10	-4.342	99.7	-55.230	-160.2	-47.542	-64.5	-3.487	94.1
11	-4.698	84.7	-58.206	121.4	-52.458	-111.9	-4.143	76.4
12	-6.106	61.5	-60.266	-92.4	-62.341	-148.3	-5.982	49.3
13	-9.715	28.6	-47.879	-158.7	-61.237	59.9	-10.912	10.4
14	-20.373	-21.9	-50.147	141.3	-21.874	-122.0	-23.272	-31.0
15	-23.097	126.6	-48.246	95.2	3.172	95.7	-21.437	83.4
16	-21.831	141.3	-49.768	78.4	18.078	-70.7	-33.951	52.5
17	-22.855	105.9	-46.299	58.5	22.388	133.5	-26.412	-27.7
18	-16.778	130.7	-43.679	-7.9	23.215	3.9	-19.550	179.7
19	-24.247	72.2	-45.736	-61.8	22.901	-97.5	-29.123	-126.0
20	-29.287	121.7	-50.811	-109.3	23.687	164.0	-20.692	-162.5
21	-45.532	6.6	-53.999	-123.6	24.182	64.7	-22.713	153.4
22	-21.384	-87.2	-48.254	-173.2	24.765	-35.9	-23.625	-78.5
23	-22.196	170.7	-54.600	112.9	24.449	-147.6	-21.237	-171.4
24	-27.004	-93.9	-49.814	-140.0	22.962	100.5	-27.412	-126.1
25	-19.684	-112.3	-49.256	164.5	21.620	-29.2	-13.970	-108.2
26	-29.799	158.4	-39.567	148.7	11.833	176.7	-22.607	166.3
27	-16.578	-87.4	-37.708	111.2	-2.301	76.4	-24.465	-142.3
28	-13.991	-115.8	-38.541	72.8	-14.787	3.8	-18.369	-119.7
29	-14.802	-138.4	-35.277	33.8	-26.586	-43.5	-17.030	-168.6
30	-18.498	-151.5	-40.281	-10.3	-35.496	-58.0	-21.376	-140.3
31	-23.154	-95.3	-37.236	-35.5	-39.287	-37.0	-24.902	-139.0
32	-13.089	-71.1	-39.345	-33.9	-38.642	-57.0	-13.900	-112.3
33	-8.915	-87.4	-47.220	-39.0	-41.821	-125.1	-21.645	147.6
34	-6.750	-107.0	-41.299	-81.5	-42.482	-91.6	-13.682	17.4
35	-5.404	-121.4	-37.585	-113.1	-42.891	-130.0	-7.588	-19.6
36	-4.749	-137.2	-43.064	-124.5	-47.039	156.9	-4.016	-63.2
37	-4.651	-151.9	-40.026	-130.6	-48.961	89.3	-2.796	-88.0
38	-4.258	-165.5	-36.769	-174.9	-42.728	121.7	-2.130	-115.3
39	-4.389	178.8	-39.984	87.6	-41.884	36.0	-2.914	-113.3
40	-5.162	159.2	-21.342	86.9	-39.354	72.8	3.812	-37.2

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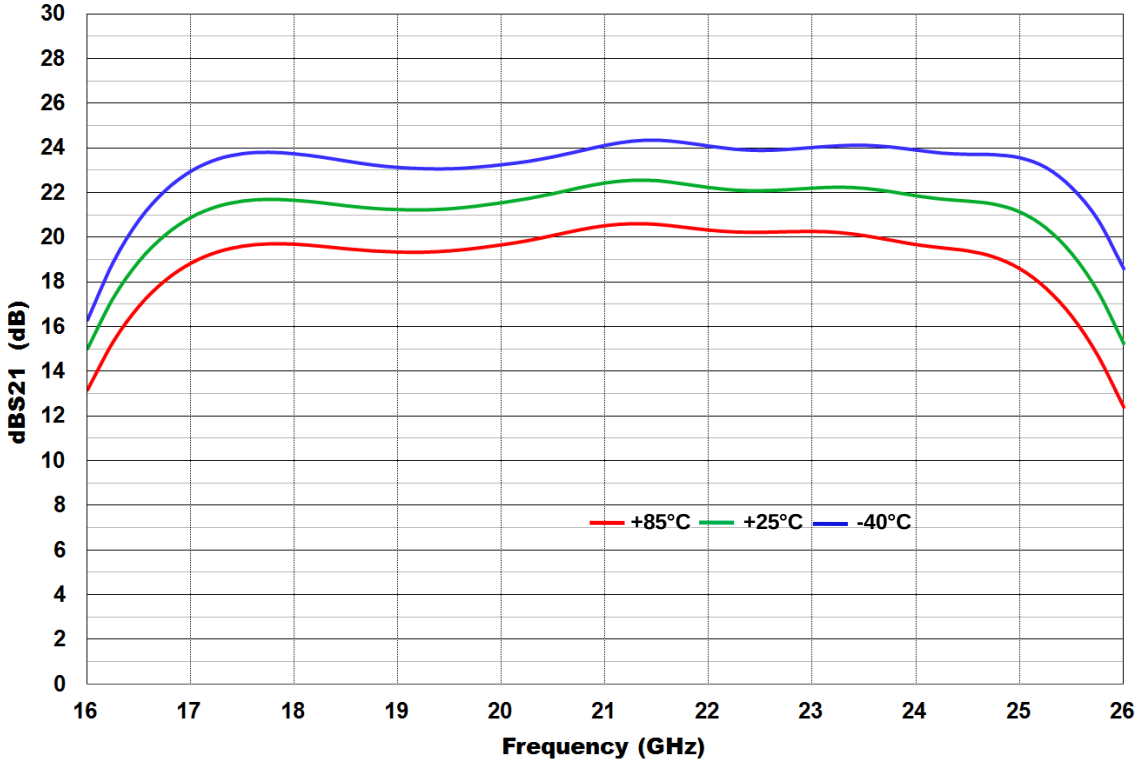
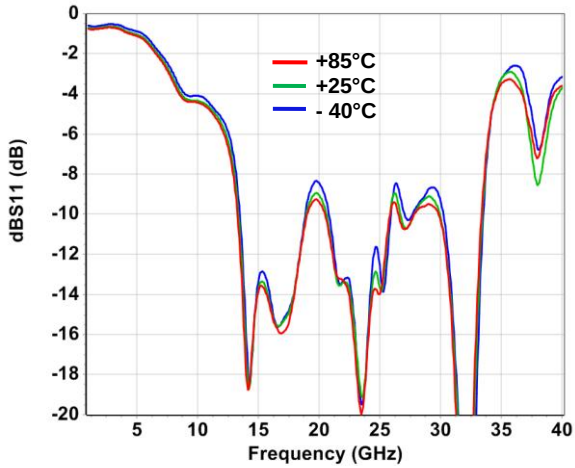
Typical Board Measurements

Vd = +6.0V, Id = 1300mA
Measurement performed in the access plans of the die.

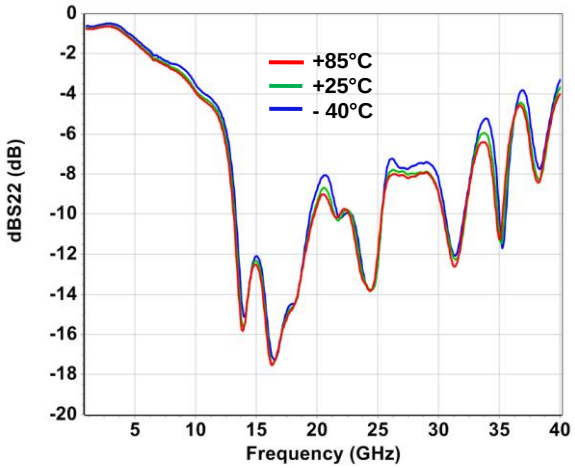
Linear Gain versus Frequency in Temperature



Input Return Loss versus Frequency in Temperature



Output Return Loss versus Frequency in Temperature



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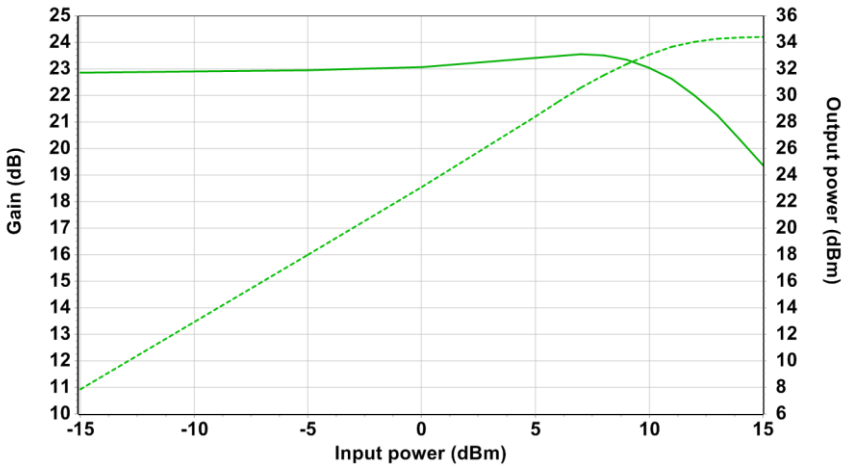
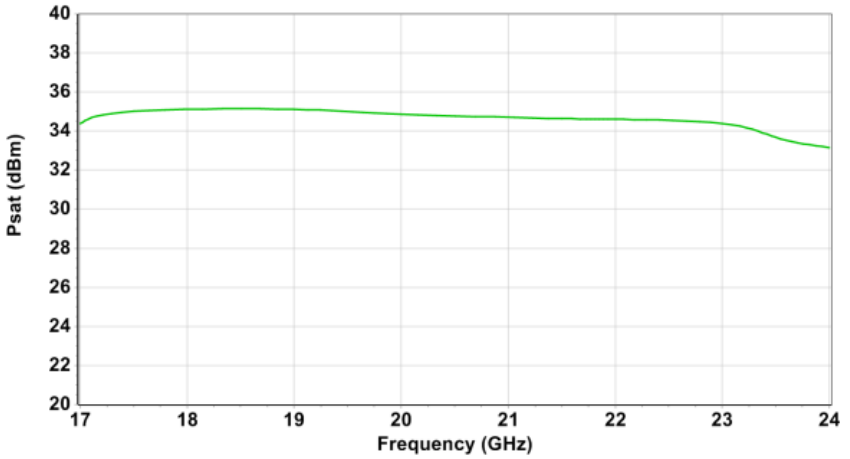
Typical Board Measurements

Tamb.= +25°C, Vd = +6.0V, Id = 1300mA

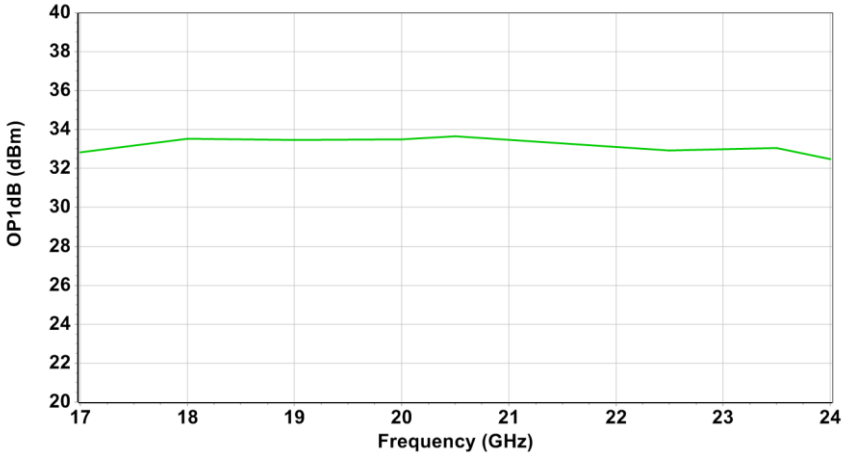
Gain & Output Power versus Input Power at 20.5GHz



Saturated Power versus Frequency



Output Power at 1dB compression versus Frequency



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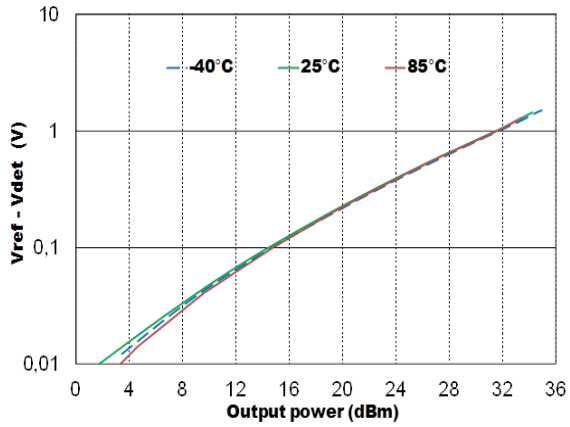
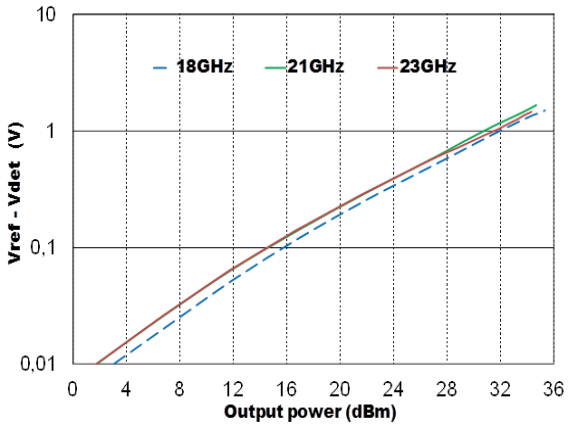
Typical Board Measurements

Tamb.= +25°C, Vd = +6.0V, Id = 1300mA

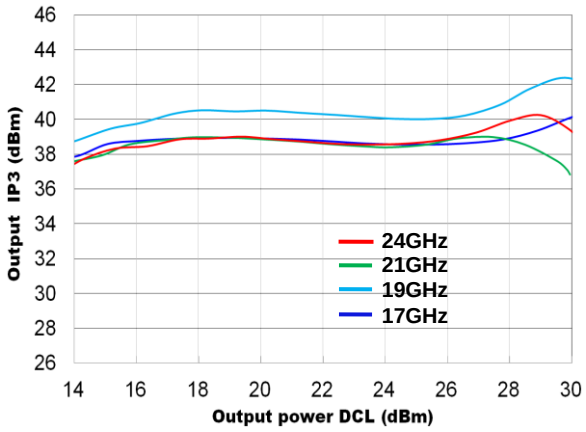
Power Detector versus Pout and Temperature



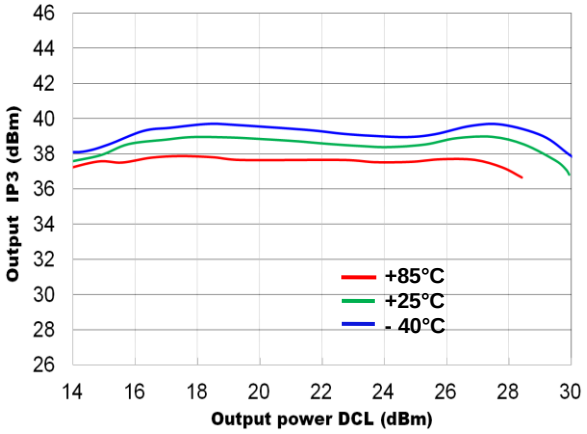
Power Detector versus Pout and Frequency



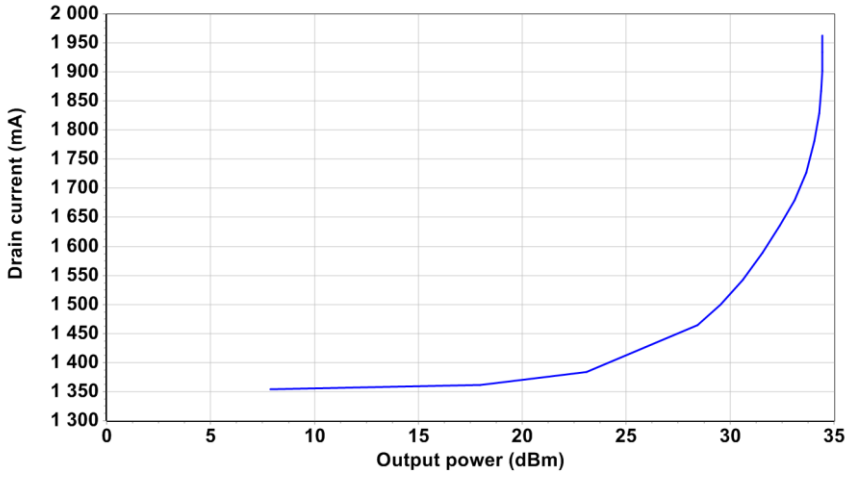
Output IP3 versus Output Power DCL and Frequency



Output IP3 versus Output Power DCL in Temperature at 21GHz



Total Drain Current versus Output Power at 20.5GHz



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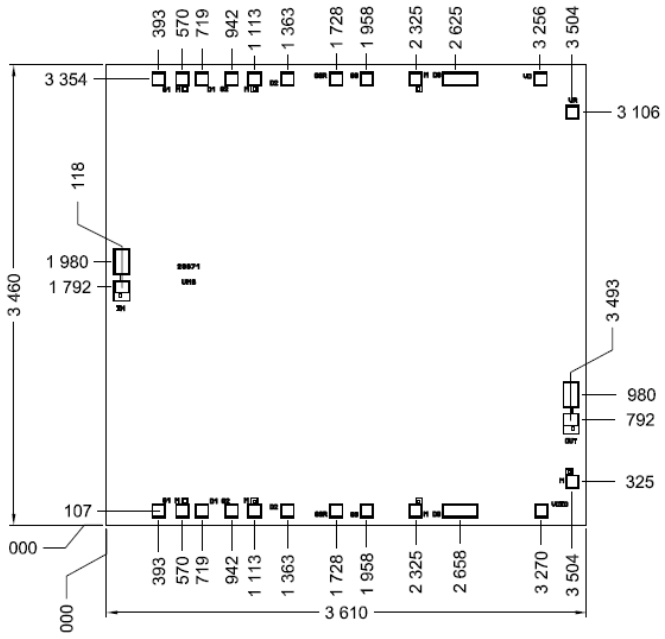
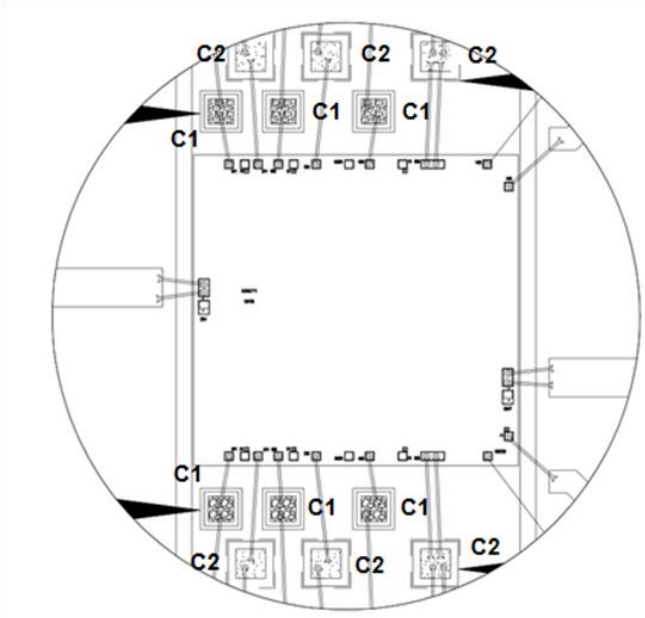
Mechanical data



Chip thickness: 70µm.
All dimensions are in micrometers
DC pad size: 83um x 83 um (BCB opening)
RF pad size: 90um x 180 um (BCB opening)

Recommended assembly plan



C1=22pF (on gate access) & C2=120pF (on drain access)

Note: Supply feed should be bypassed. 25µm diameter gold wire is to be preferred.

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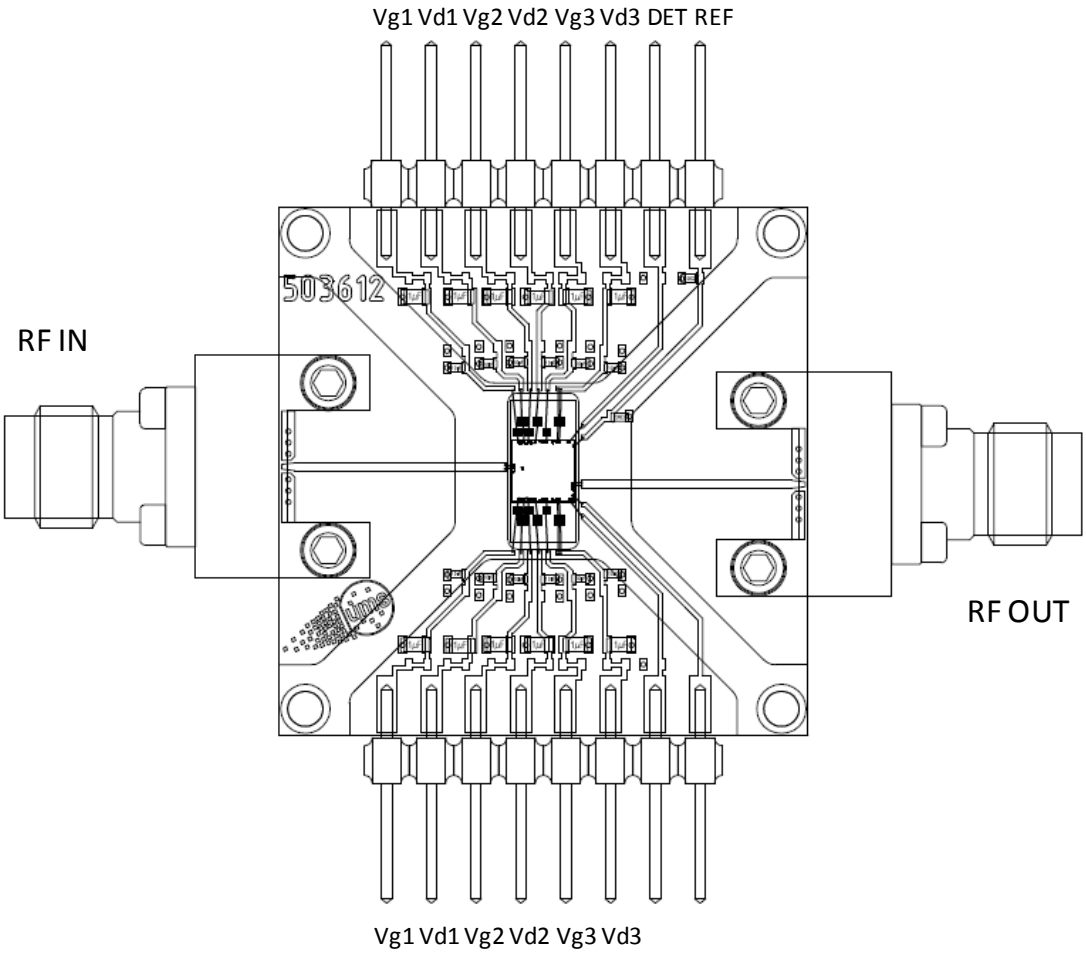
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003C / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the chip.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 22pF ±10%, 10nF ±10% and 1µF ±10% are recommended for the gate accesses.
- Decoupling capacitors of 120pF ±10%, 10nF ±10% and 1µF ±10% are recommended for the drain accesses.
- A 10KΩ resistor is recommended on VREF & VDET accesses for the detector
- Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.



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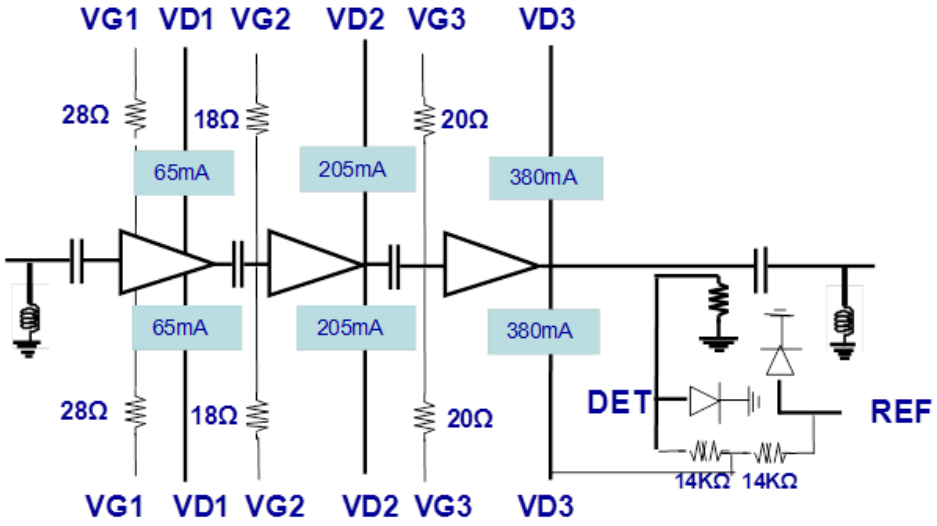
DC Schematic

HPA: 6V, 1.3A



Biasing procedure

Device Power Up instructions:

1. Ground the device
2. Bias HPA gate voltage at Vg close to Vpinch-off (example: Vg ≈ -2V)
3. Apply Vds quiescent bias voltage (Example: Vd = 6V)
4. Increase slowly Vgs up to quiescent bias drain current Ids0 (pulsed applied on the gate)
5. Apply RF input power

Device Power down instructions:

1. Remove RF input power
2. Decrease HPA gate voltage up to Vg -2V
3. Decrease drain voltage up to 0V

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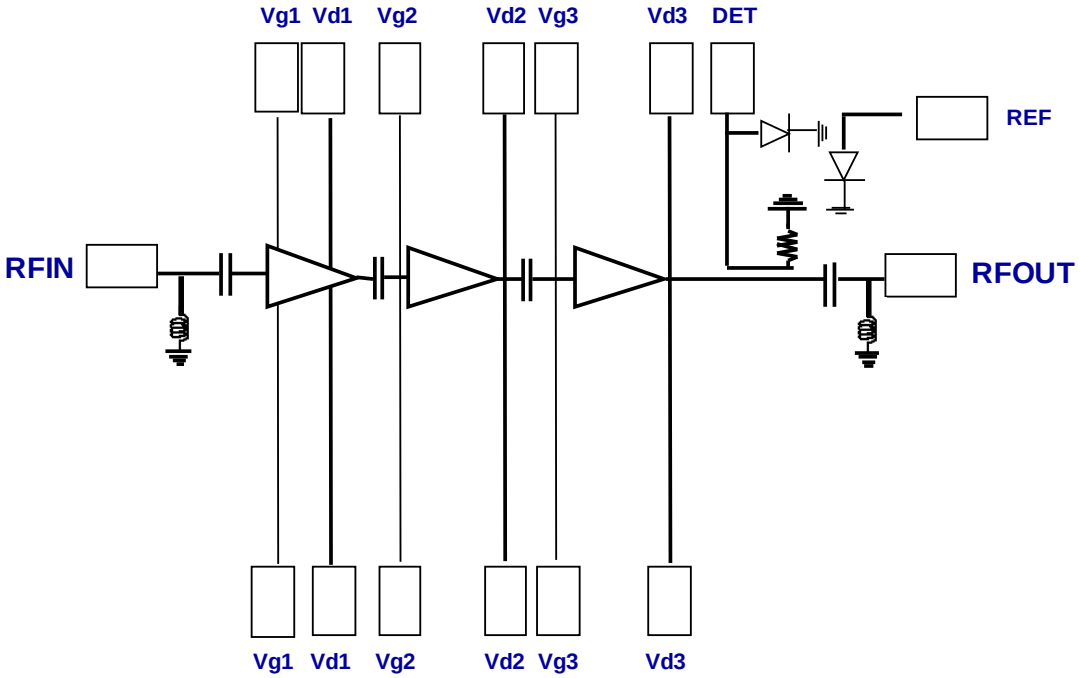
Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.



The DC connections do not include any decoupling capacitor, therefore it is mandatory to provide a good external DC decoupling (22pF, 120pF, 10nF, 1µF) on the PC board, as close as possible to the bare die.

A 10KΩ resistor is recommended in parallel to VDET, and VREF accesses.

The circuit includes ESD protections on all RF and DC accesses.

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Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Ordering Information

Bare Die:	CHA6550-98F/00

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