

17.3-21.5GHz GaN Power Amplifier

GaN Monolithic Microwave IC in SMD leadless package

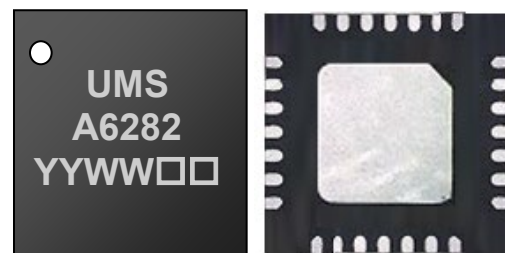
Description

The CHA6282-QCB is a three-stage GaN High Power Amplifier in the frequency band 17.3-21.5GHz. This HPA typically provides 4W output power associated to 28% of Power Added Efficiency. The circuit exhibits a small signal gain higher than 30dB. The overall power supply is 18V/260mA.

The circuit is a very versatile amplifier for high performance systems.

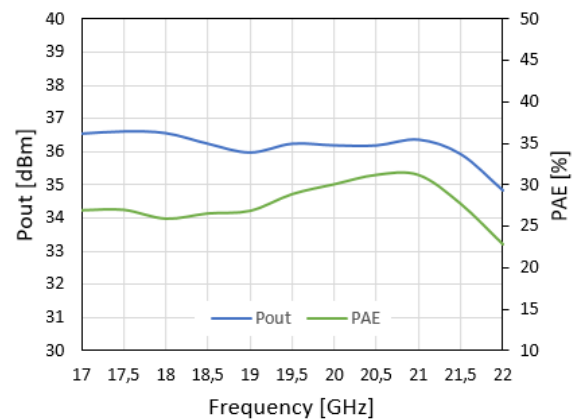
The circuit is dedicated to Space applications and well suited for a wide range of microwave applications and systems.

The product is developed on a robust 0.15 μ m gate length GaN on SiC HEMT process and is provided on low cost SMD RoHS compliant plastic package.



Main Features

- 17.3-21.5GHz frequency range
- Linear gain is 30 dB
- $P_{out}=36\text{dBm}$ for $P_{in}=18\text{dBm}$
- NPR > 13dB for $P_{out} = 2\text{Watts}$
- PAE=28% at P_{sat}
- DC bias: $V_d=18\text{Volts}$ @ $I_{dq}=260\text{mA}$
- 28 Leads - QFN 5x5mm²
- MSL3



Main Electrical Characteristics

$T_{case} = +25^{\circ}\text{C}$

T_{case} : QFN backside temperature

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	17.3		21.5	GHz
Gain	Linear Gain		30		dB
PAE	Power Added Efficiency		28		%
P_{sat}	Saturated Output Power		36		dBm

These values are representative of on board measurements as defined on the drawing in paragraph "Evaluation Board".

Specifications

$T_{case} = +25^{\circ}\text{C}$, $V_d = +18\text{V}$, $I_{dq} = 260\text{mA}$

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	17.3		21.5	GHz
Gain	Linear Gain		30		dB
S_{11}	Input return loss		15		dB
S_{22}	Output return loss		15		dB
P_{sat}	Saturated output Power		36		dBm
NPR	Noise Power Ratio @ $P_{out}=2\text{Watt}$		14		dB
PAE	Power Added Efficiency		28		%
I_{dq}	Quiescent Current		0.26		A
V_d	Drain Voltage		18		V

“Power ON” sequence

1. Ground the device
2. Set the gate voltage to -5V
3. Apply the drain voltage V_d (Typically 18V)
4. Increase V_g up to quiescent bias drain current I_{dq}
5. Apply RF signal

“Power OFF” sequence

1. Turn off RF signal
2. Decrease the gate voltage to -5V
3. Decrease the drain voltage to 0V
4. Turn off V_d supply
5. Turn off V_g supply

Absolute Maximum Ratings ⁽¹⁾T_{case} = +25°C

Symbol	Parameter	Values	Unit
V _d	Drain bias voltage	27	V
I _d	Drain bias current (with RF signal at saturation)	1.1	mA
V _g	Gate bias voltage	-7 to -2	V
P _{in}	Maximum input power	20	dBm

⁽¹⁾ Operation of this device above anyone of these parameters may cause permanent damage.

Recommended Operating Range ^{(3), (4)}

Symbol	Parameter	Values	Unit
V _d	Drain bias voltage	18 to 25	V
I _d	Drain bias current (without RF)	182 to 260	mA
V _g	Gate bias voltage	~ -2.5 to ~ -3	V
P _{in}	Maximum input power	18	dBm
T _j	Maximum Junction temperature ⁽²⁾	200	°C

⁽²⁾ Value is provided for T_{case}=95°C

⁽³⁾ Electrical performances are defined for specified test conditions

⁽⁴⁾ Electrical performances are not guaranteed over all recommended operating conditions

Temperature Range

T _{case}	Operating temperature range	-40 to +95	°C
T _{stg}	Storage temperature range	-55 to +150	°C

Typical Bias ConditionsT_{case} = +25°C

Symbol	Pad N°	Parameter	Values	Unit
V _g	12, 24, 26, 28	Gate Voltage	~ -2.7	V
V _d	10, 11, 13, 23, 25	Drain Voltage	18	V

Device thermal performances

The thermal performances of the device are based on UMS rules to evaluate the junction temperature (T_j). This temperature is defined as the peak temperature in the channel area.

This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHA6282-QCB is fabricated (GaN Power PHEMT 0.15 μ m).

All the figures given in this section are obtained assuming that the QFN device is only cooled down by conduction through the package thermal pad (to be adapted to the assembly/package) (no convection mode considered).

The temperature is monitored at the package back-side interface (T_{case}).

The system maximum temperature must be adjusted in order to guarantee that junction temperature T_j remains below the maximum value specified in the Recommended Operating Range table. So, the system PCB must be designed to comply with this requirement.

The thermal resistance (R_{TH}) is given in the tables below for the full circuit in CW mode.

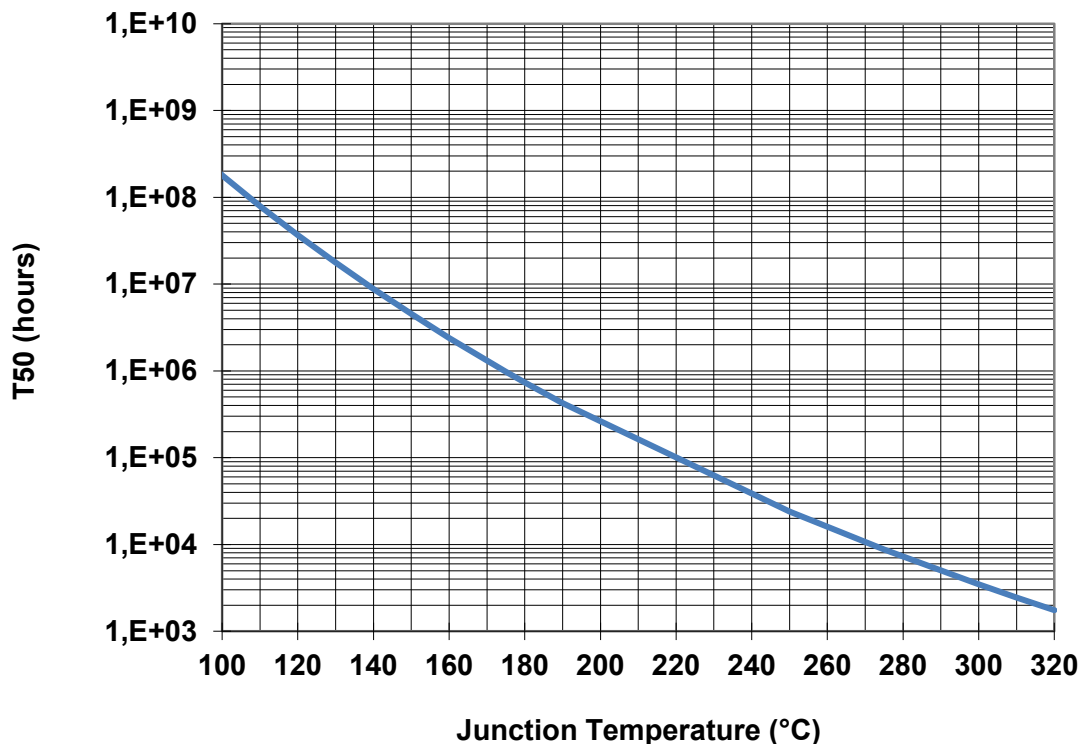
Parameter	Biasing conditions	T_j (°C)	R_{TH} (°C/W)	T50 (hours)
$R_{TH}^{(1)}$ Thermal Resistance (Junction to Case)	Psat=36.6dBm Pdiss= 10.25W CW	183	9.56	7.3E+05

¹ Assuming $T_{case} = 85^\circ\text{C}$

Parameter	Biasing conditions	T_j (°C)	R_{TH} (°C/W)	T50 (hours)
$R_{TH}^{(2)}$ Thermal Resistance (Junction to Case)	Psat=36.6dBm Pdiss= 10.25W CW	160	8.78	2.4E+06

² Assuming $T_{case} = 70^\circ\text{C}$

Median Life Time versus Junction Temperature



Typical Package Sij parameters

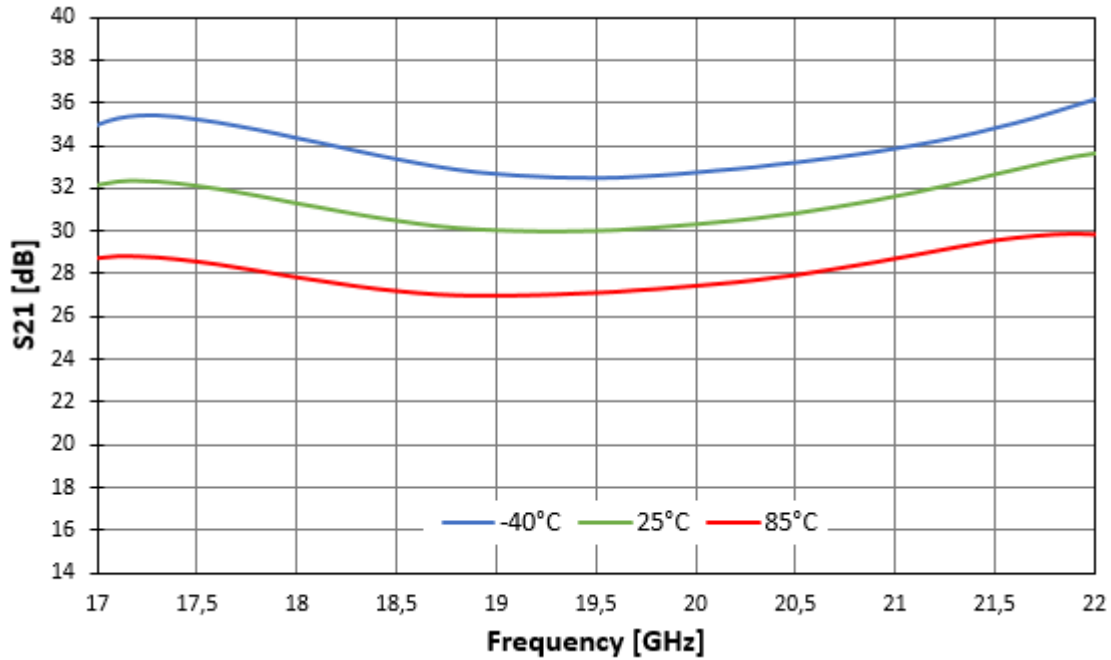
$T_{case} = +25^{\circ}C$, $V_d = +18V$, $I_{dq} = 260mA$

Freq (GHz)	dBS11	PhS11	dBS12	PhS12	dBS21	PhS21	dBS22	PhS22
1	-2.16	44.59	-86.28	-42.81	-85.36	-49.93	-1.56	47.78
2	-2.55	-91.43	-78.15	-178.05	-41.39	-13.92	-1.69	-78.03
3	-3.37	135.23	-83.98	95	-33.26	13.77	-2.24	150.39
4	-3.97	-2.7	-85.79	-29.67	-34.88	-166.67	-2.85	10.72
5	-4.52	-153.73	-84	-40.84	-33.32	30.64	-3.14	-126.75
6	-4.15	53.87	-85.02	-91.8	-33.16	-140.54	-3.95	96.41
7	-3.69	-86.88	-81.53	156.13	-38.63	38.65	-4.84	-52.83
8	-3.65	132.4	-78.1	67.55	-57.33	48.7	-4.46	164.76
9	-3.3	-9.31	-62.04	-1.91	-44.74	-79.67	-4.72	29.38
10	-2.9	-143.45	-61.21	179.47	-43.37	167.89	-4.17	-104.94
11	-3.07	85.78	-63.39	24.94	-39.84	0.85	-3.35	115.57
12	-3.57	-47.37	-65.31	-103.54	-52.02	-144.22	-3.81	-21.82
13	-4.2	173.98	-64.92	99.84	-26.13	5.26	-3.82	-159.34
14	-4.98	33.41	-70.2	-36.09	-5.88	-156.7	-4.84	56.11
15	-7.15	-108.25	-80.19	-119.22	10.61	19.15	-6.78	-96.78
16	-12.02	87.62	-72.13	160.52	23.76	157.23	-8.73	105.13
17	-12.61	-83.93	-72.61	62.62	28.05	-79.46	-11.33	-55.42
18	-14.57	152.78	-70.99	-54.49	27.82	69.96	-12.2	140.5
19	-20.36	16.63	-70.23	-173.83	27.17	-119.78	-11.88	8.63
20	-19.04	-158.45	-68.29	73.12	27.6	54.37	-15.25	-122.57
21	-18.45	113.57	-69.53	-59.77	28.45	-140.72	-16.17	77.36
22	-11.05	68.39	-72.36	166.32	27.84	6.94	-21.9	-42.91
23	-7.07	-45.64	-81.8	96.43	23.53	142.92	-15.94	-22.78
24	-6.68	163.86	-74.52	27.08	13.34	-82	-10.13	-152.31
25	-4.94	27.92	-70.64	-108.06	-2.23	84.5	-8.58	73.56
26	-4.21	-82.55	-73.19	119.48	-21.23	-75.42	-6.59	-62.63
27	-4.51	165.7	-91.92	-48.43	-37.88	-95.75	-4.97	176.09
28	-5.06	42.67	-75.08	-65.82	-36.03	140.71	-4.66	60.54
29	-4.7	-81.63	-69.56	-158.95	-40.83	4.06	-4.87	-60.91
30	-4.21	166.72	-85.07	123.07	-47.01	-128.5	-4.7	174.87
31	-4.23	59.91	-71.05	-108.96	-54.32	114.32	-4.24	57.82
32	-4.41	-49.37	-70.68	81	-59.76	6.78	-3.94	-51.74
33	-4.81	-159.63	-76.76	-91.27	-64.7	-113.57	-4.15	-158.86
34	-5.28	81.72	-73.77	-27.25	-66.15	88.32	-4.86	87.5
35	-4.52	-36.68	-76.73	-146.68	-81.21	-116.51	-4.84	-39.28
36	-3.75	-134.51	-72.09	75.88	-67.56	91.83	-3.79	-147.85
37	-4.35	134.14	-63.46	-24.65	-62.51	-30.25	-3.94	117.88
38	-6.6	17.13	-66.6	-151.34	-68.39	-153.6	-5.32	6.69
39	-6.09	-124.26	-75.32	92.27	-68.46	103.35	-5.17	-122.28
40	-4.39	131.46	-74.97	38.65	-67.82	-95.49	-4.13	131.03

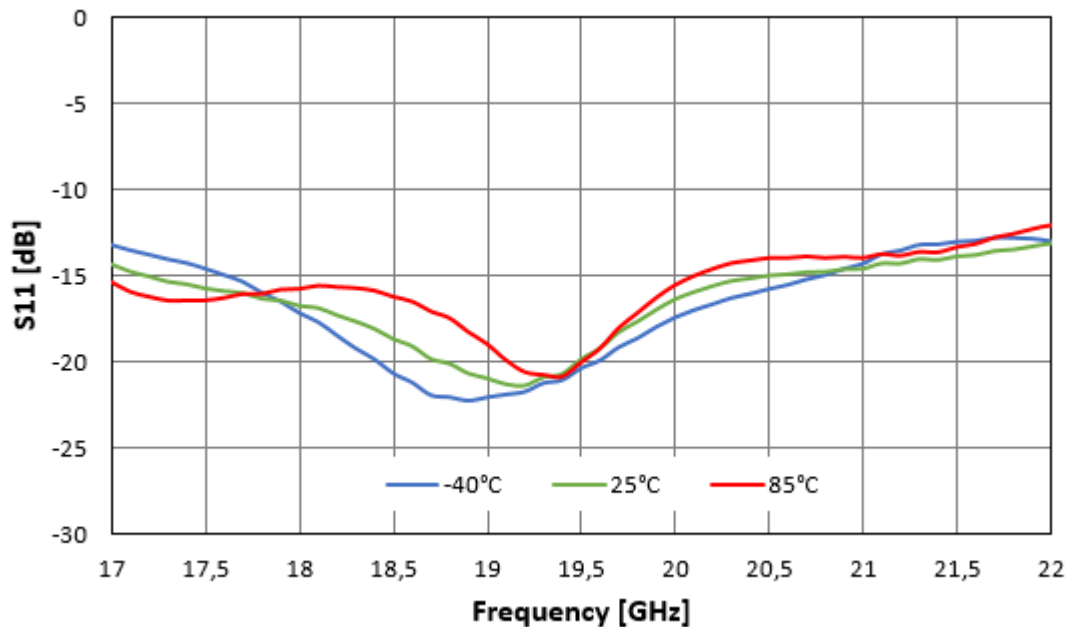
Typical Board Measurements : Small Signal Performances

$T_{case} = -40^{\circ}\text{C} / 25^{\circ}\text{C} / 85^{\circ}\text{C}$ (Backside QFN), $V_d = +18\text{V}$, $I_{dq} = 260\text{mA}$ (Adjusted at $T_{case}=25^{\circ}\text{C}$).
 Board losses are de-embedded. Measurements are given in the QFN access plan.

Linear Gain versus Frequency & temperature



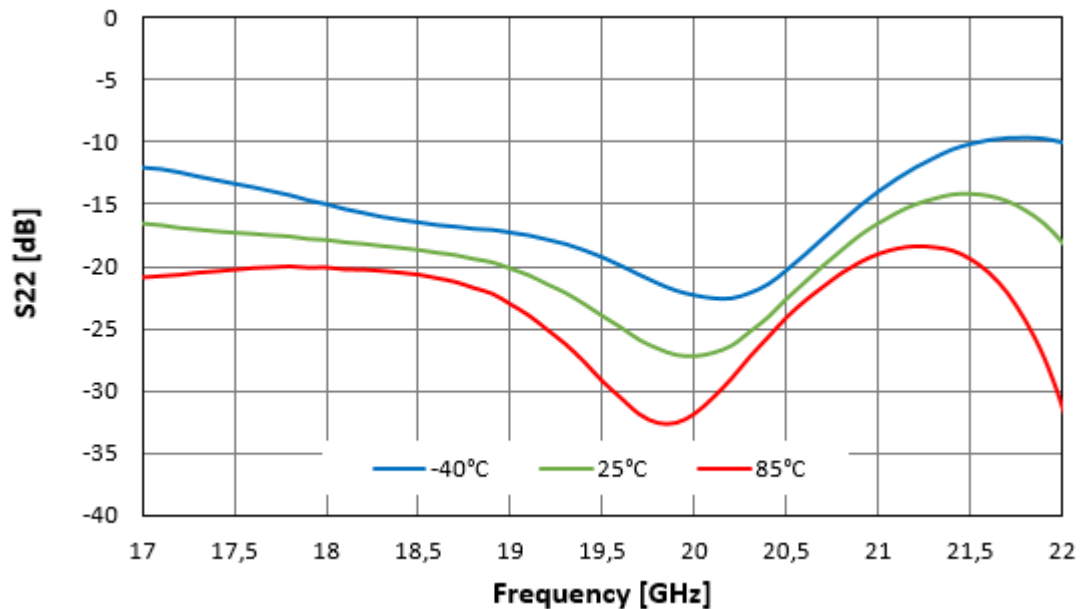
Input Return Losses versus Frequency & temperature



Typical Board Measurements : Small Signal Performances

$T_{\text{case}} = -40^{\circ}\text{C} / 25^{\circ}\text{C} / 85^{\circ}\text{C}$ (Backside QFN), $V_d = +18\text{V}$, $I_{dq} = 260\text{mA}$ (Adjusted at $T_{\text{case}} = 25^{\circ}\text{C}$).

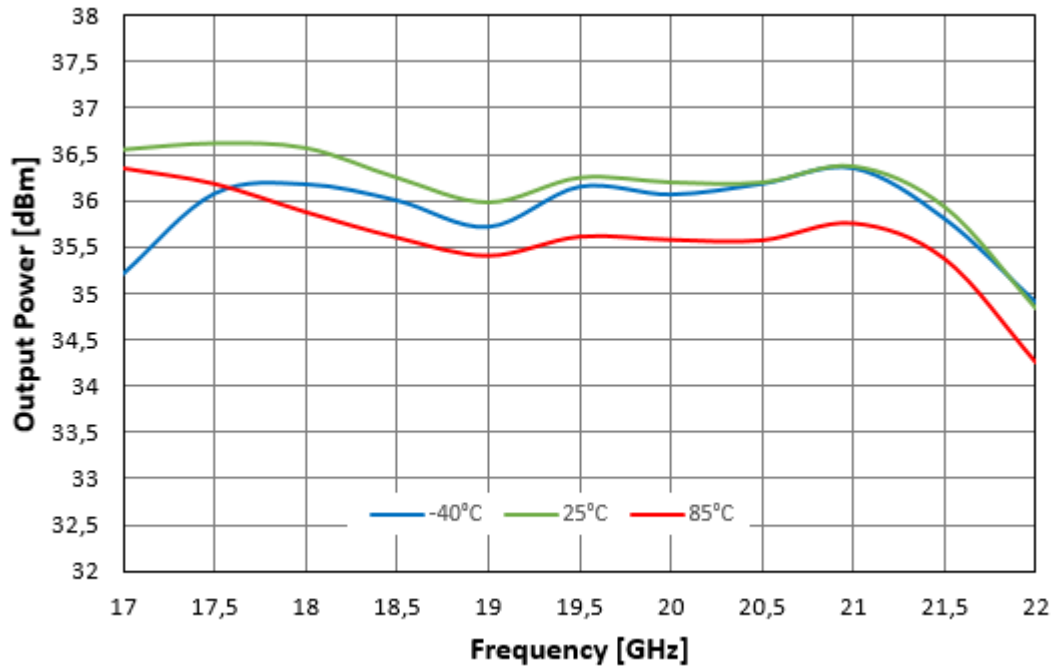
Board losses are de-embedded. Measurements are given in the QFN access plan.

Output Return Losses versus Frequency & temperature

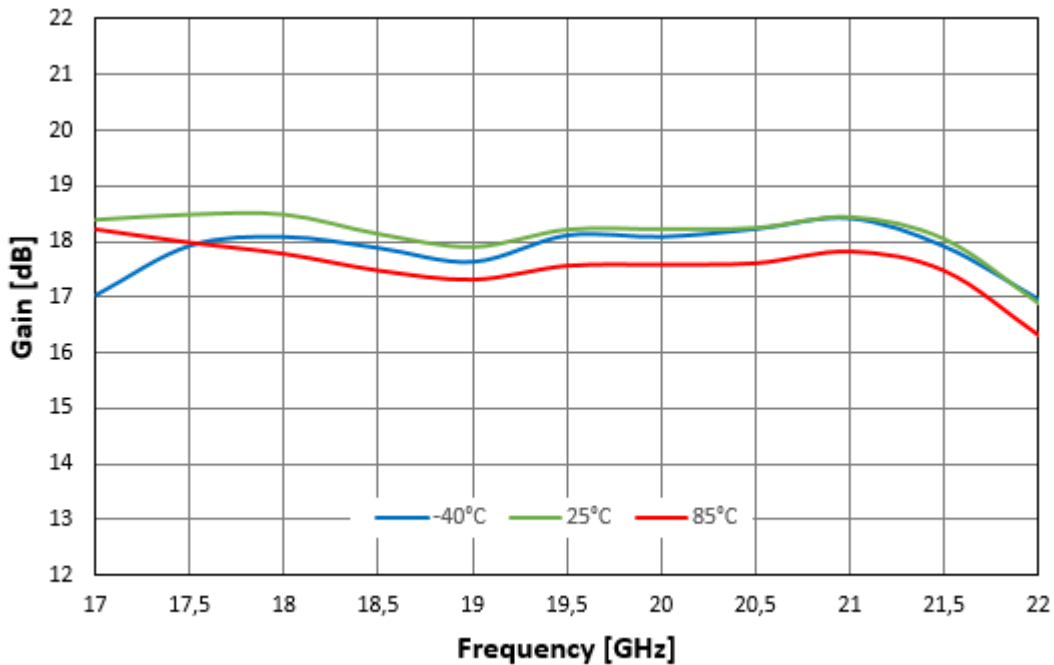
Typical Board Measurements : Non-linear performances

CW measurements: $P_{in}=18\text{dBm}$, $V_d = +18\text{V}$, $I_{dq} = 260\text{mA}$ (Adjusted at $T_{case}=25^\circ\text{C}$).
 Board losses are de-embedded. Measurements are given in the QFN access plan.

Output power versus Frequency & temperature



Gain versus Frequency & temperature

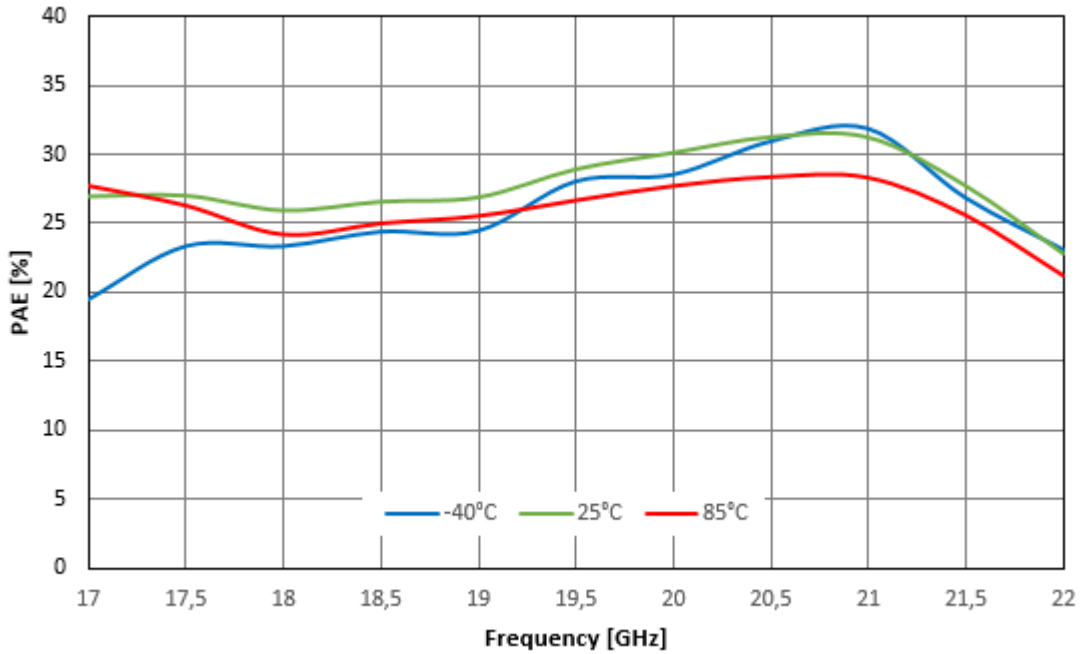


Typical Board Measurements : Non-linear performances

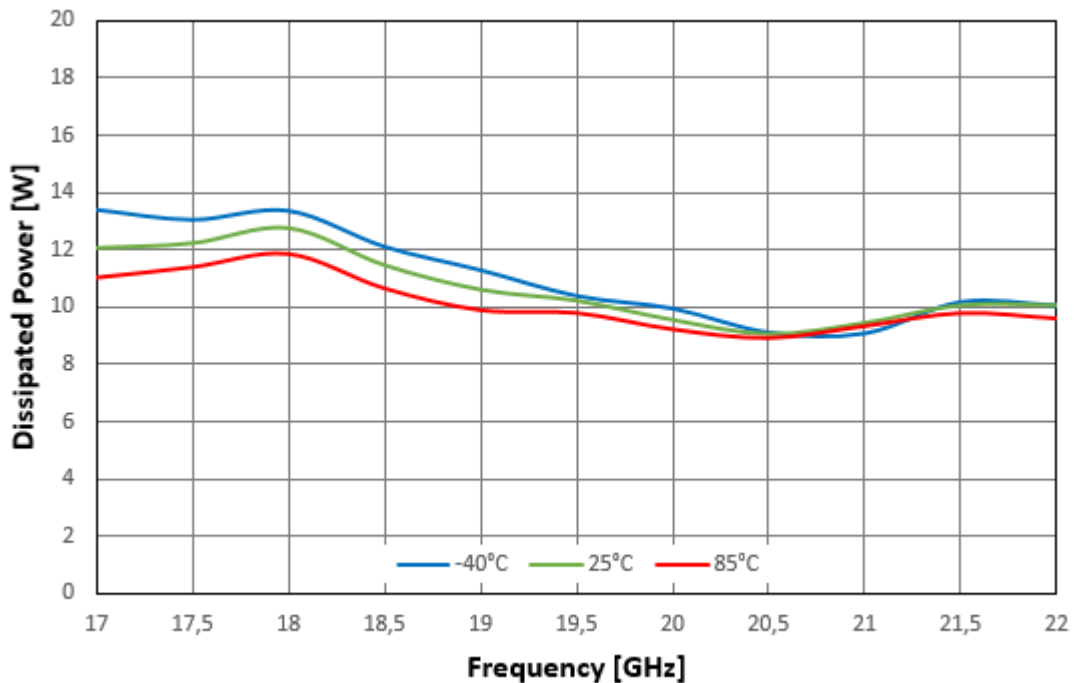
CW measurements: $P_{in}=18\text{dBm}$, $V_d = +18\text{V}$, $I_{dq} = 260\text{mA}$ (Adjusted at $T_{case}=25^\circ\text{C}$).

Board losses are de-embedded. Measurements are given in the QFN access plan.

Power Added Efficiency vs Frequency & temperature



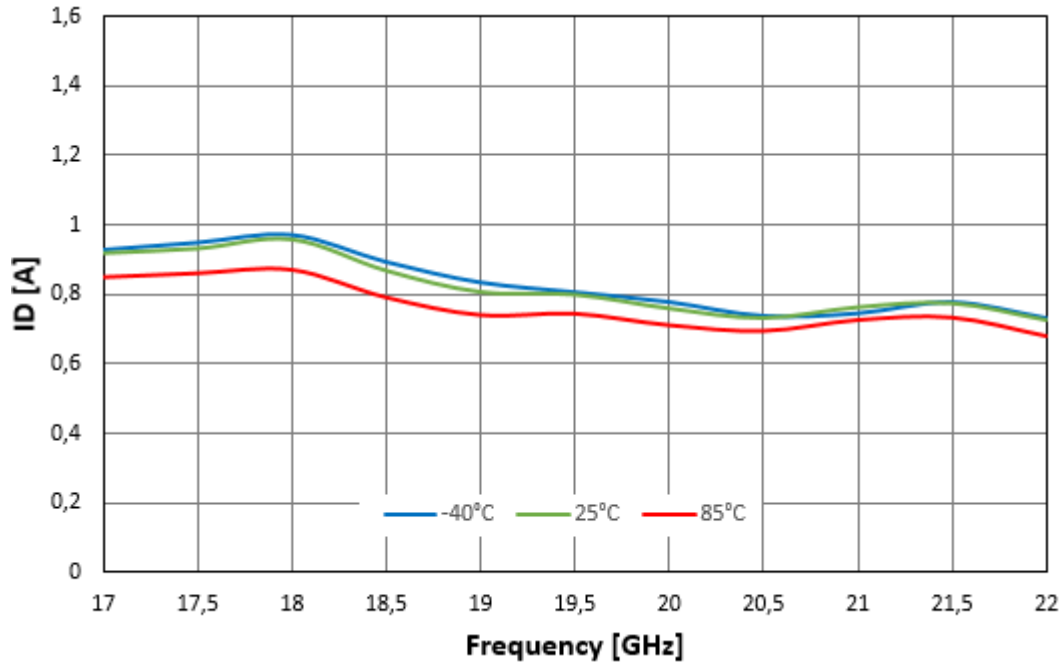
Dissipated Power versus Frequency & temperature



Typical Board Measurements : Non-linear performances

CW measurements: $P_{in}=18\text{dBm}$, $V_d = +18\text{V}$, $I_{dq} = 260\text{mA}$ (Adjusted at $T_{case}=25^\circ\text{C}$).
 Board losses are de-embedded. Measurements are given in the QFN access plan.

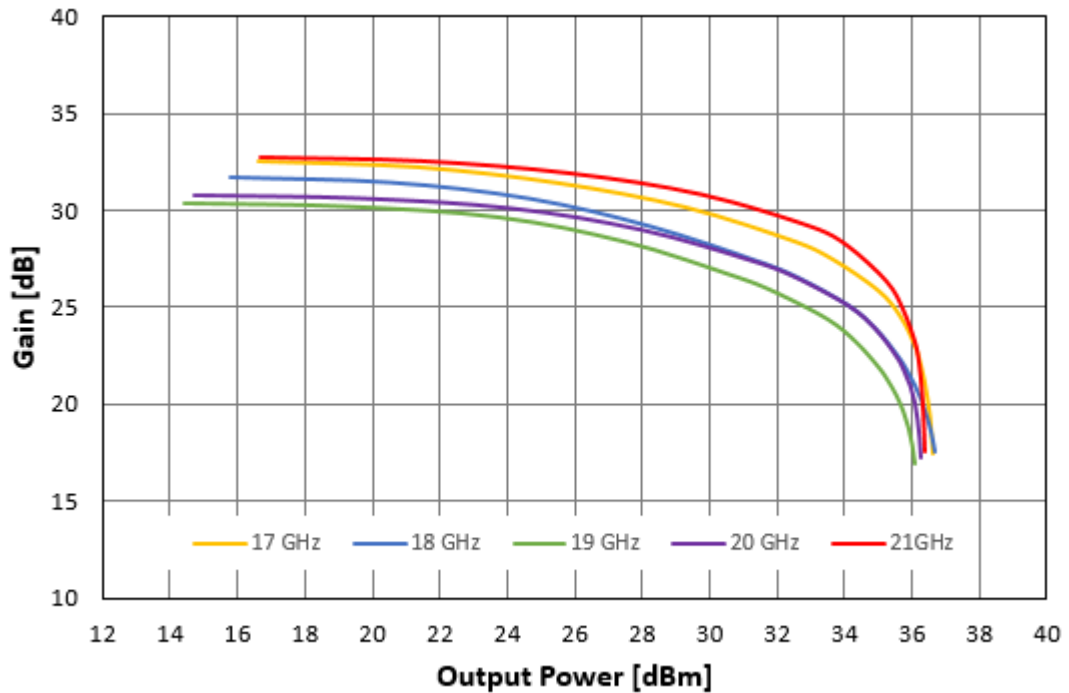
Drain current vs Frequency & temperature



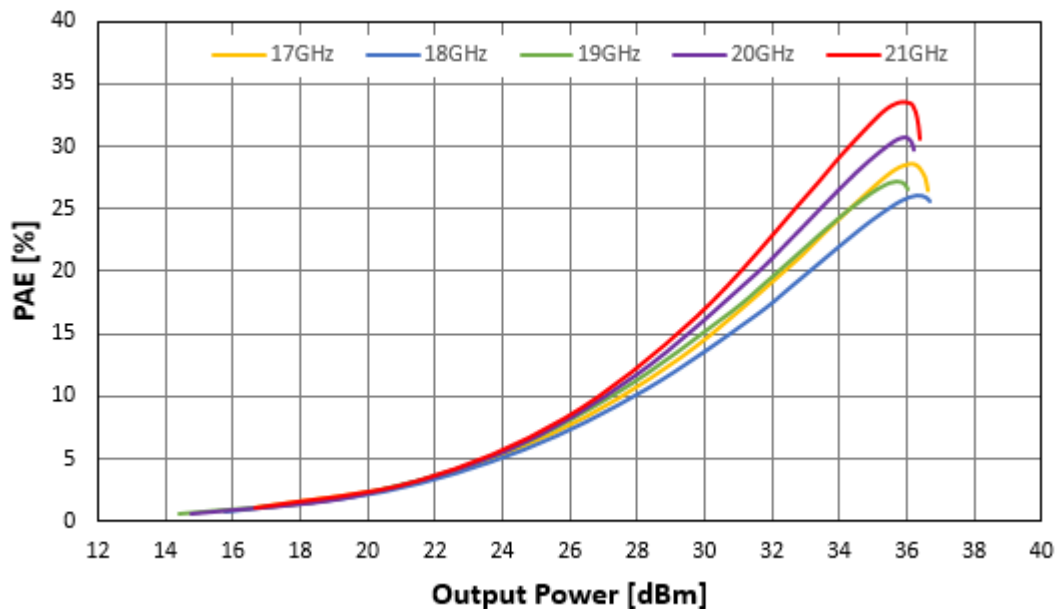
Typical Board Measurements : Non-linear performances

CW measurements: $T_{case}=+25^{\circ}C$, $V_d = +18V$, $I_{dq} = 260mA$ (Adjusted at $T_{case}=25^{\circ}C$).
 Board losses are de-embedded. Measurements are given in the QFN access plan.

Gain versus Output Power & Frequency



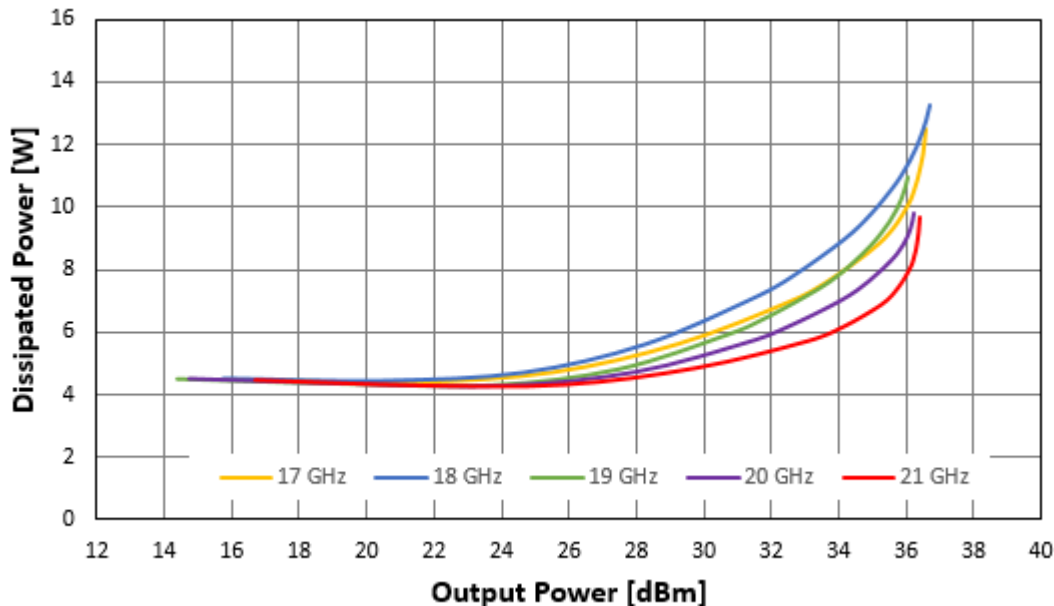
Power Added Efficiency versus Output Power & Frequency



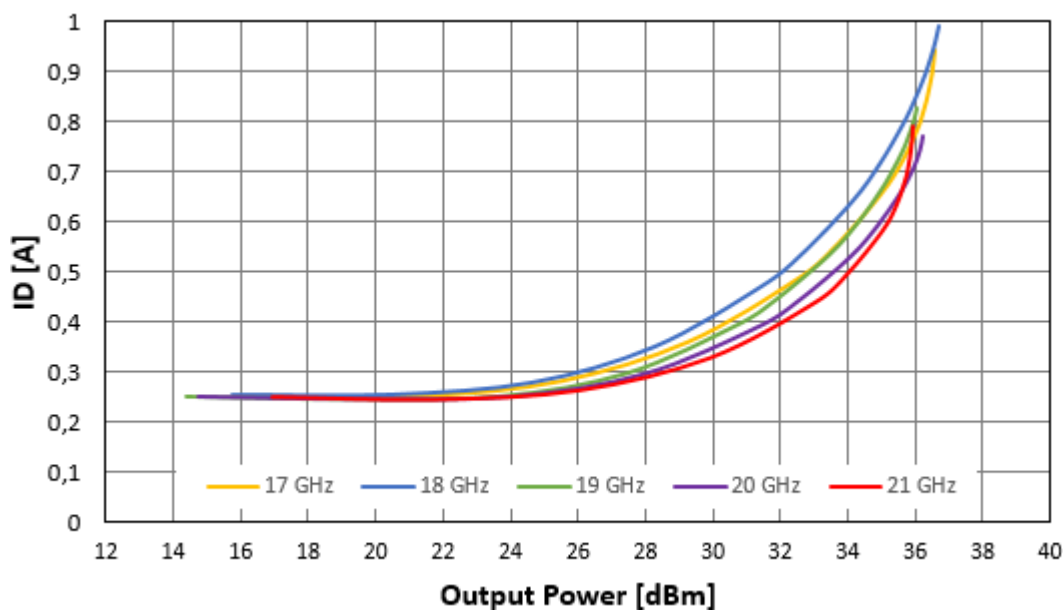
Typical Board Measurements : Non-linear performances

CW measurements: $T_{case}=+25^{\circ}C$, $V_d = +18V$, $I_{dq} = 260mA$ (Adjusted at $T_{case}=25^{\circ}C$).
 Board losses are de-embedded. Measurements are given in the QFN access plan.

Dissipated Power versus Output Power & Frequency



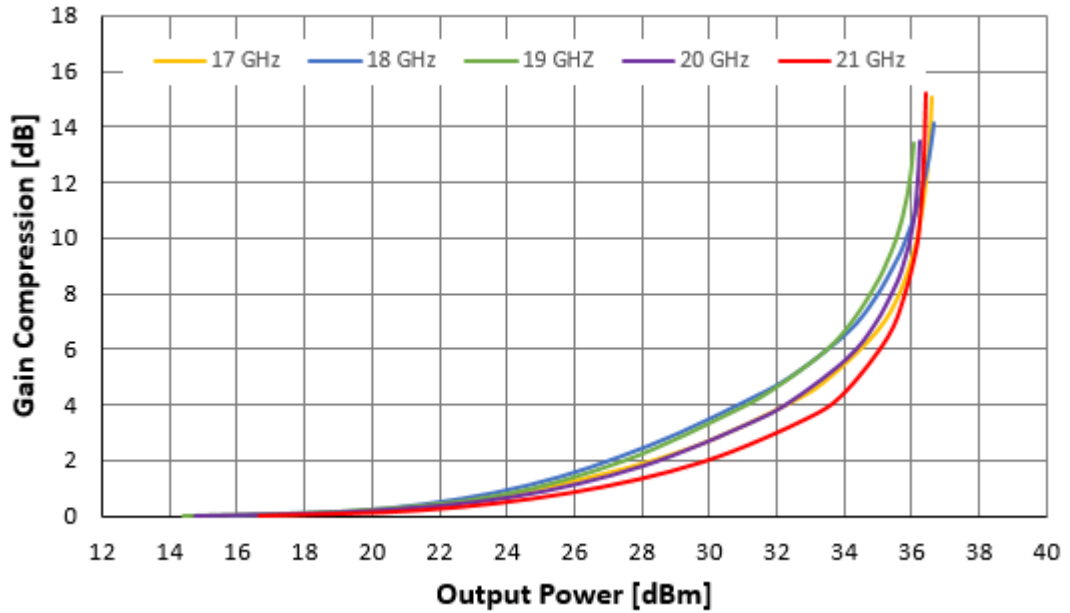
Drain Current versus Output Power & Frequency



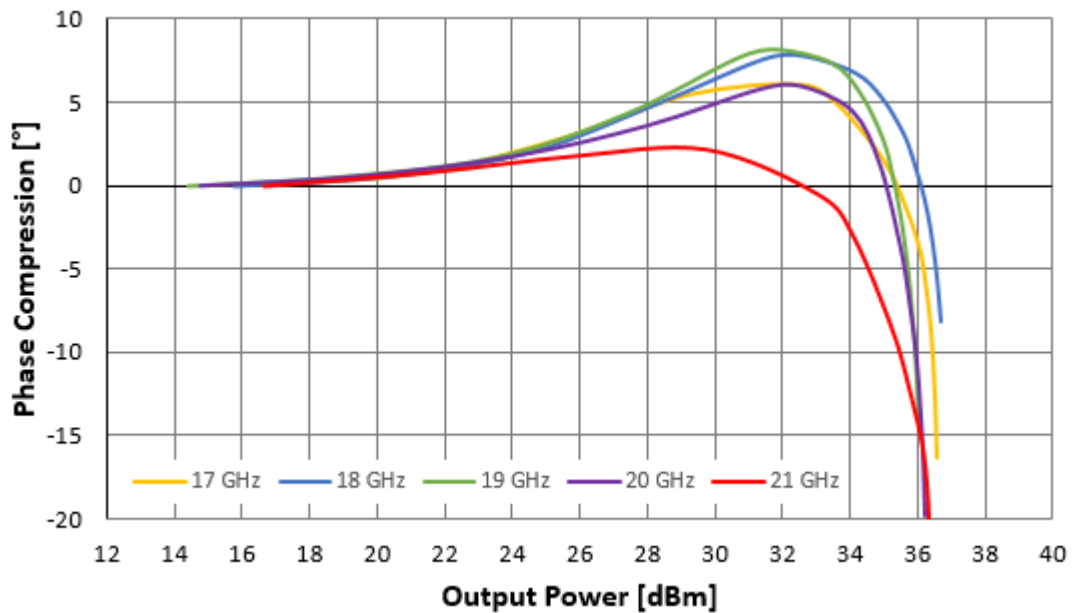
Typical Board Measurements : Non-linear performances

CW measurements: $T_{case}=+25^{\circ}C$, $V_d = +18V$, $I_{dq} = 260mA$ (Adjusted at $T_{case}=25^{\circ}C$).
 Board losses are de-embedded. Measurements are given in the QFN access plan.

Compression versus Output Power & Frequency



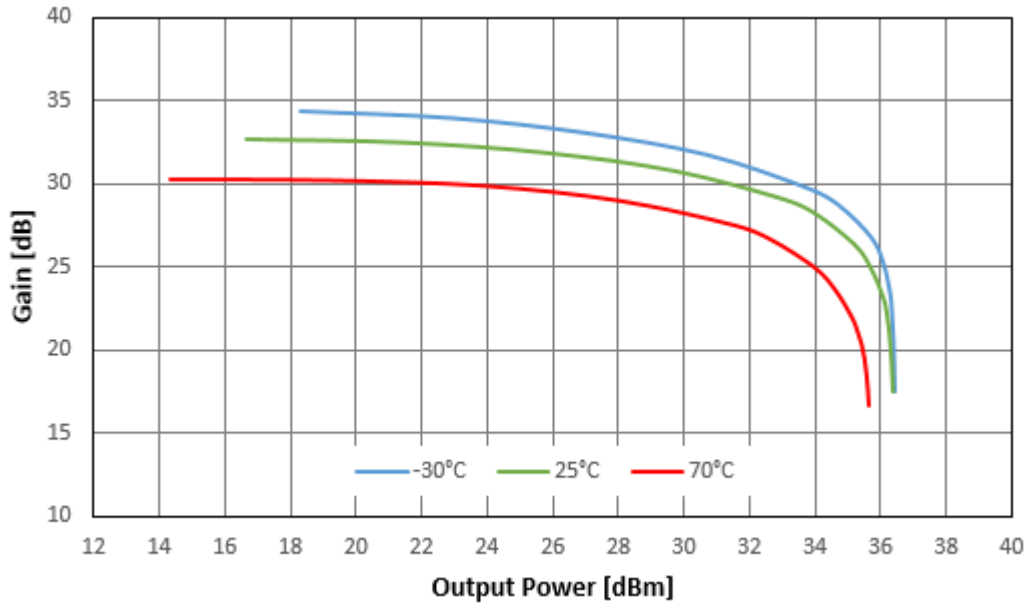
Phase Compression versus Output Power & Frequency



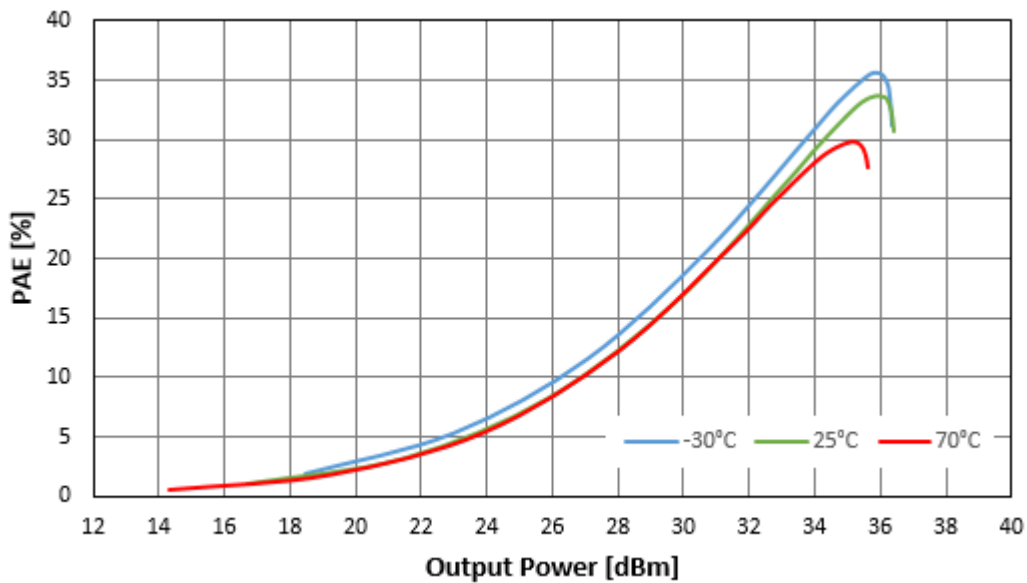
Typical Board Measurements : Non-linear performances

CW measurements: $V_d = +18V$, $I_{dq} = 260mA$ (Adjusted at $T_{case}=25^\circ C$), Frequency=21GHz.
 Board losses are de-embedded. Measurements are given in the QFN access plan.

Gain versus Output Power & Temperature



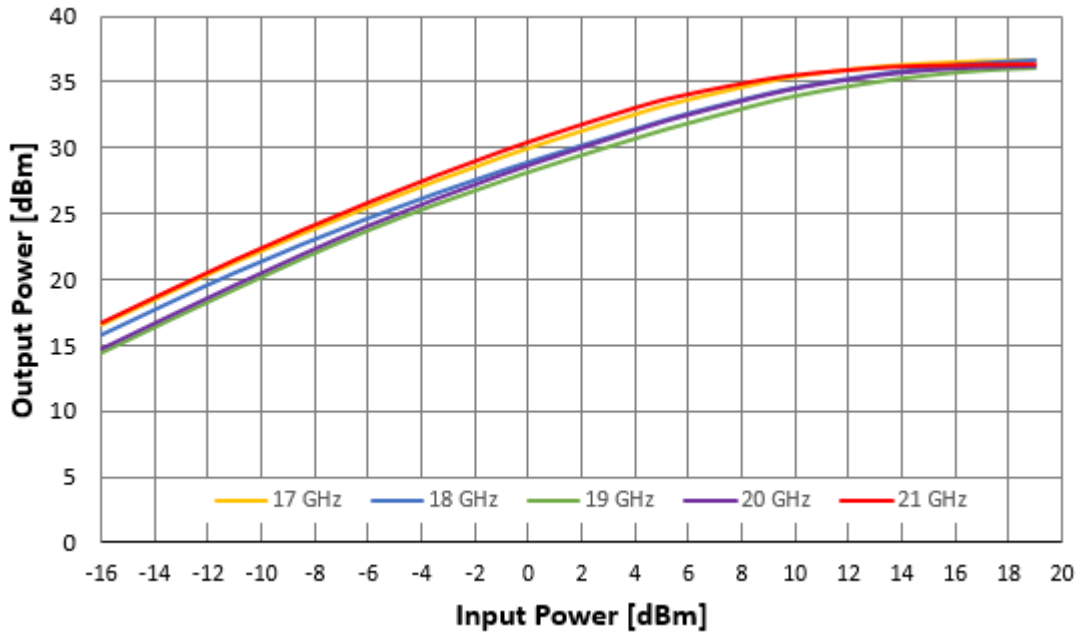
Power Added Efficiency versus Output Power & Temperature



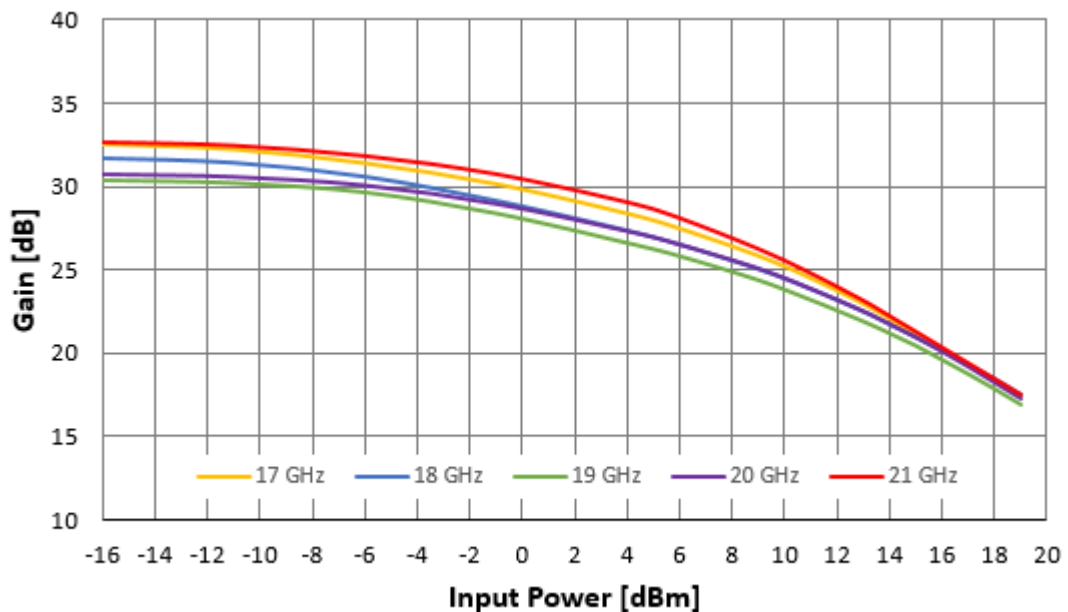
Typical Board Measurements : Non-linear performances

CW measurements: $T_{case}=+25^{\circ}C$, $V_d = +18V$, $I_{dq} = 260mA$ (Adjusted at $T_{case}=25^{\circ}C$).
 Board losses are de-embedded. Measurements are given in the QFN access plan.

Output Power vs Input Power & Frequency



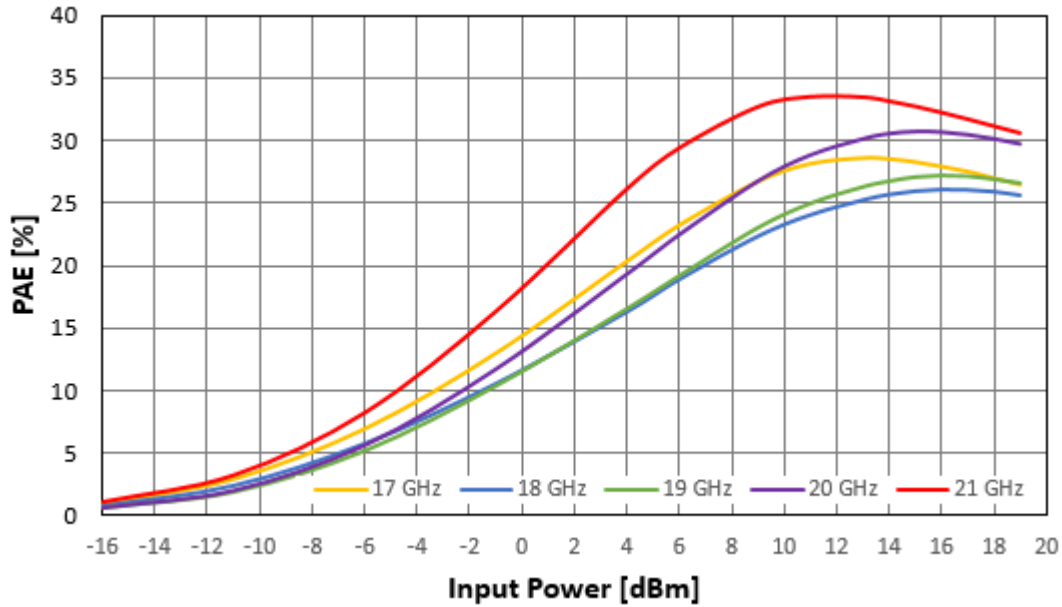
Gain versus Input Power & Frequency



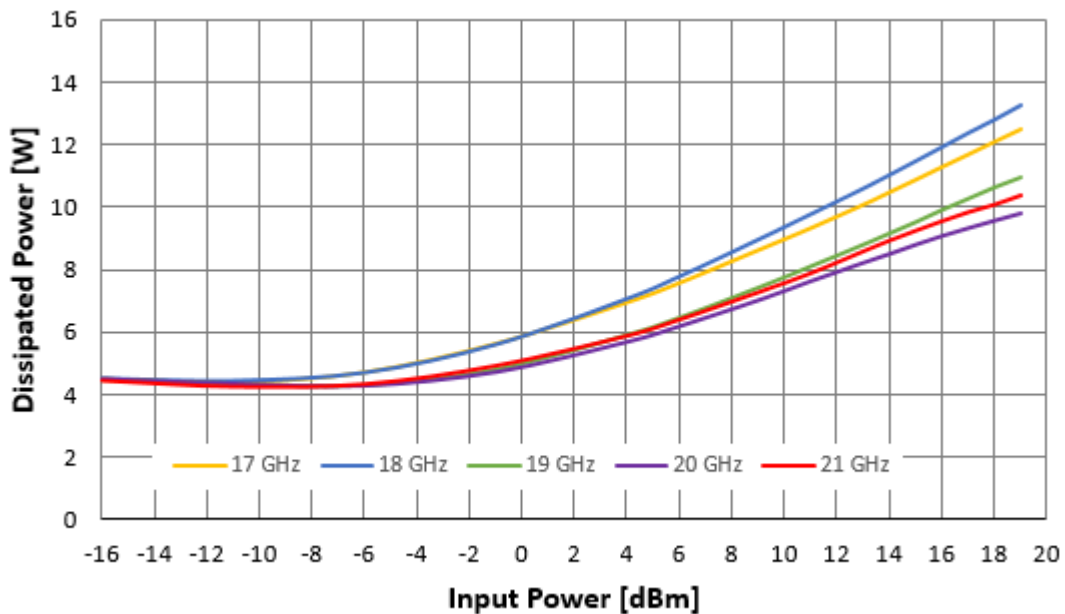
Typical Board Measurements : Non-linear performances

CW measurements: $T_{case}=+25^{\circ}C$, $V_d = +18V$, $I_{dq} = 260mA$ (Adjusted at $T_{case}=25^{\circ}C$).
 Board losses are de-embedded. Measurements are given in the QFN access plan.

Power Added Efficiency vs Input Power & Frequency



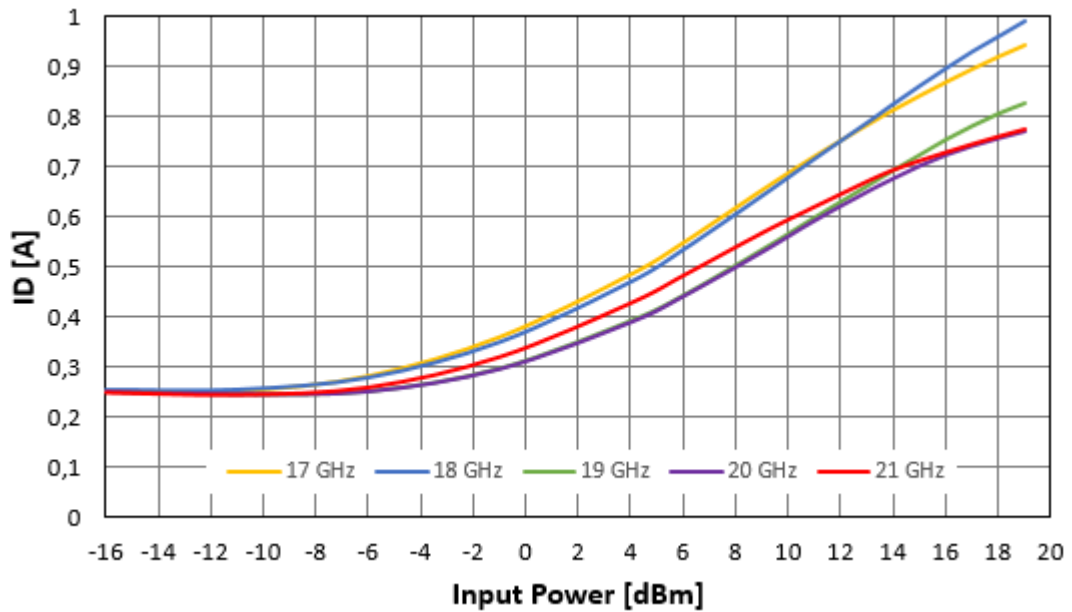
Compression versus Input Power & Frequency



Typical Board Measurements : Non-linear performances

CW measurements: $T_{case}=+25^{\circ}C$, $V_d = +18V$, $I_{dq} = 260mA$ (Adjusted at $T_{case}=25^{\circ}C$).
 Board losses are de-embedded. Measurements are given in the QFN access plan.

Drain Current vs Input Power & Frequency



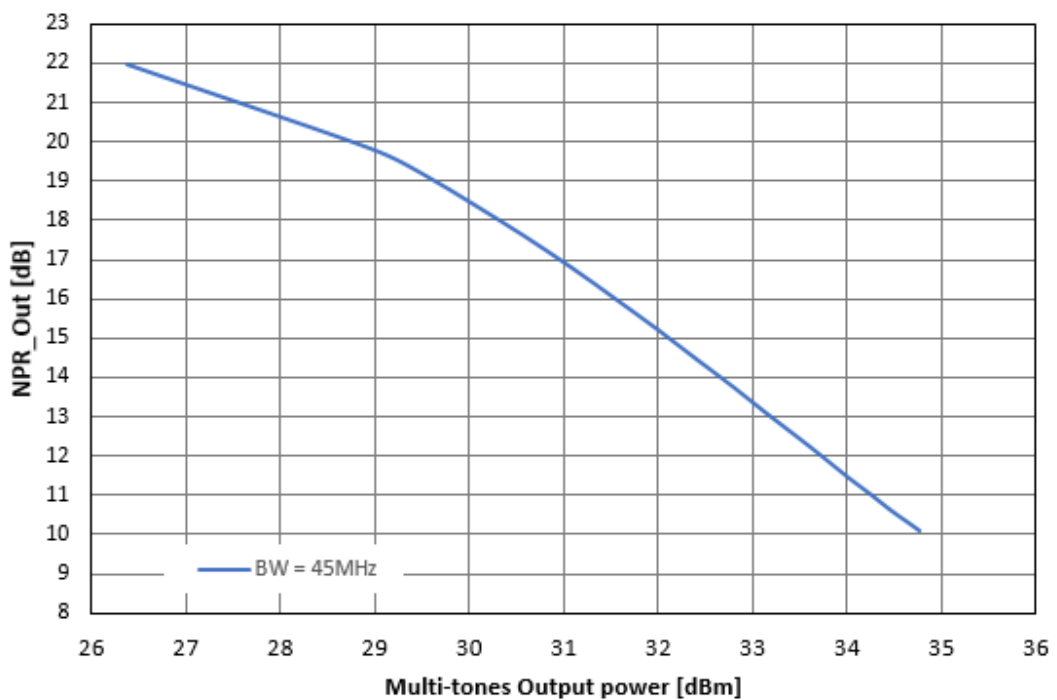
Typical Board Measurements : NPR performances

$T_{case}=+25^{\circ}C$, $V_d = +18V$, $I_{dq} = 260mA$

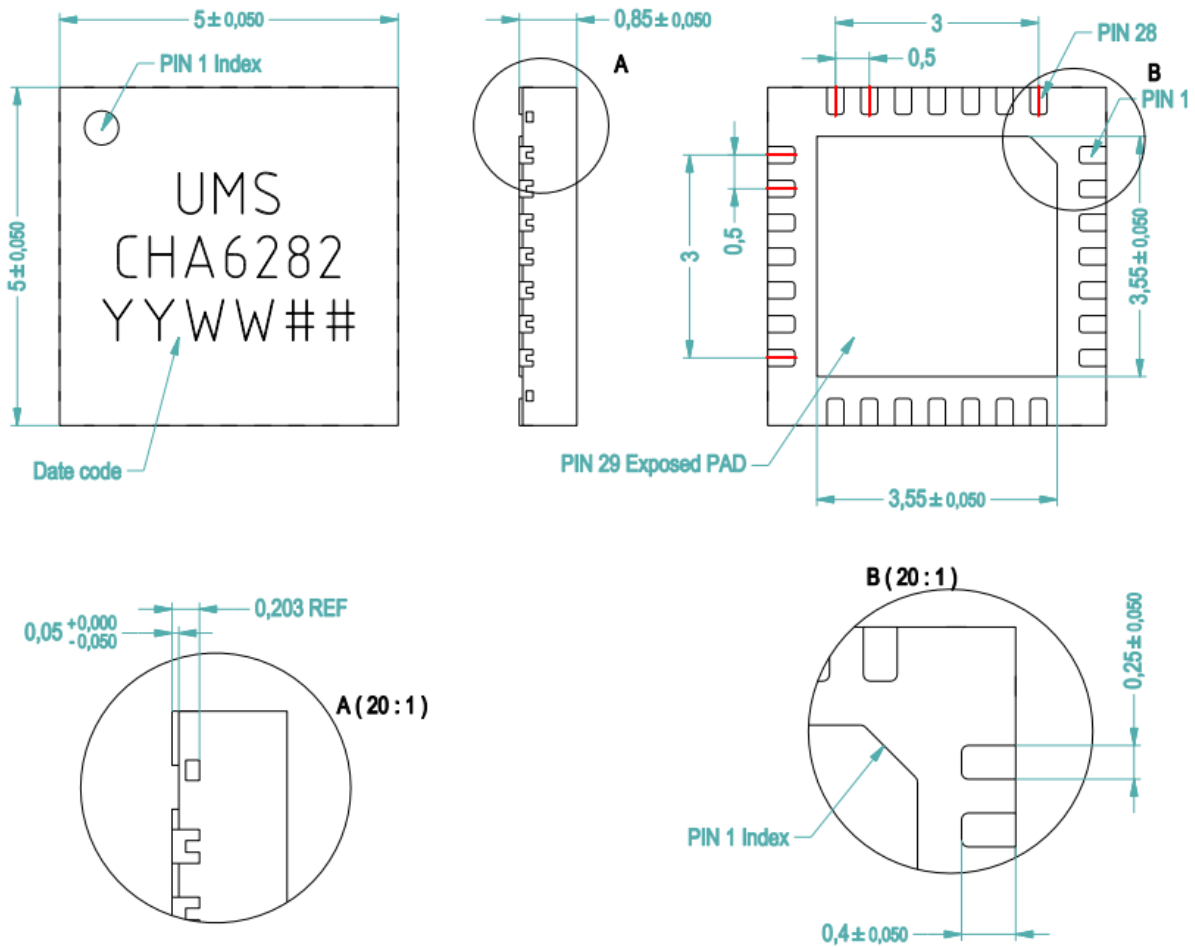
Center Frequency : 19GHz

Measured bandwidth : 45MHz

Notch width : 10%



Package outline ⁽¹⁾



Units : mm
 Finish : NiPdAuAg
 Lead free (Green)



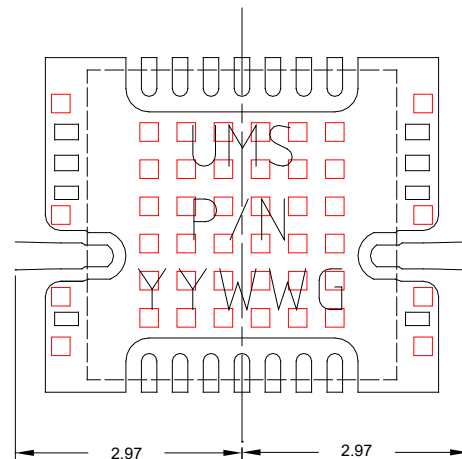
NiPdAuAg, Lead Free (Green)	1- Nc	11- D4	21- Nc
Units : mm	2- Nc	12- G4	22- GND ⁽²⁾
From the standard : JEDEC MO-220	3- GND ⁽²⁾	13- D3	23- D2
(VGGD)	4- RF in	14- GND ⁽²⁾	24- G3
	5- GND ⁽²⁾	15- Nc	25- D1
	6- Nc	16- Nc	26- G2
	7- Nc	17- GND ⁽²⁾	27- GND ⁽²⁾
	8- GND ⁽²⁾	18- RF out	28- G1
	9- Nc	19- GND ⁽²⁾	29- GND ⁽²⁾
	10- D5	20- Nc	

⁽¹⁾ The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (<https://www.ums-rf.com>) for exact package dimensions.

⁽²⁾ It is strongly recommended to ground all pins marked "GND" through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 2.97mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation board recommended in paragraph "Evaluation board".



ESD sensitivity

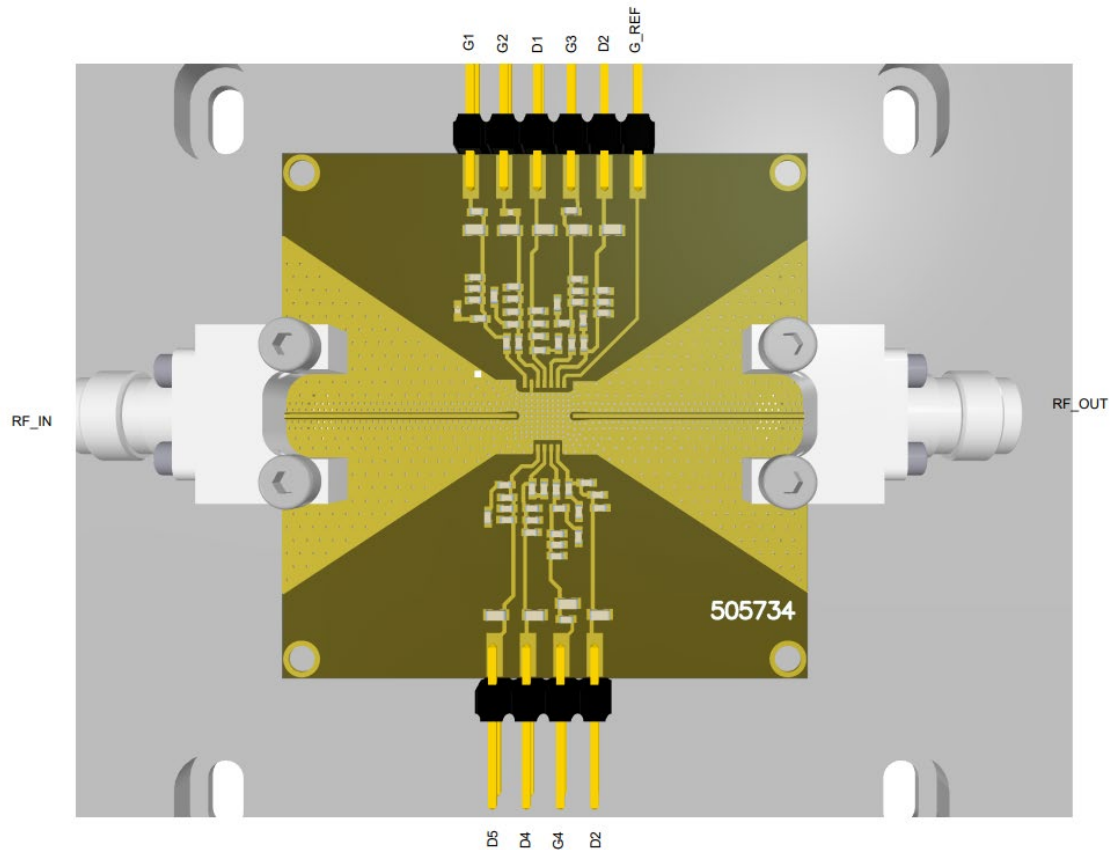
Standard	Value
MIL-STD-1686C	HBM Class 1 (<2000V)
ESD STM5.1-1998	HBM Class 0 (<250V)

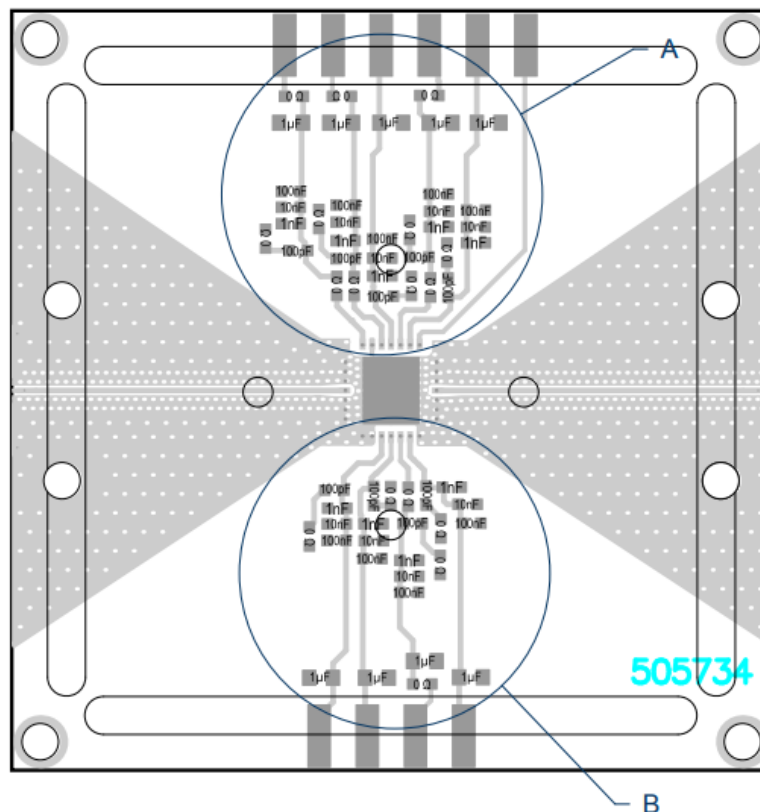
Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% NiPdAuAg
MSL Rating	MSL3

Evaluation board

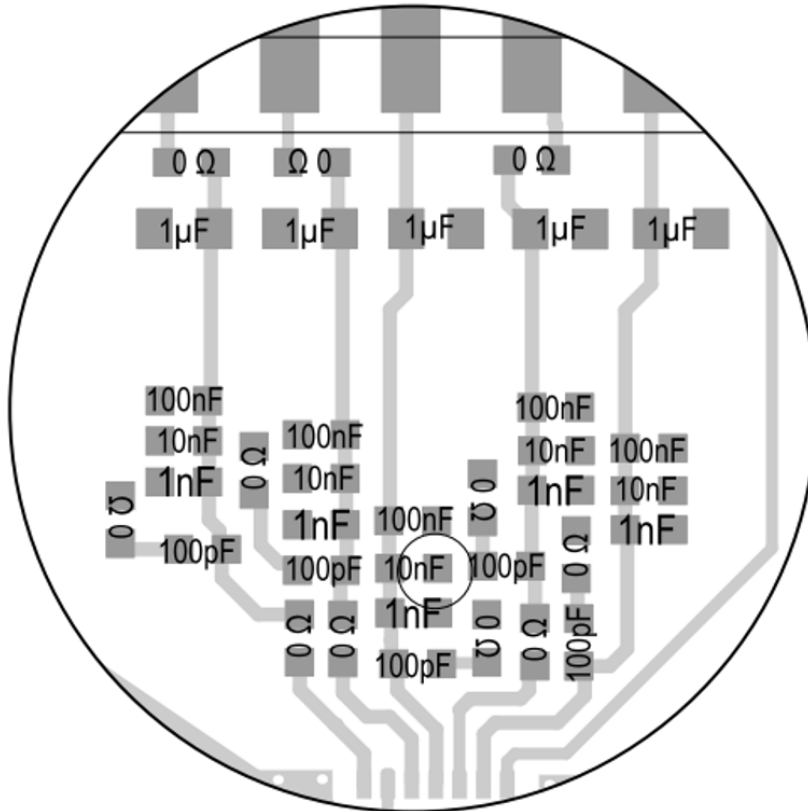
- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 100pF, 1nF, 10nF, 100nF and 1 μ F (\pm 10%) are recommended for all DC accesses.
- See application note AN0017 for details.



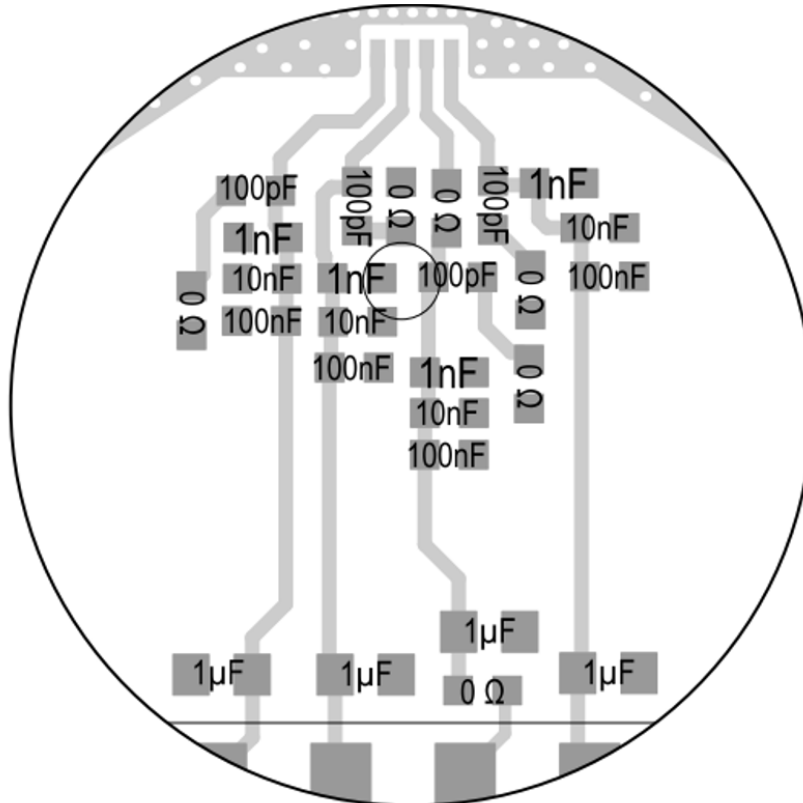


5 levels of decoupling capacitor have been used :
First level of capacitor is 100pF, second level is 1nF, third level 10nF, fourth level 100nF
and fifth level is 1μF

Détail A



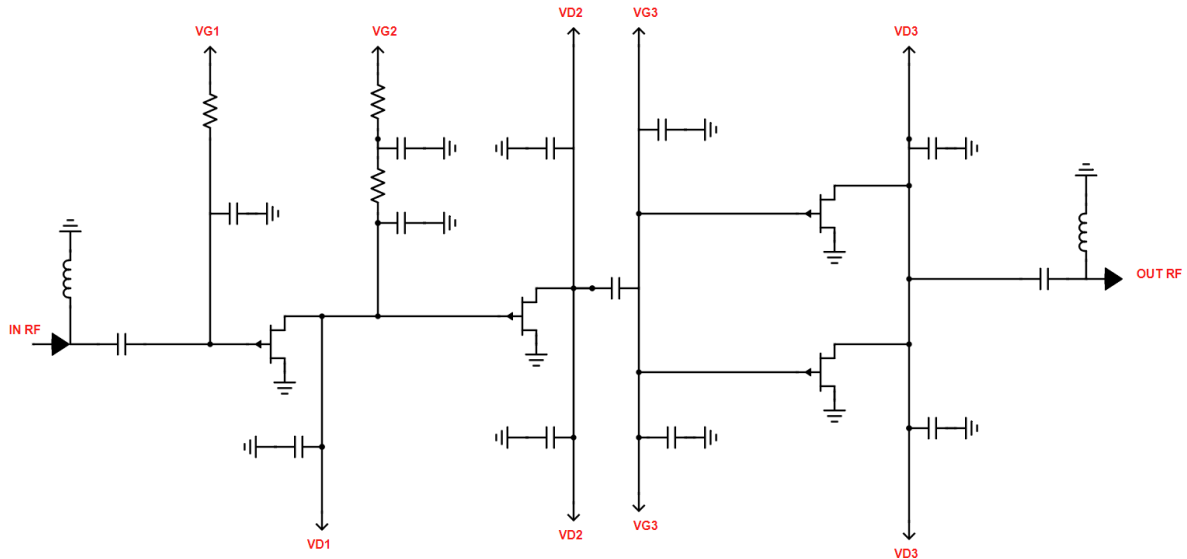
Détail B



Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.

DC Schematic

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.



The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (100pF, 1nF, 10nF, 100nF, 1μF) on the PC board, as close as possible to the package.

Recommended package footprint

Refer to the application note AN0017 available at <https://www.ums-rf.com> for package footprint recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017 at <https://www.ums-rf.com>.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <https://www.ums-rf.com>.

Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 5x5 package:

CHA6282-QCB/XY

Stick: XY = 20

Tape & reel: XY = 21

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