

## 10W K-Band Doherty Power Amplifier

### GaN Monolithic Microwave IC

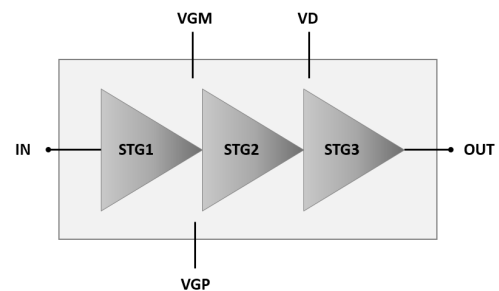
#### Description

The CHA8254-99F is a three-stage GaN Doherty Power Amplifier in the frequency band 17.3-20.3GHz. This DPA typically provides 10W of output power associated to 31% of Power Added Efficiency. Thanks to Doherty architecture, it also provides 27% Power Added Efficiency at 6dB of input back-off. The small signal gain reaches more than 29dB. The overall power supply is 15V/225mA (quiescent current). Thanks to a low drain voltage biasing, the CHA8254-99F provides a junction temperature below 160°C even in saturation.

This circuit is a very versatile amplifier for high performance systems.

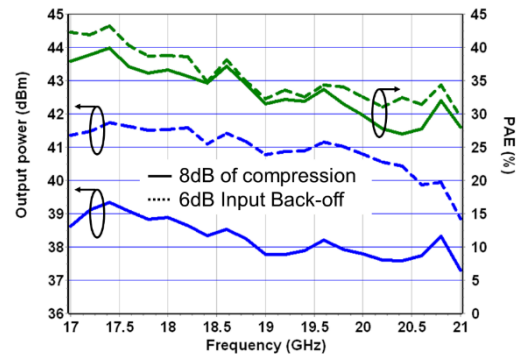
The circuit is firstly dedicated to space applications and well suited for a wide range of microwave applications and systems.

The part is developed on a robust 0.15µm gate length GaN on SiC HEMT process and is available as a bare die.



#### Main Features

- 17.3-20.3 GHz frequency range
- Linear Gain is 29dB
- 40dBm Pout for +20dBm input power
- Associated PAE is more than 31% for +20dBm input power and 27% for +14dBm input power
- DC bias: Vd=15Volts @Idq\_main=210mA @Idq\_peak=15mA
- Chip size : 5x3.6x0.07mm



#### Main Electrical Characteristics

Tb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	17.3		20.3	GHz
Gain	Linear Gain		29		dB
PAE	Power Added Efficiency at 6dB Input Back-off (Pin=14dBm)		27		%
Pout	Output Power (Pin=20dBm)		40		dBm

## Specifications (CW mode)

Tb.= +25°C, Vd = +15V, Idq\_Main (VGM) = 210mA, Idq\_Peak (VGP)=15mA,

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	17.3		20.3	GHz
Gain	Linear Gain		29		dB
Pout	Output Power (Pin = 20dBm)		40		dBm
PAE	Associated Power Added Efficiency (Pin = 20dBm)		31		%
PAE	Power Added Efficiency at 6dB Input Back-Off (Pin = 14dBm)		27		%
Id	Drain current at saturation (Pin = 20dBm)		2.1		A
S11	Input Return Loss		17		dB
S22	Output Return Loss		12		dB
Idq	Quiescent Current		0.225		A
Vd	Drain Voltage		15		V

These values are representative of measurements done in test fixture with a bonding wire of typically 0.25 to 0.3nH.

## Recommended Operating Ratings

Tb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	15V	V
Id_main_stg_1_2_3	1 <sup>st</sup> , 2 <sup>nd</sup> and 3 <sup>rd</sup> stage Main drain current (North) <sup>(2)</sup>	1.1	A
Id_peak_stg_1_2_3	1 <sup>st</sup> , 2 <sup>nd</sup> and 3 <sup>rd</sup> stage Peak drain current (South) <sup>(2)</sup>	1.1	A
Pin	Maximum peak input power overdrive	22	dBm
Tj	Maximum Junction temperature <sup>(1)</sup>	160	°C

<sup>(1)</sup> value is provided for Tb=85°C <sup>(2)</sup> Currents are provided at saturation (with RF signal)

## Absolute Maximum Ratings <sup>(3)</sup>

Tb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	25	V
Id_main_stg_1_2_3	1 <sup>st</sup> , 2 <sup>nd</sup> and 3 <sup>rd</sup> stage Main drain current (North) <sup>(2)</sup>	1.4	A
Id_peak_stg_1_2_3	1 <sup>st</sup> , 2 <sup>nd</sup> and 3 <sup>rd</sup> stage Peak drain current (South) <sup>(2)</sup>	1.4	A
Pin	Maximum peak input power overdrive	25	dBm

<sup>(3)</sup> Operation of this device above anyone of these parameters may cause permanent damage.

**Temperature Range**

Tb	Operating temperature range (chip backside temperature reference)	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

**Typical Bias Conditions**

Tb.= +25°C

Symbol	Pad N°	Parameter	Values	Unit
Vg_main	2,6,10	Gate voltage tuned for Idq ~ 210mA	-3	V
Vg_peak	16,20,24	Gate voltage tuned for Idq ~ 15mA	-3.4	V
Vd	4,8,12,14,18,22	Drain Voltage	15	V

**“Power ON” sequence**

<ol style="list-style-type: none"> <li>1. Bias HPA gate voltages at Vg close to Vpinch-off (example: Vg_main=Vg_peak≈ -5V).</li> <li>2. Apply Vd bias voltage (example: Vd = 15V).</li> <li>3. Increase slowly Vg_main up to quiescent bias drain current Ids0 (applied on the gate: 210mA).</li> <li>4. Increase slowly Vg_peak up to quiescent bias drain current Ids0 (applied on the gate: 15mA).</li> <li>5. Apply RF signal</li> </ol>
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**“Power OFF” sequence**

<ol style="list-style-type: none"> <li>1. Turn off RF signal</li> <li>2. Bias HPA gate voltages at Vg close to Vpinch-off (example: Vg_main=Vg_peak≈ -5V).</li> <li>3. Set Vd to 0V.</li> <li>4. Turn off Vd supply.</li> <li>5. Turn off Vg supply.</li> </ol>
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## Device thermal information

The device thermal performances below are based on UMS rules to evaluate the junction temperature.

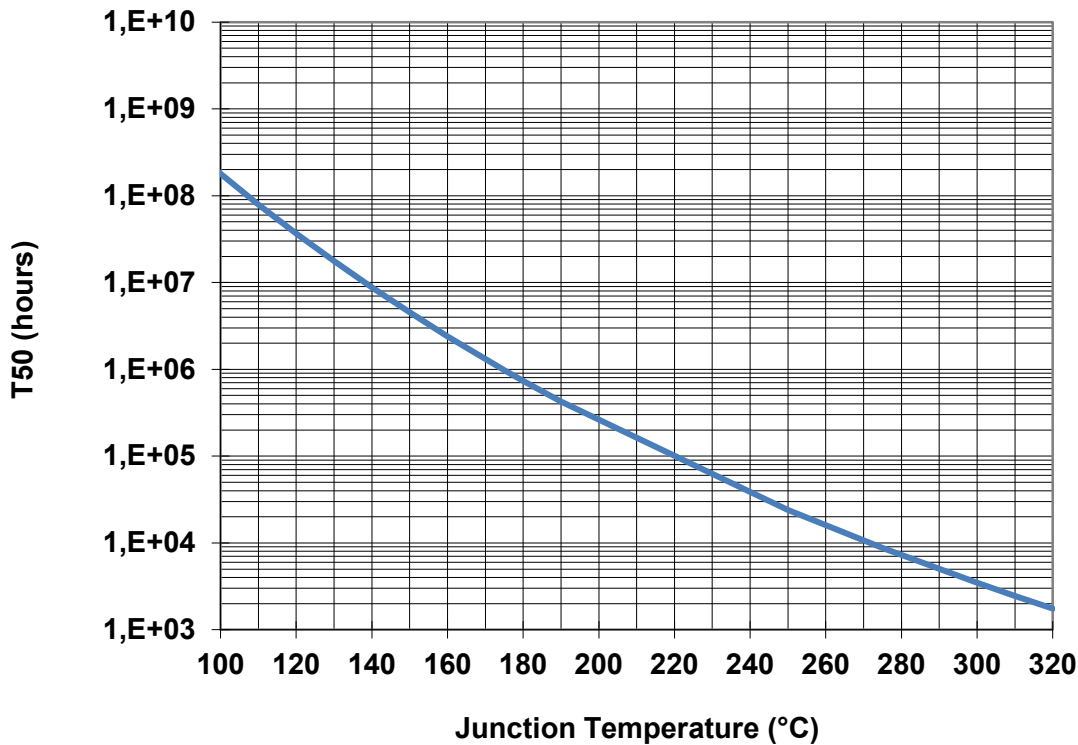
This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHA8254-99F is manufactured (GaN HEMT 0.15µm).

The temperature  $T_{b_{chip}}$  is defined as the chip backside temperature. The thermal resistance ( $R_{th\_eq}$ ), given in the following table, is for the full circuit in CW mode.

Thermal Resistance <sup>(1)</sup>	$R_{th\_eq}$	$T_{b_{chip}} = 85^{\circ}\text{C}$ , $V_d = 15\text{V}$ , $I_{d\_drive} = 1.1\text{A}$ $P_{in} = 14\text{dBm}$ , $P_{out} = 37\text{dBm}$ $P_{diss} = 13\text{W CW}$	2.6	$^{\circ}\text{C/W}$
Junction Temperature	$T_j$		120	$^{\circ}\text{C}$
Median Life	T50		3.5E07	Hrs

<sup>(1)</sup> Thermal resistance measured at the back of the chip

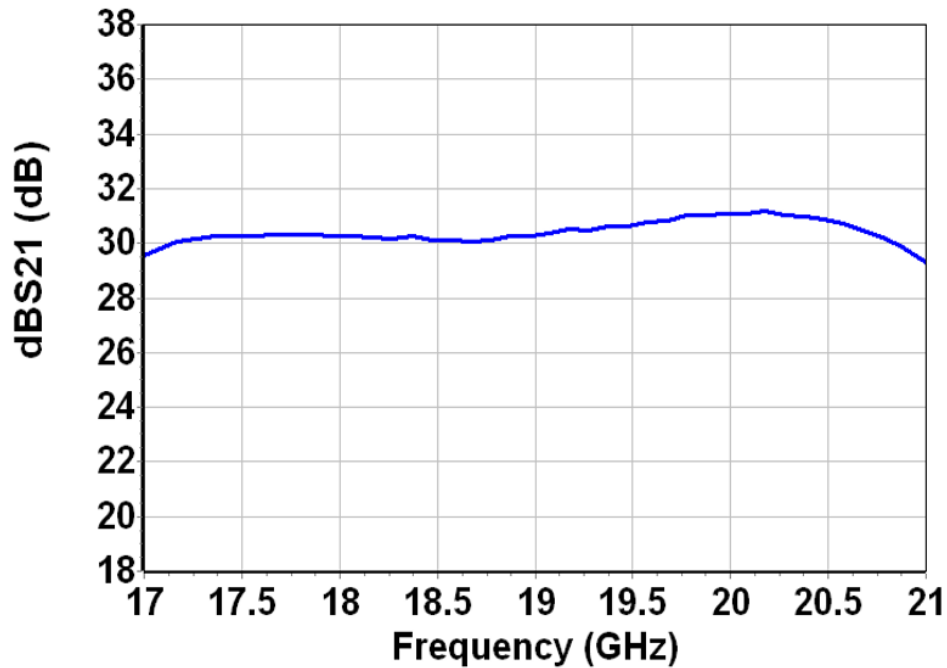
## Median Life Time versus Junction Temperature



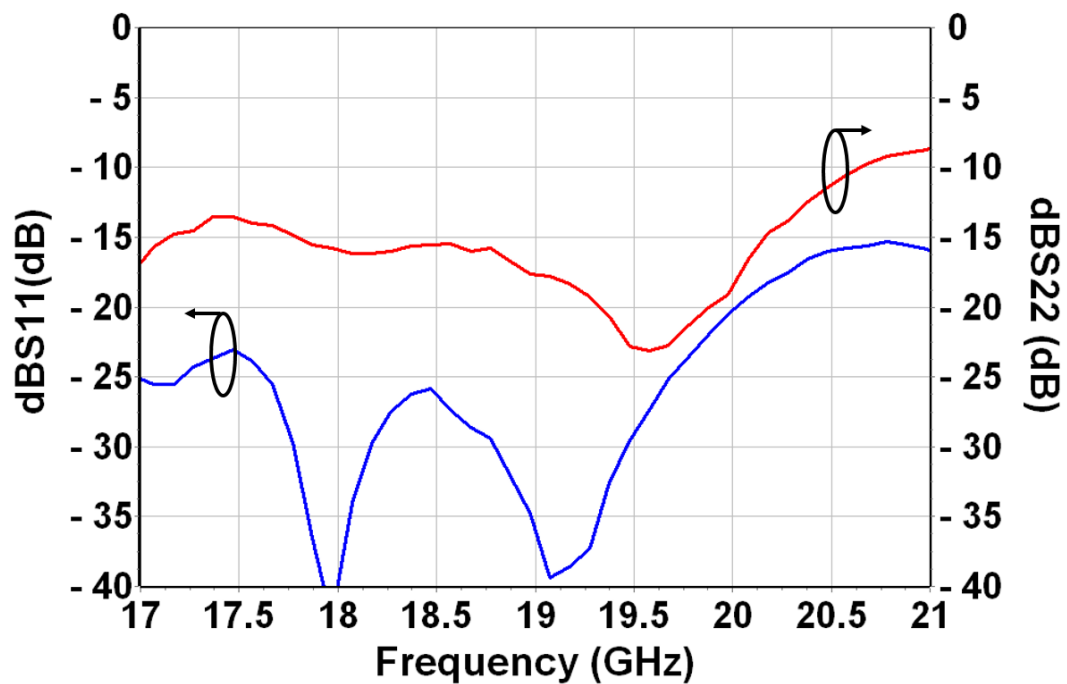
**Typical Test Fixture Measurements: Small Signal Performances**

CW measurements:  $T_b = 25^\circ\text{C}$ ,  $V_d = +15\text{V}$ ,  $I_{dq\_Main} \text{ (VGM)} = 210\text{mA}$ ,  $I_{dq\_Peak} \text{ (VGP)} = 15\text{mA}$

**Linear Gain versus Frequency**



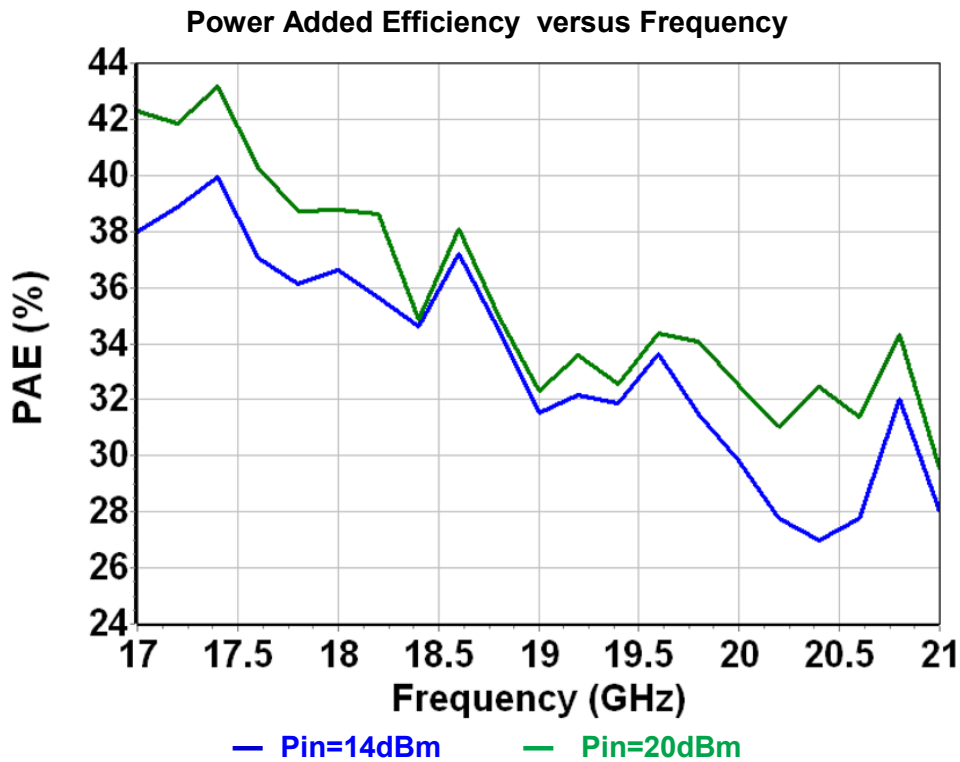
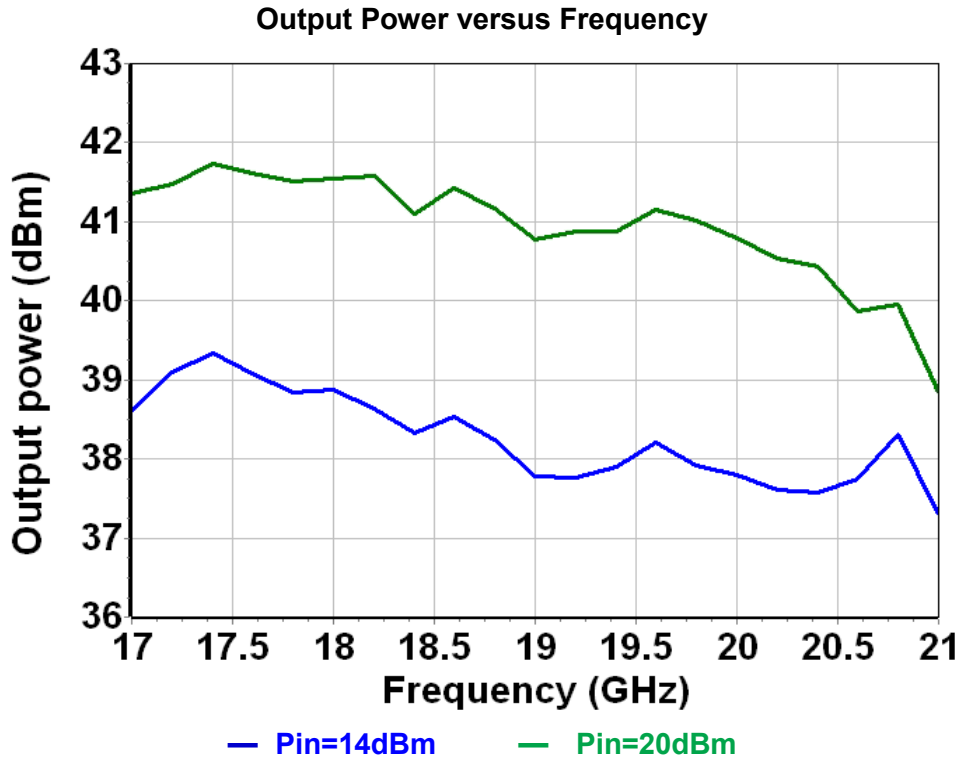
**Input and Output Return Loss versus Frequency**



## Typical Test Fixture Measurements: Non-linear performances

CW measurements:  $T_b = 25^\circ\text{C}$ ,  $V_d = +15\text{V}$ ,  $I_{dq\_Main} (VGM) = 210\text{mA}$ ,  $I_{dq\_Peak} (VGP) = 15\text{mA}$

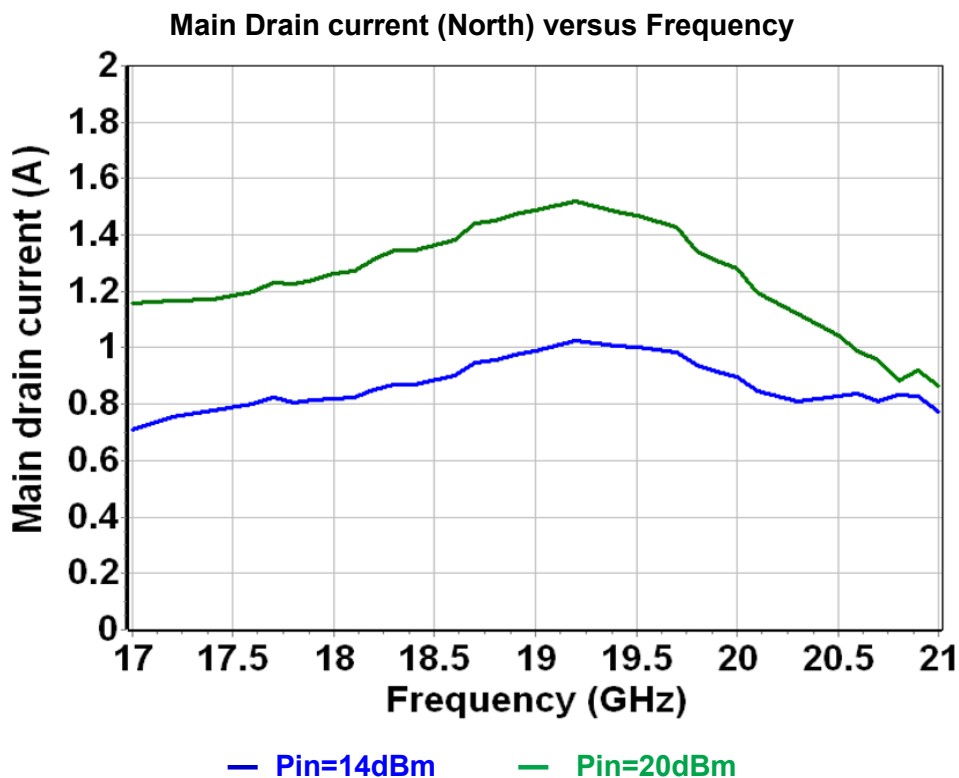
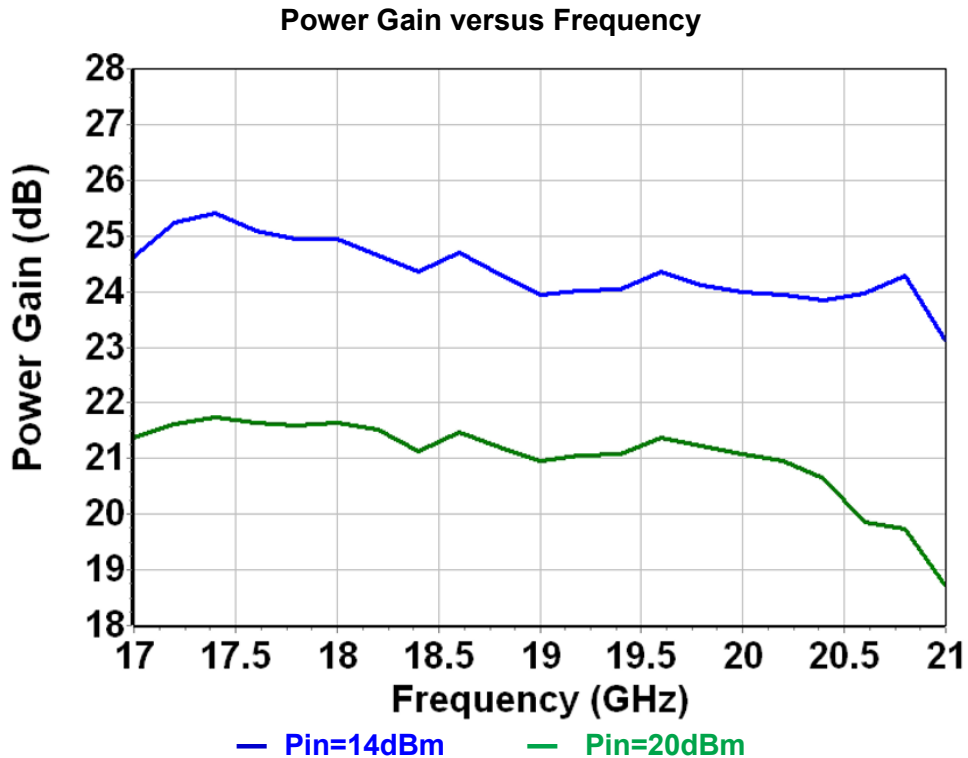
Pin range : -15 to 20 dBm, Frequency range: 17-21 GHz step 0.2 GHz



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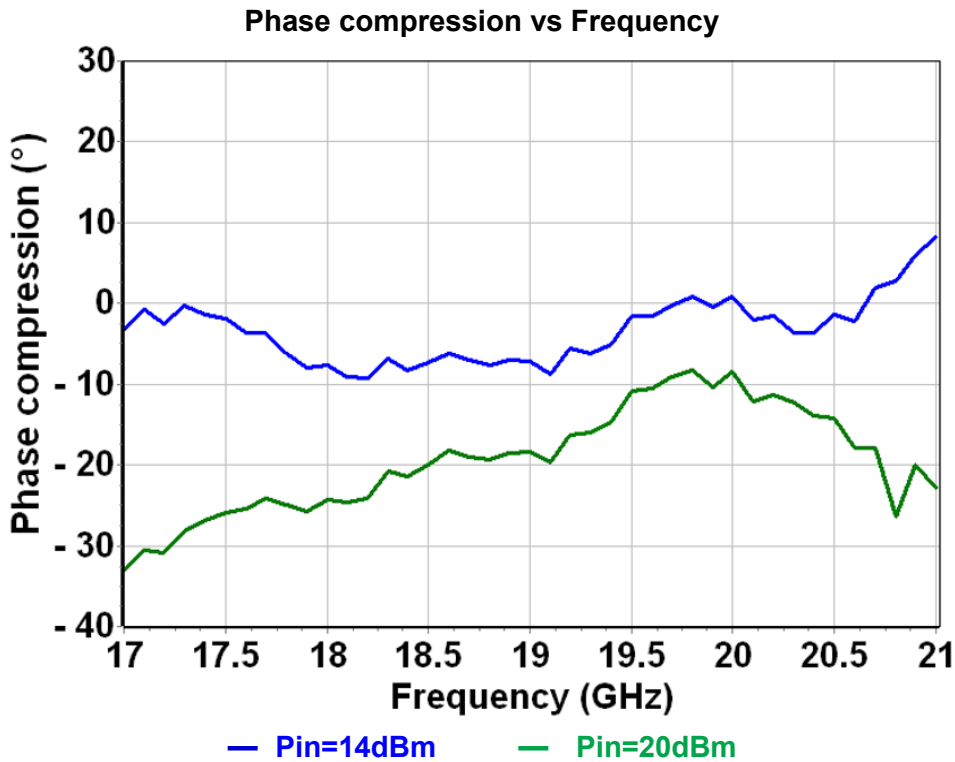
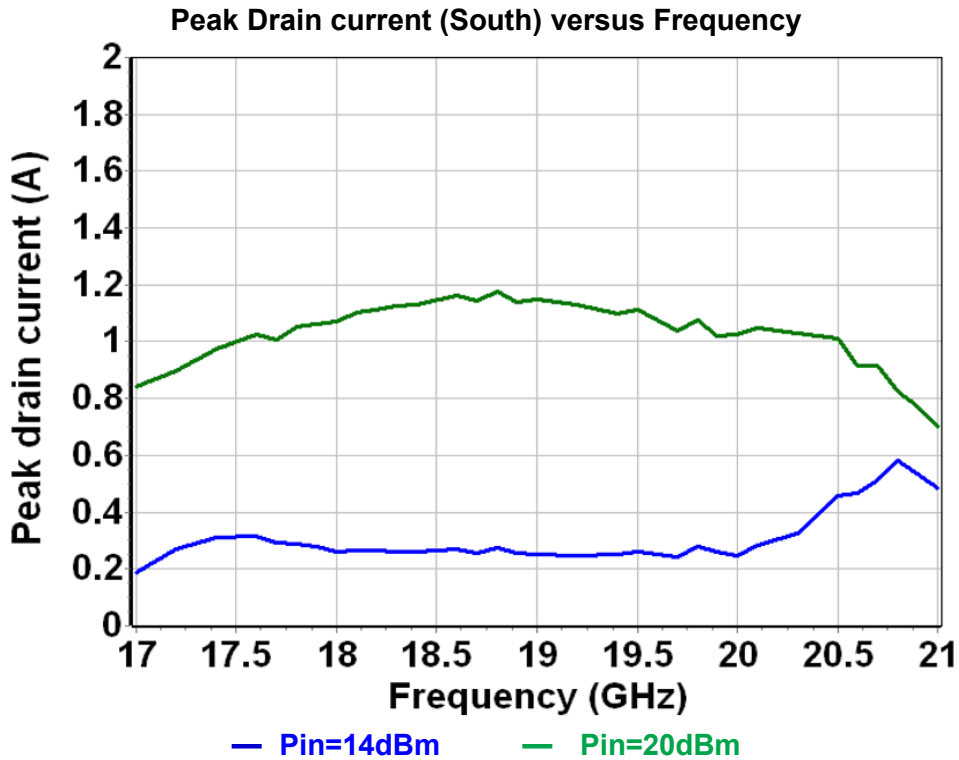
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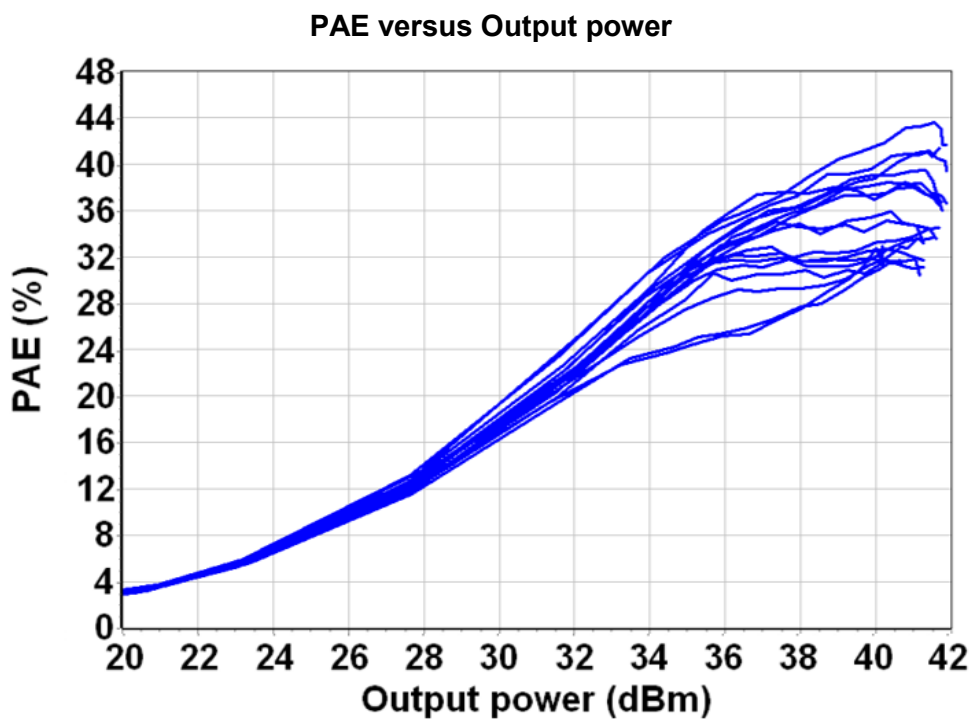
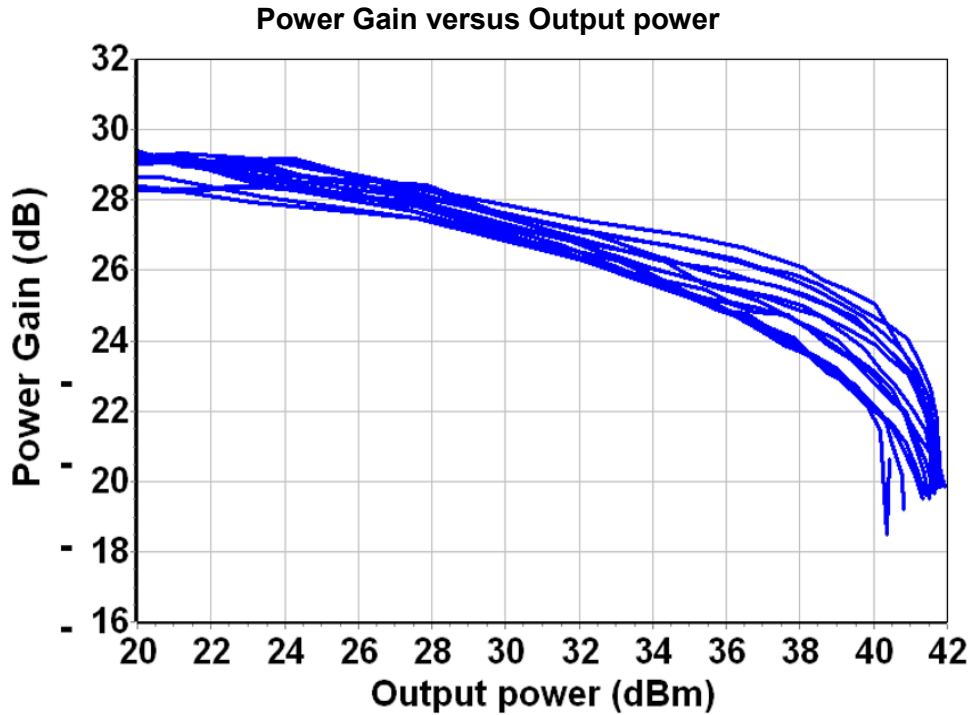




**Typical Test Fixture Measurements: Non-linear Performances**

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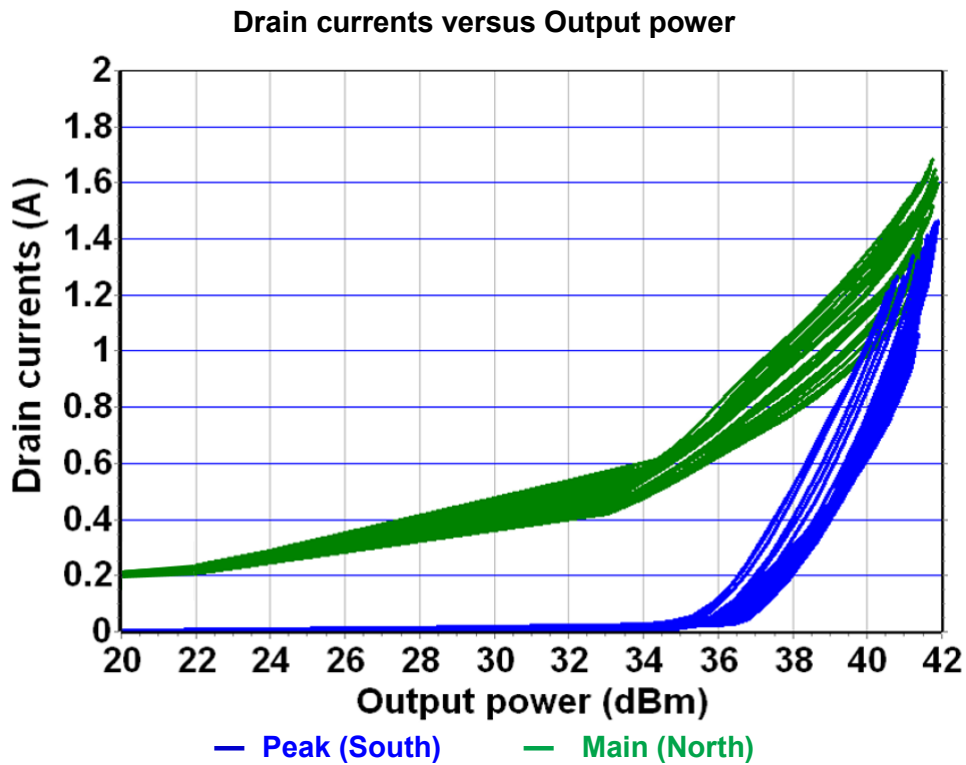
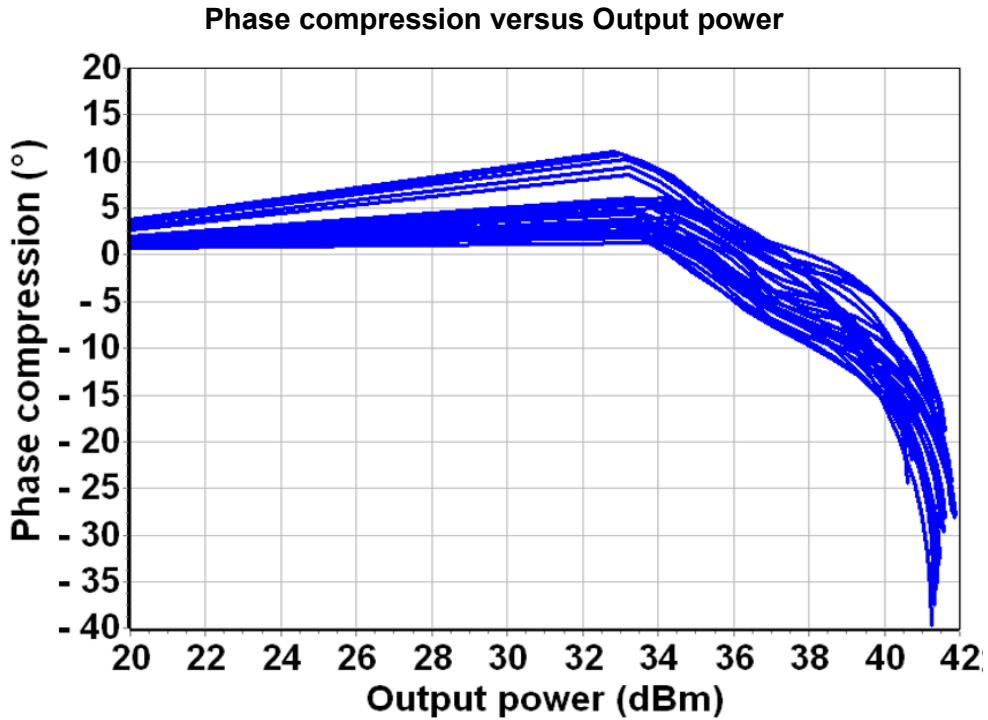
Pin range : -15 to 20 dBm, Frequency range: 17.2-20.4 GHz step 0.2 GHz



**Typical Test Fixture Measurements: Non-linear Performances**

CW measurements:  $T_b = 25^\circ\text{C}$ ,  $V_d = +15\text{V}$ ,  $I_{dq\_Main} (VGM) = 210\text{mA}$ ,  $I_{dq\_Peak} (VGP) = 15\text{mA}$

Pin range : -15 to 20 dBm, Frequency range: 17.2-20.4 GHz step 0.2 GHz

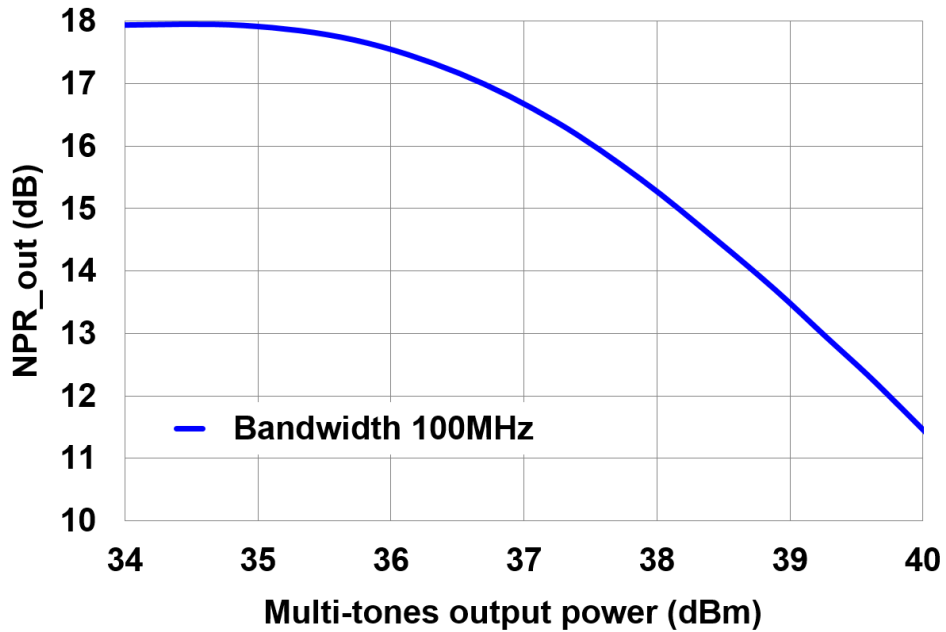


**Typical Test Fixture Measurements: NPR Performances**

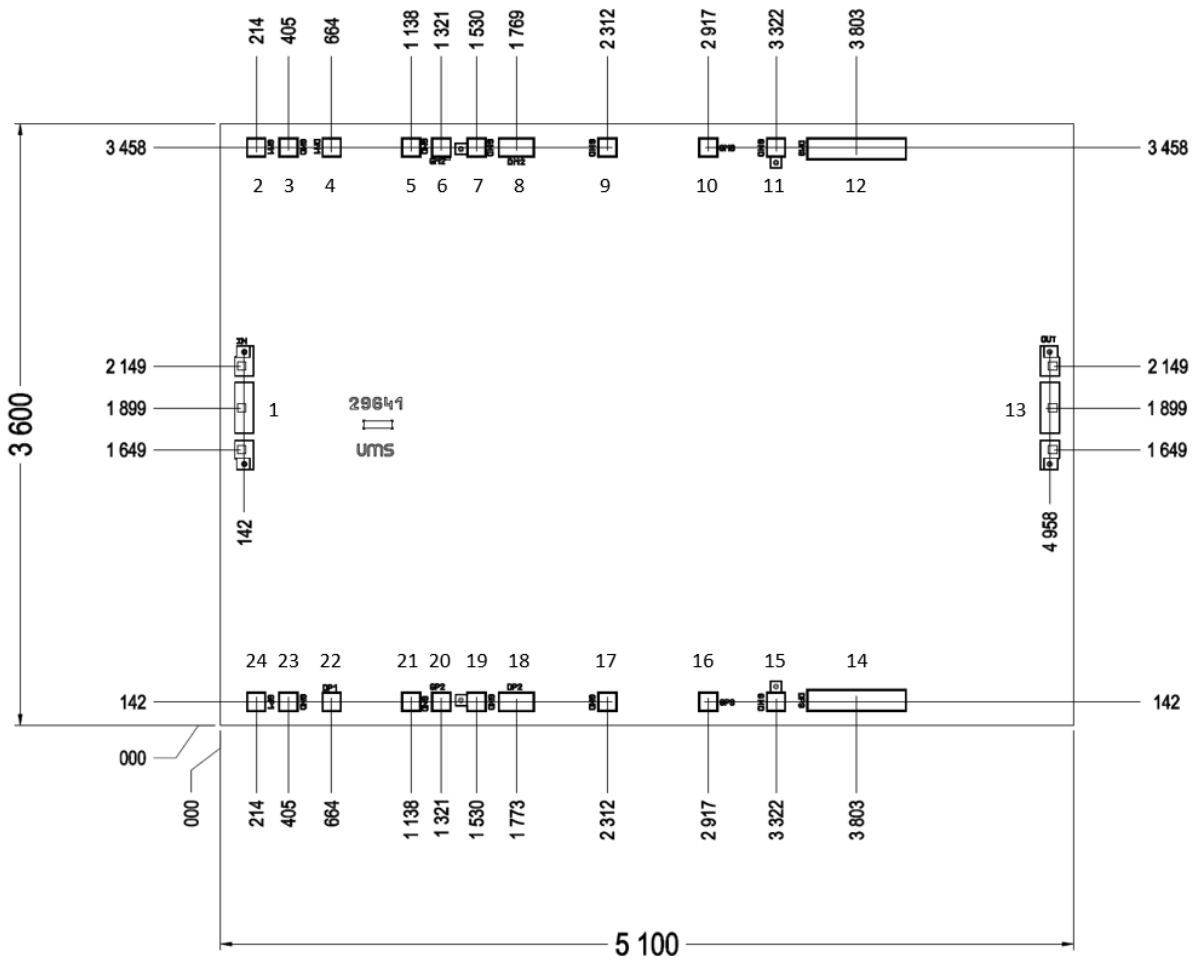
CW measurements:  $T_b = 25^{\circ}\text{C}$ ,  $V_d = +15\text{V}$ ,  $I_{dq\_Main} \text{ (VGM)} = 210\text{mA}$ ,  $I_{dq\_Peak} \text{ (VGP)} = 15\text{mA}$

Frequency carrier point : 18.75GHz, Instantaneous bandwidth : 100MHz, Noise width : 4%

**NPR\_out versus Two-tones output power**



## Chip Mechanical data



All dimensions are in micrometres.

Chip size = 5000x3600 ±50μm

Chip thickness = 70μm ±10μm

Chip width and length are given with a tolerance of ±50μm

RF pads (1, 13) = 308 x 118μm<sup>2</sup>

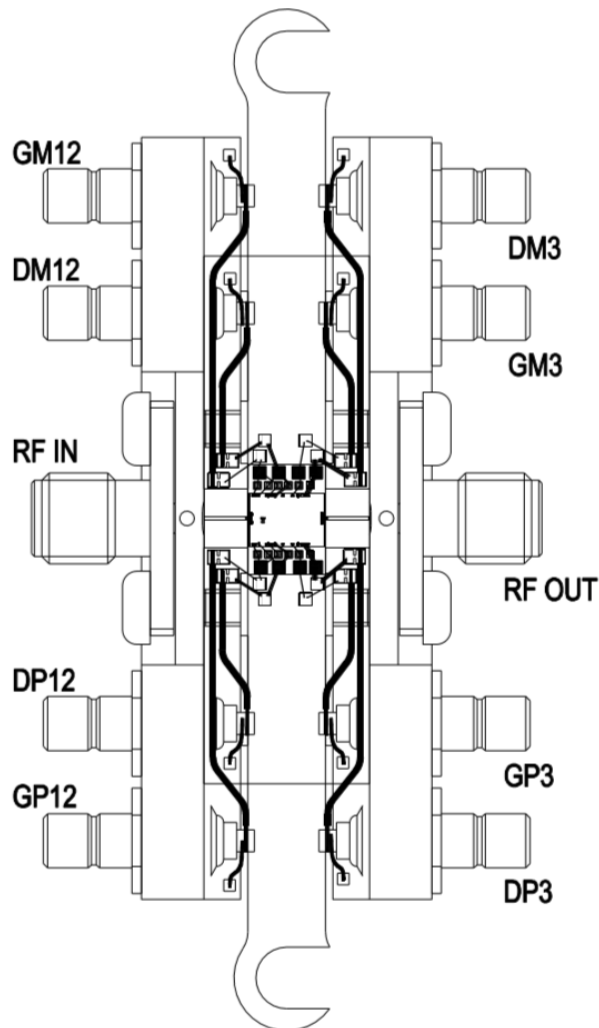
DC pads (2, 3, 4, 5, 7, 9, 10, 11, 15, 16, 17, 19, 20, 21, 22, 23, 24) = 118 x 118μm<sup>2</sup>

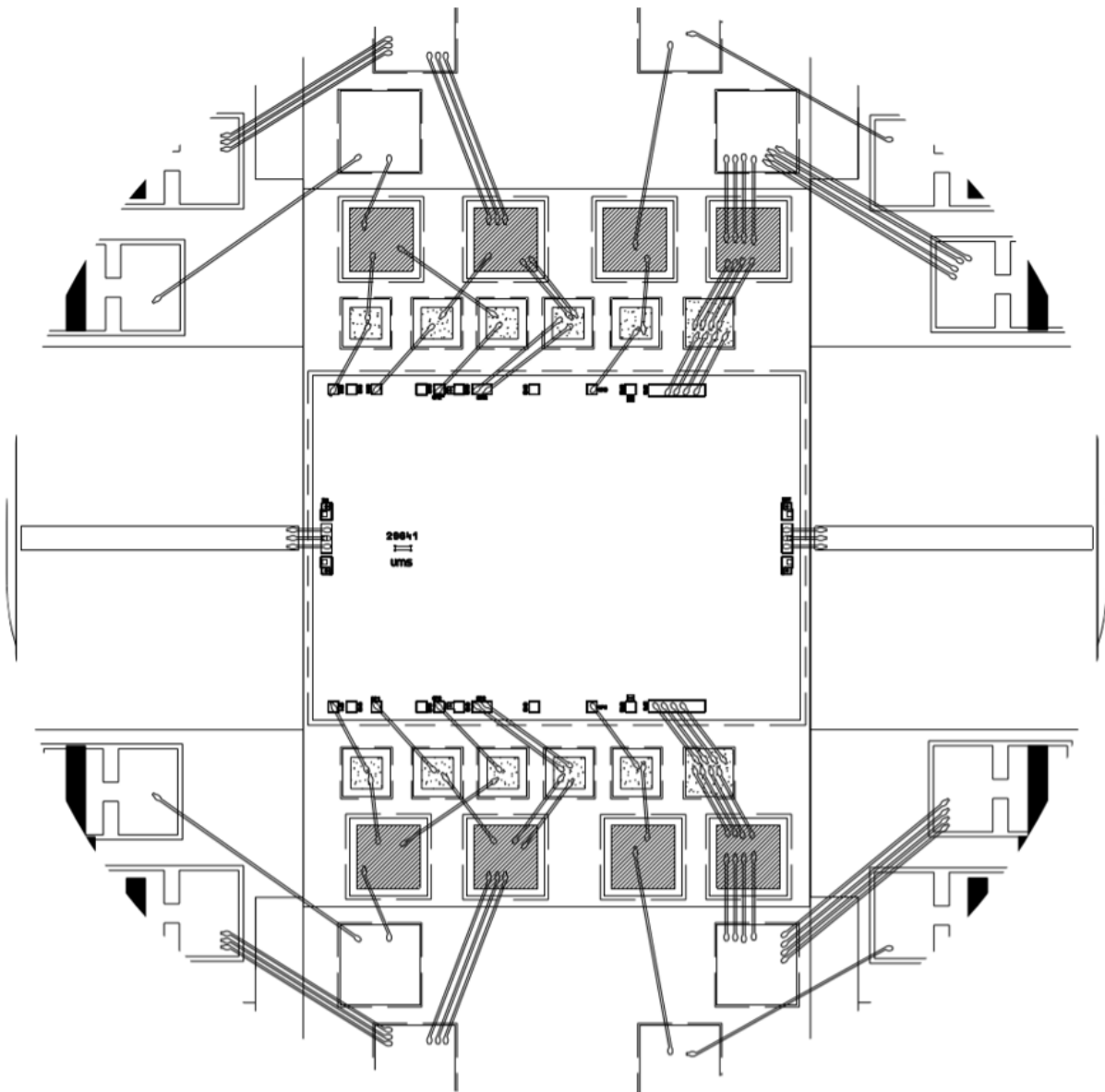
DC pads (8, 18) = 218 x 118μm<sup>2</sup>

DC pads (12, 14) = 600 x 134μm<sup>2</sup>

PAD Number	Name	Description
1	IN	RF input
3, 5, 7, 9, 11, 15, 17, 19, 21, 23	GND	Ground (Not connected)
2	GM1	Main gate voltage of 1 <sup>st</sup> stage
24	GP1	Peak gate voltage of 1 <sup>st</sup> stage
6	GM2	Main gate voltage of 2 <sup>nd</sup> stage
20	GP2	Peak gate voltage of 2 <sup>nd</sup> stage
10	GM3	Main gate voltage of 3 <sup>rd</sup> stage
16	GP3	Peak gate voltage of 3 <sup>rd</sup> stage
4	DM1	Main drain voltage of 1 <sup>st</sup> stage
22	DP1	Peak drain voltage of 1 <sup>st</sup> stage
8	DM2	Main drain voltage of 2 <sup>nd</sup> stage
18	DP2	Peak drain voltage of 2 <sup>nd</sup> stage
12	DM3	Main drain voltage of 3 <sup>rd</sup> stage
14	DP3	Peak drain voltage of 3 <sup>rd</sup> stage
13	OUT	RF output

**Recommended Test Jig**



**Recommended assembly plan**

4 levels of decoupling capacitor have been used:

First level of capacitor is 120pF, second level is 1nF, third level is 10nF and fourth level is 1 $\mu$ F. Only 120pF, 1nF and 10nF capacitors could be seen on the previous assembly drawing (close to the chip).

Note: Supply feed should be bypassed. 25 $\mu$ m diameter gold wire is to be preferred.

**Notes:**

## Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations for the UMS products.

## Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <https://www.ums-rf.com>.

## Recommended reflow process assembly

Refer to the application note AN0001 available at <https://www.ums-rf.com> for die attach.

## Ordering Information

Chip form:

CHA8254-99F/00

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