

10W K-Band High Power Amplifier

GaN Monolithic Microwave IC

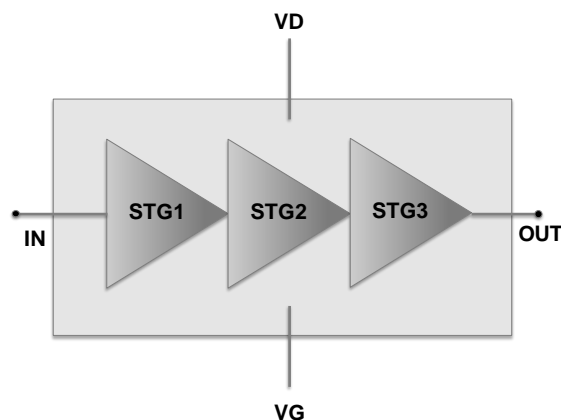
Description

The CHA8252-99F is a three-stage GaN High Power Amplifier in the frequency band 17.3-20.3GHz. This HPA typically provides 10W of output power associated to 35% of Power Added Efficiency. The small signal gain exhibits more than 31dB. The overall power supply is 18V/0.3A (quiescent current).

This circuit is a very versatile amplifier for high performance systems.

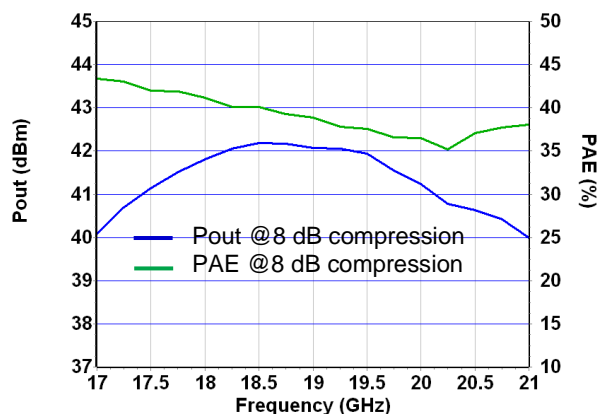
The circuit is dedicated to space applications and well suited for a wide range of microwave applications and systems.

The part is developed on a robust 0.15µm gate length GaN on SiC HEMT process and is available as a bare die.



Main Features

- 17.3-20.3 GHz frequency range
- Linear Gain is 31dB
- 40.5dBm Pout for +16dBm input power
- Associated PAE is more than 35% for +16dBm input power
- Associated Id is 1.8A for +16dBm input power
- DC bias: Vd=18Volts @Idq=0.3A
- Chip size : 5x3.4x0.07mm



Main Electrical Characteristics

Tb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	17.3		20.3	GHz
Gain	Linear Gain		31		dB
PAE	Power Added Efficiency (Pin=16dBm)		35		%
Pout	Output Power (Pin=16dBm)		40.5		dBm

Specifications (CW mode)

Tb.= +25°C, Vd = +18V, Idq = 307mA,

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	17.3		20.3	GHz
Gain	Linear Gain		31		dB
Pout	Output Power (Pin = 16dBm)		40.5		dBm
PAE	Associated Power Added Efficiency (Pin = 16dBm)		35		%
Id	Associated current (Pin = 16dBm)		1.8		A
S11	Input Return Loss		9		dB
S22	Output Return Loss		7		dB
Idq	Quiescent Current		0.3		A
Vd	Drain Voltage		18		V
Vg	Gate Voltage		-2.98		V

These values are representative of measurements done in test fixture with a bonding wire of typically 0.25 to 0.3nH.

Recommended Operating Ratings

Tb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	18V	V
Id_stg1_2	1 st and 2 nd stage drain current (North and South) ⁽²⁾	1	A
Id_stg3	3 rd stage drain current (North and South) ⁽²⁾	1.9	A
Pin	Maximum peak input power overdrive	22	dBm
Tj	Maximum Junction temperature ⁽¹⁾	200	°C

⁽¹⁾ value is provided for Tb=85°C ⁽²⁾ Currents are provided at saturation (with RF signal)

Absolute Maximum Ratings ⁽³⁾

Tb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	25	V
Id_stg1_2	1 st and 2 nd stage drain current (North and South)	1.2	A
Id_stg3	3 rd stage drain current (North and South)	2.3	A
Pin	Maximum peak input power overdrive	25	dBm

⁽³⁾ Operation of this device above anyone of these parameters may cause permanent damage.

Temperature Range

Tb	Operating temperature range (chip backside temperature reference)	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

Typical Bias Conditions

Tb.= +25°C

Symbol	Pad N°	Parameter	Values	Unit
VG1	2, 20	Gate voltage tuned for Idq ~ 307mA	-2.98	V
VG2	5, 17			
VG3	8, 14			
VD	4, 6, 10, 12, 16, 18	Drain Voltage	18	V

“Power ON” sequence

1. Bias HPA gate voltage at Vg close to Vpinch-off (example: Vg ≈ -5V).
2. Apply Vd bias voltage (Example: Vd = 18V).
3. Increase slowly Vgs up to quiescent bias drain current Ids0 (applied on the gate: 307mA).
4. Apply RF signal

“Power OFF” sequence

1. Turn off RF signal
2. Bias HPA gate voltage at Vg close to Vpinch-off (example: Vg ≈ -5V)
3. Set Vd to 0V.
4. Turn off Vd supply.
5. Turn off Vg supply.

Device thermal information

The device thermal performances below are based on UMS rules to evaluate the junction temperature.

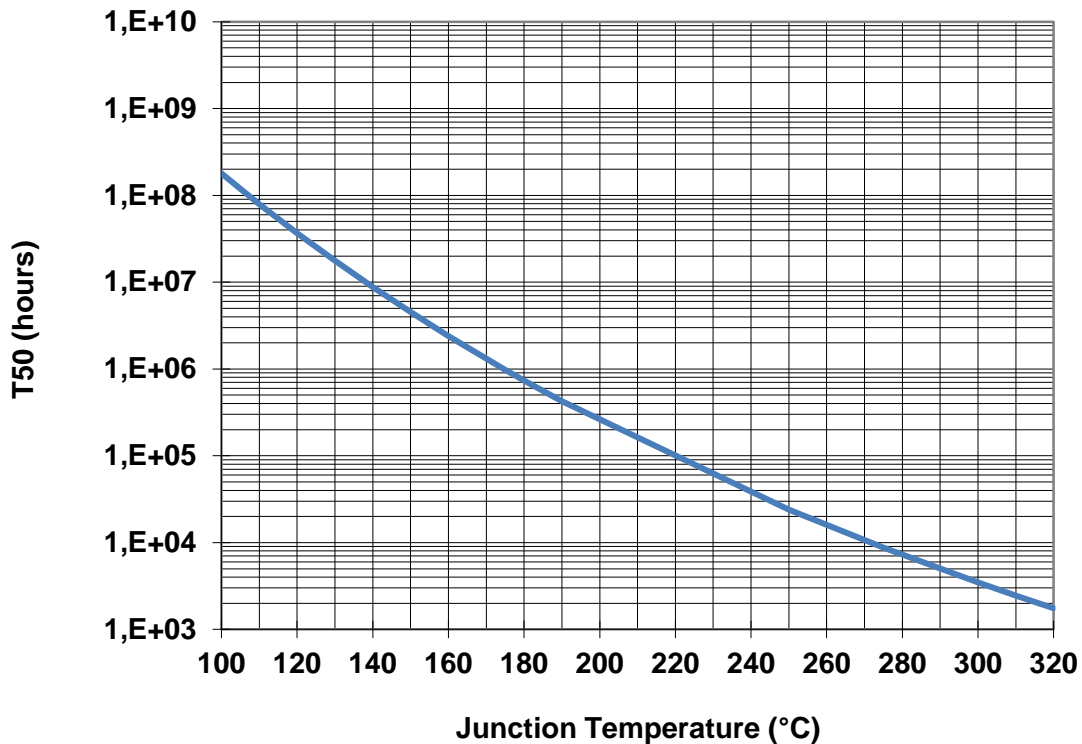
This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHA8252-99F is manufactured (GaN HEMT 0.15µm).

The temperature $T_{b_{chip}}$ is defined as the chip backside temperature. The thermal resistance (R_{th_eq}) is given for the full circuit, and assumes CW mode is given in the table.

Thermal Resistance ⁽¹⁾	R_{th_eq}	$T_{b_{chip}} = 85^{\circ}\text{C}$, $V_d = 18\text{V}$, $I_{d_drive} = 1.9\text{A}$ $P_{in} = 17\text{dBm}$, $P_{out} = 41\text{dBm}$ $P_{diss} = 18.5\text{W CW}$	2.2	$^{\circ}\text{C/W}$
Junction Temperature	T_j		126	$^{\circ}\text{C}$
Median Life	T50		2E07	Hrs

⁽¹⁾ Thermal resistance measured at the back of the chip

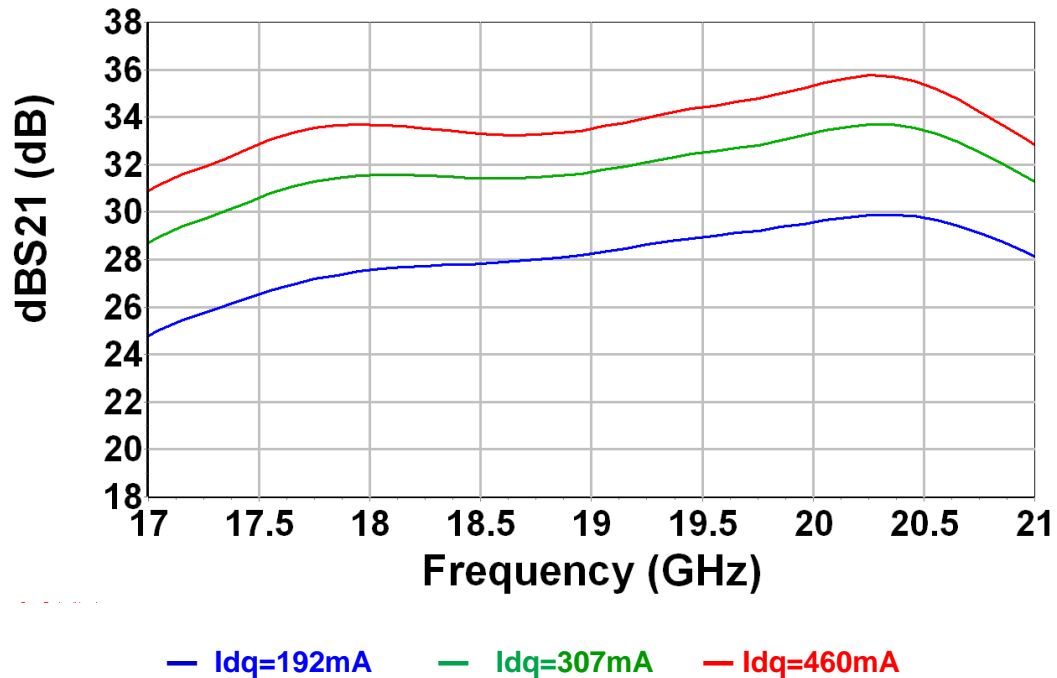
Median Life Time versus Junction Temperature



Typical Test Fixture Measurements: Small Signal Performances

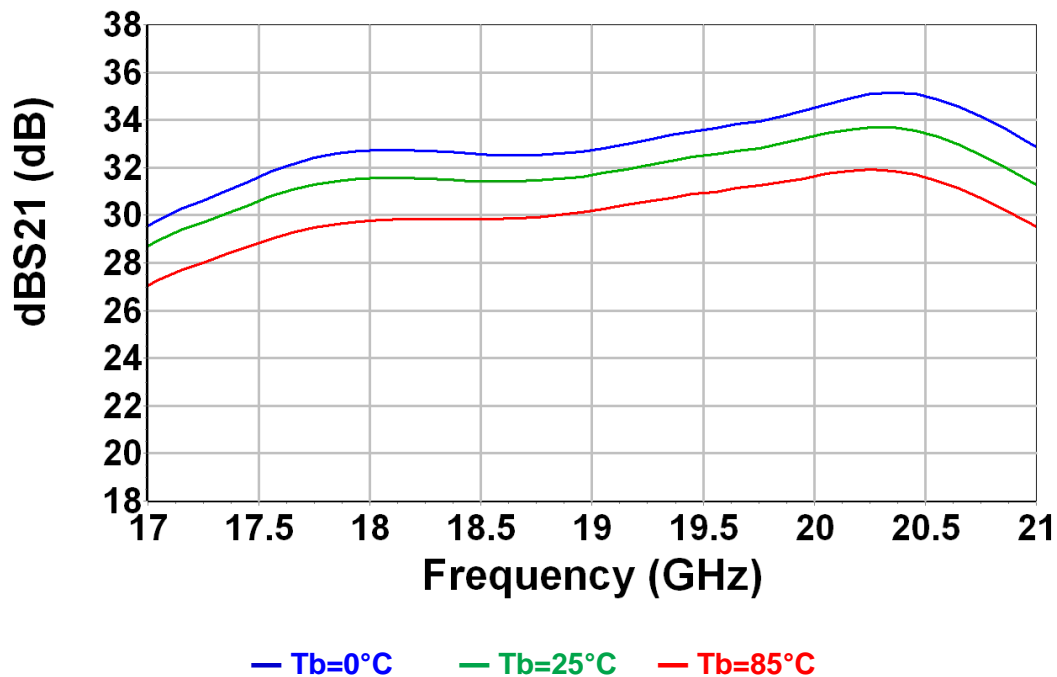
CW measurements: $T_b = 25^\circ\text{C}$, $V_d = +18\text{V}$

Linear Gain versus Frequency



CW measurements: $T_b = +25^\circ\text{C}/+85^\circ\text{C}/0^\circ\text{C}$, $V_d = +18\text{V}$, $I_{dq} = 307\text{mA}$ (kept constant versus temperature)

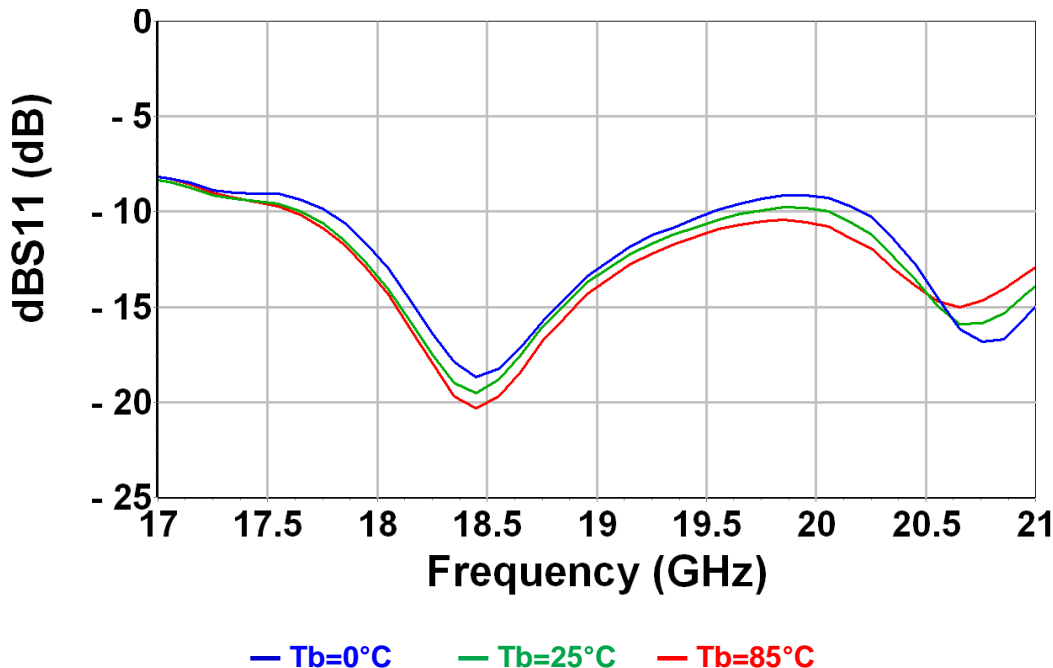
Linear Gain versus Frequency



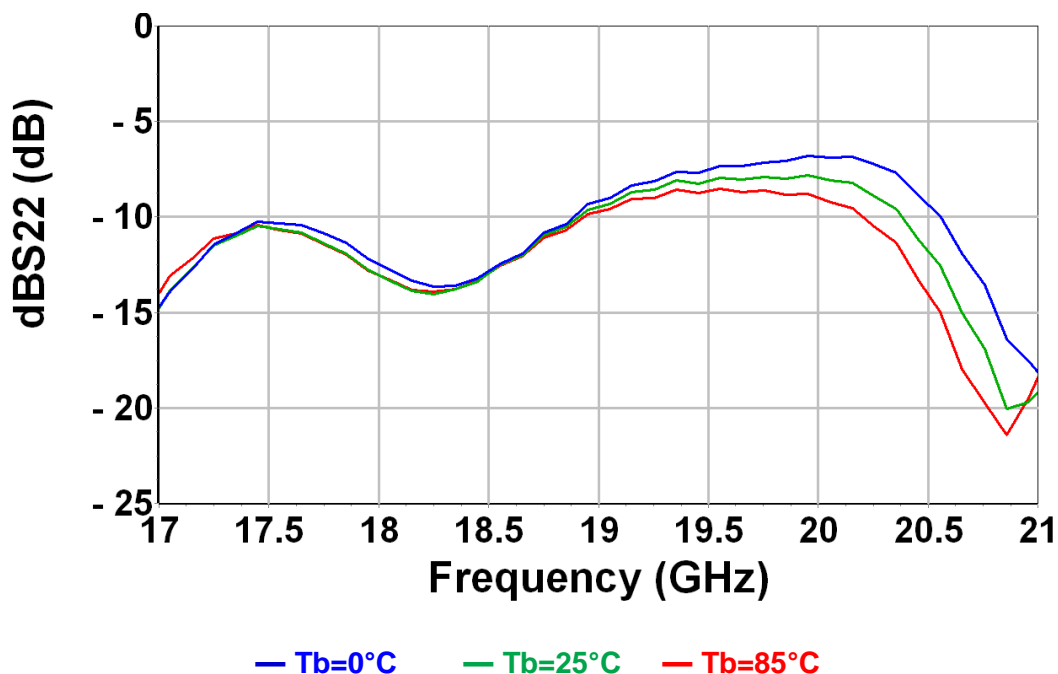
Typical Test Fixture Measurements: Small Signal Performances

CW measurements: $T_b = +25^\circ\text{C}/+85^\circ\text{C}/0^\circ\text{C}$, $V_d = +18\text{V}$, $I_{dq} = 307\text{mA}$ (kept constant versus temperature)

Input Return Loss versus Frequency

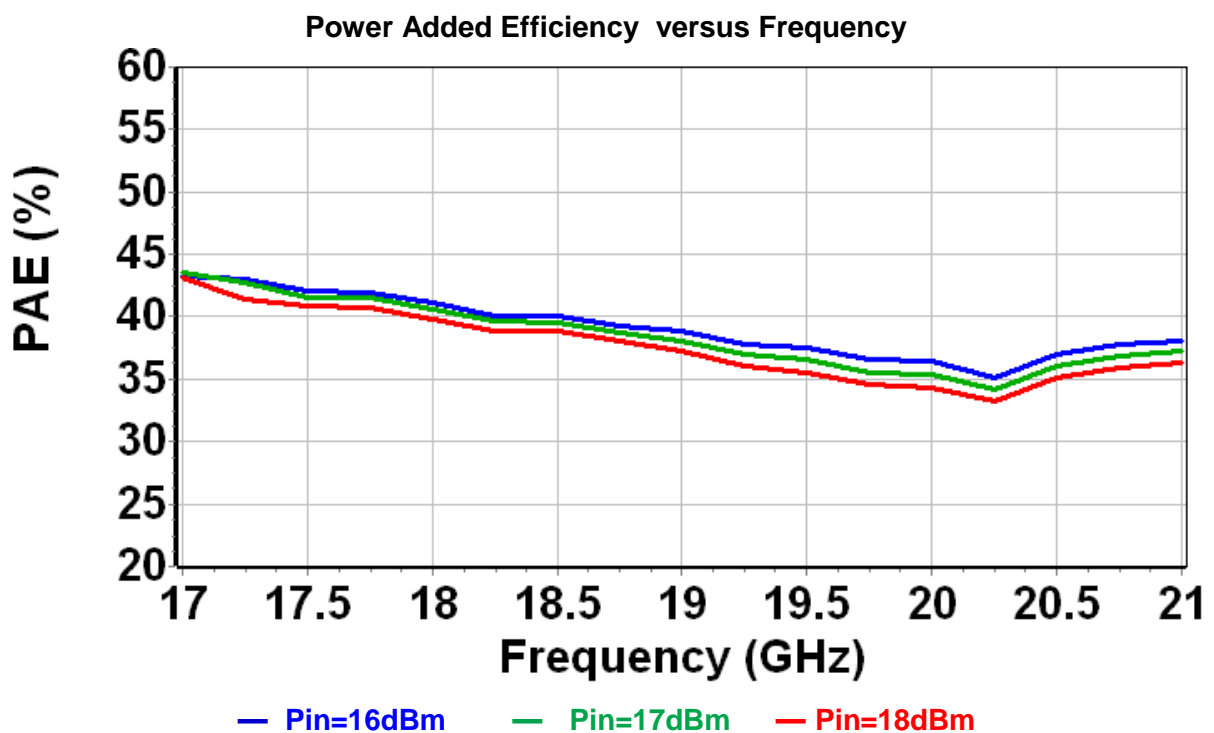
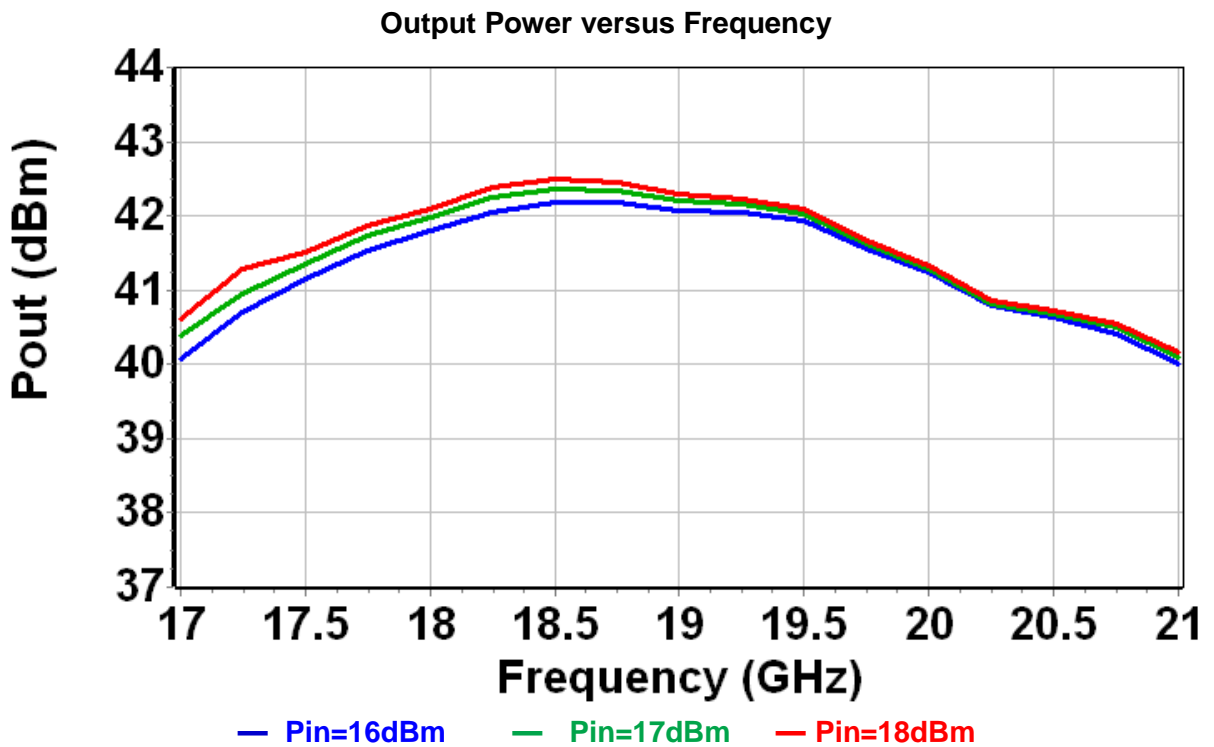


Output Return Loss versus Frequency



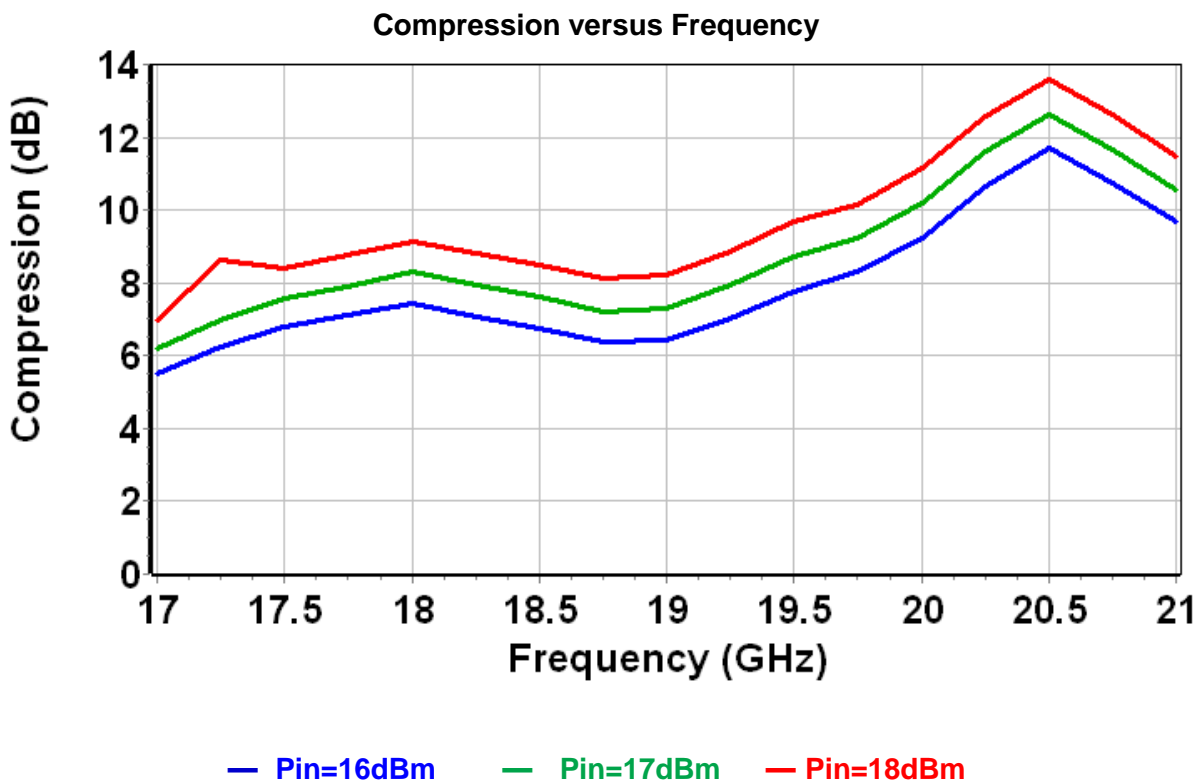
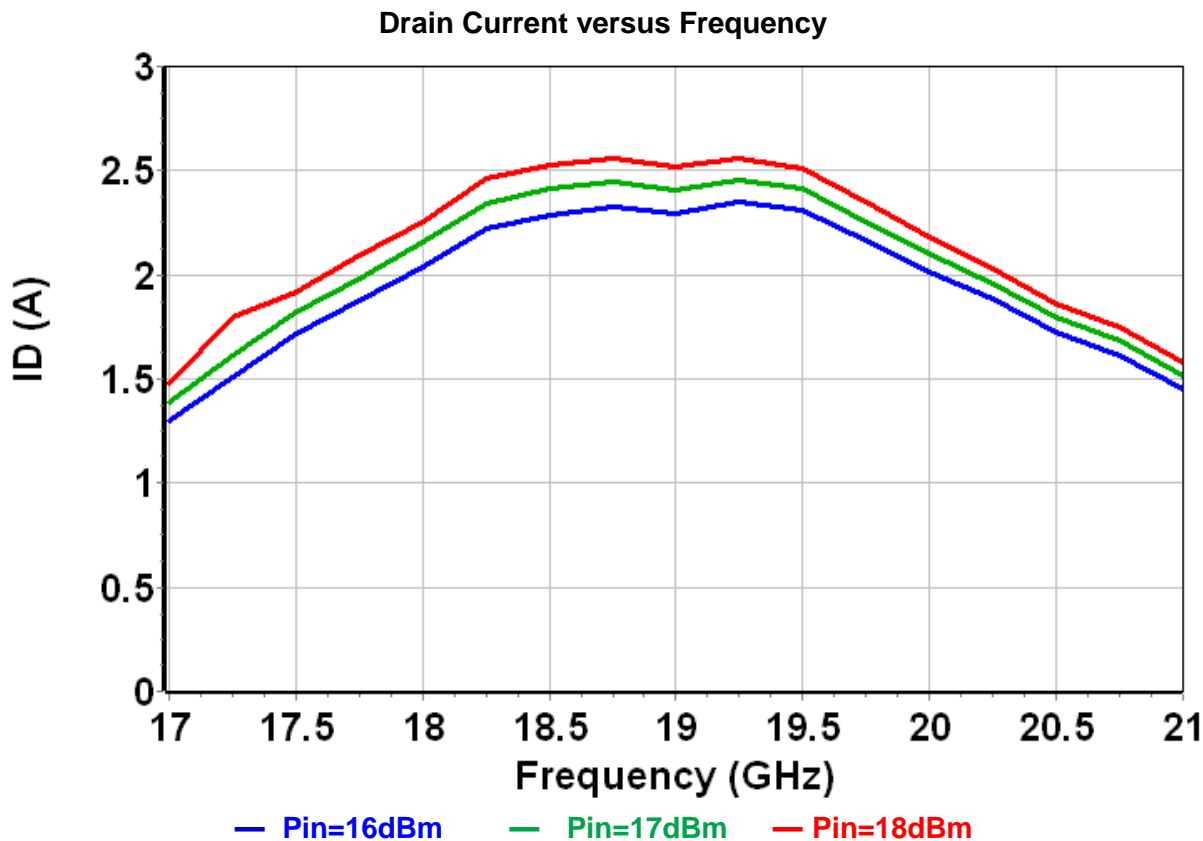
Typical Test Fixture Measurements: Non-linear performances

CW measurements: $T_b = +25^\circ\text{C}$, $V_d = +18\text{V}$, $I_{dq} = 307\text{mA}$



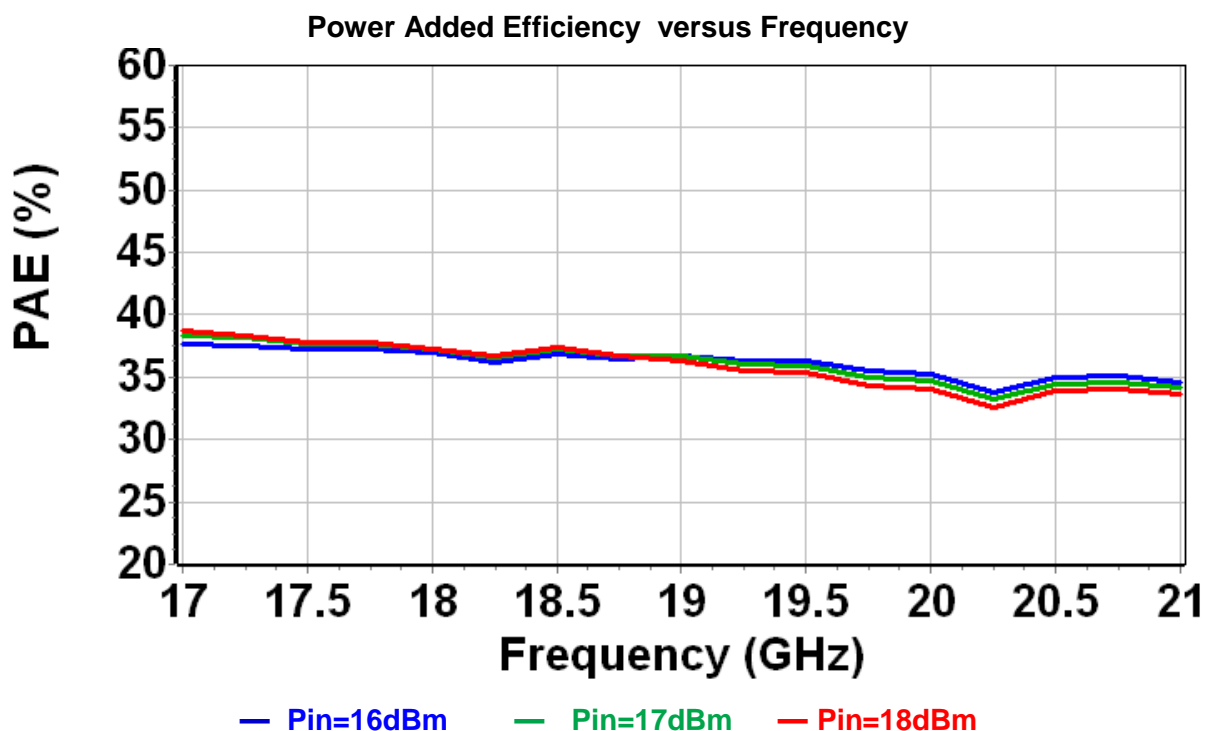
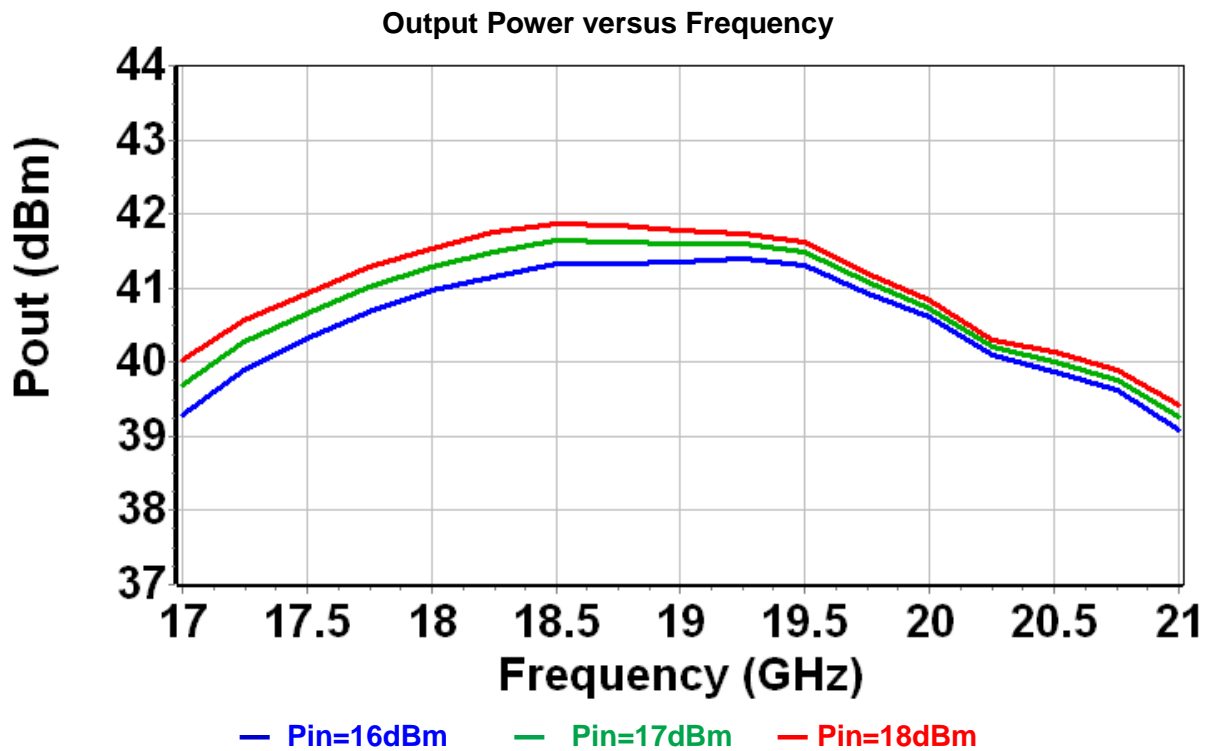
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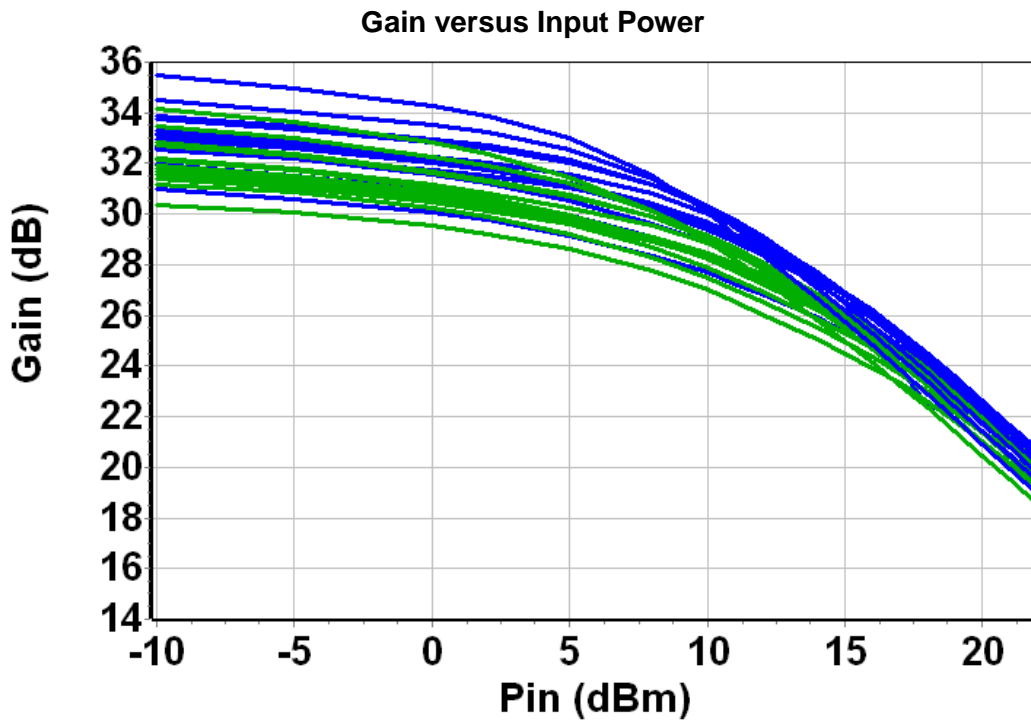
CW measurements: $T_b = +85^\circ\text{C}$, $V_d = +18\text{V}$, $I_{dq} = 307\text{mA}$



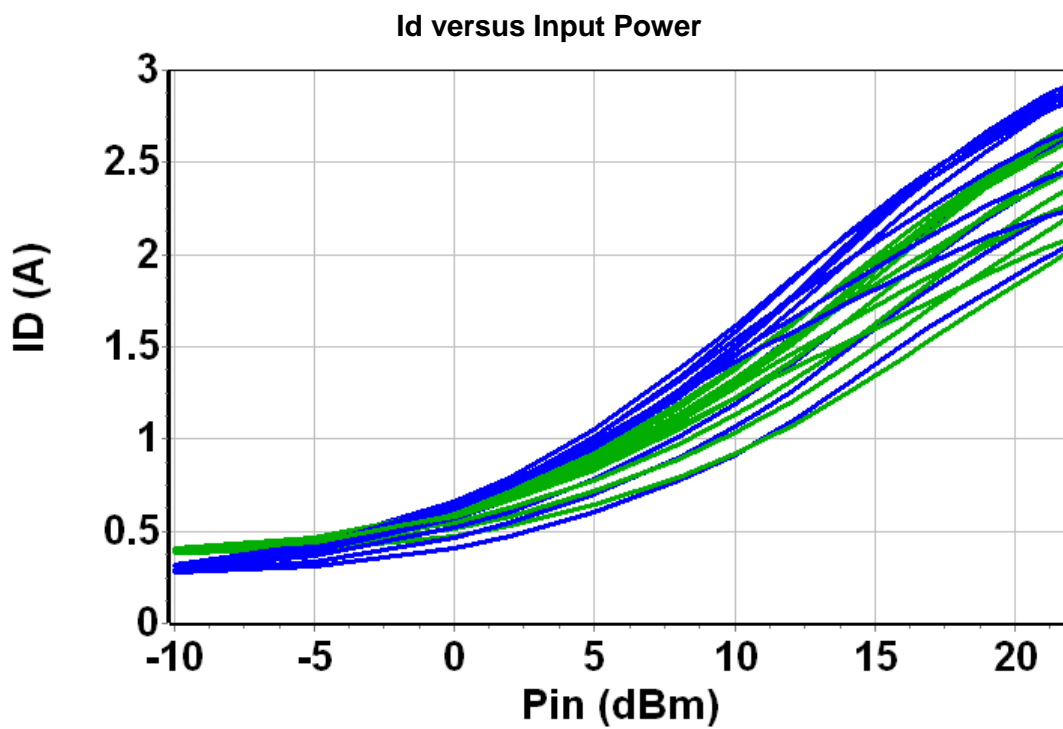
Typical Test Fixture Measurements: Non-linear Performances

CW measurements: $V_d = +18V$, $I_{dq} = 307mA$ (kept constant versus temperature)

Pin range : -10 to 22 dBm, Frequency range: 17.25-20.25 GHz step 0.25 GHz



— $T_b = 25^\circ C$ — $T_b = 85^\circ C$

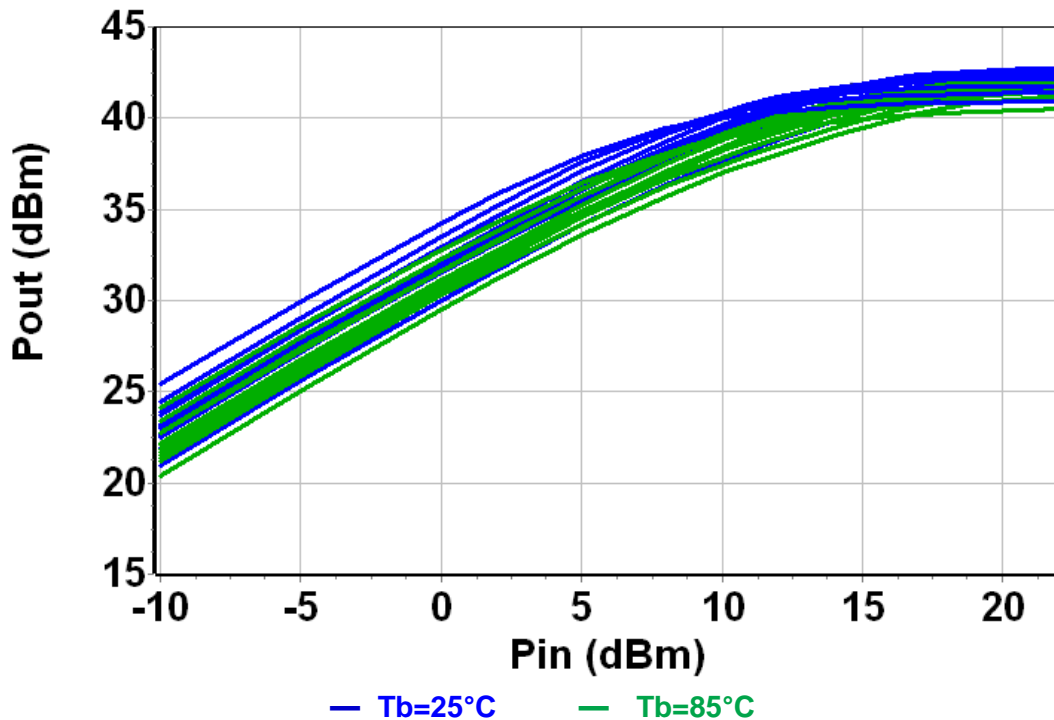


— $T_b = 25^\circ C$ — $T_b = 85^\circ C$

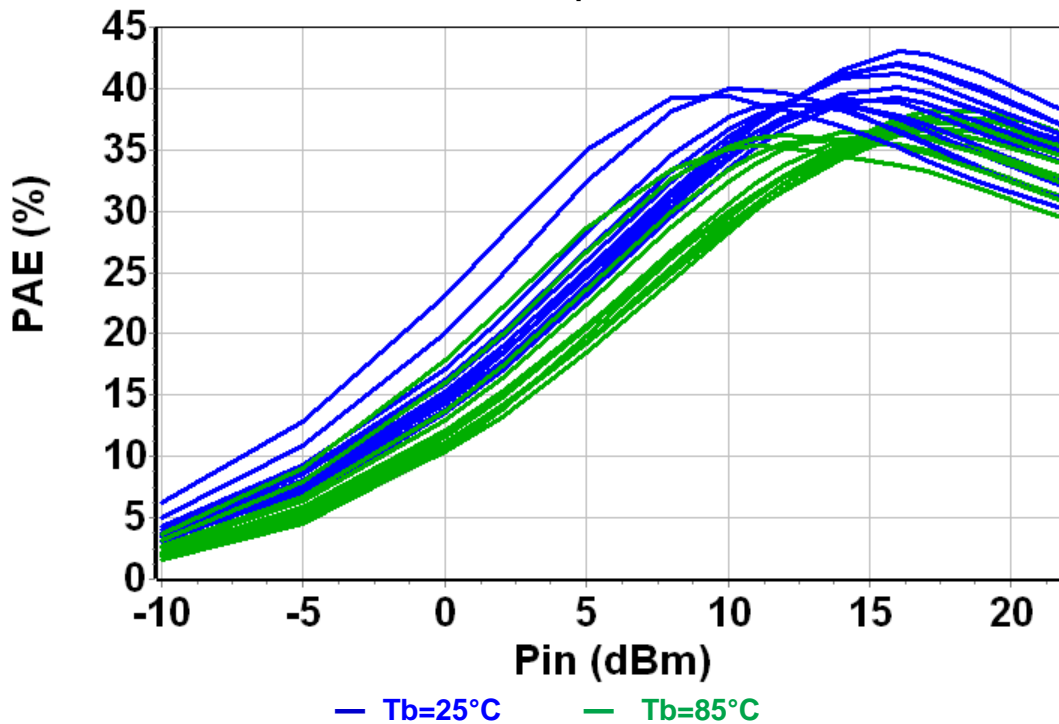
Typical Test Fixture Measurements: Non-linear Performances

CW measurements: $V_d = +18V$, $I_{dq} = 307mA$ (kept constant versus temperature)
 Pin range : -10 to 22 dBm, Frequency range: 17.25-20.25 GHz step 0.25 GHz

Pout versus Input Power



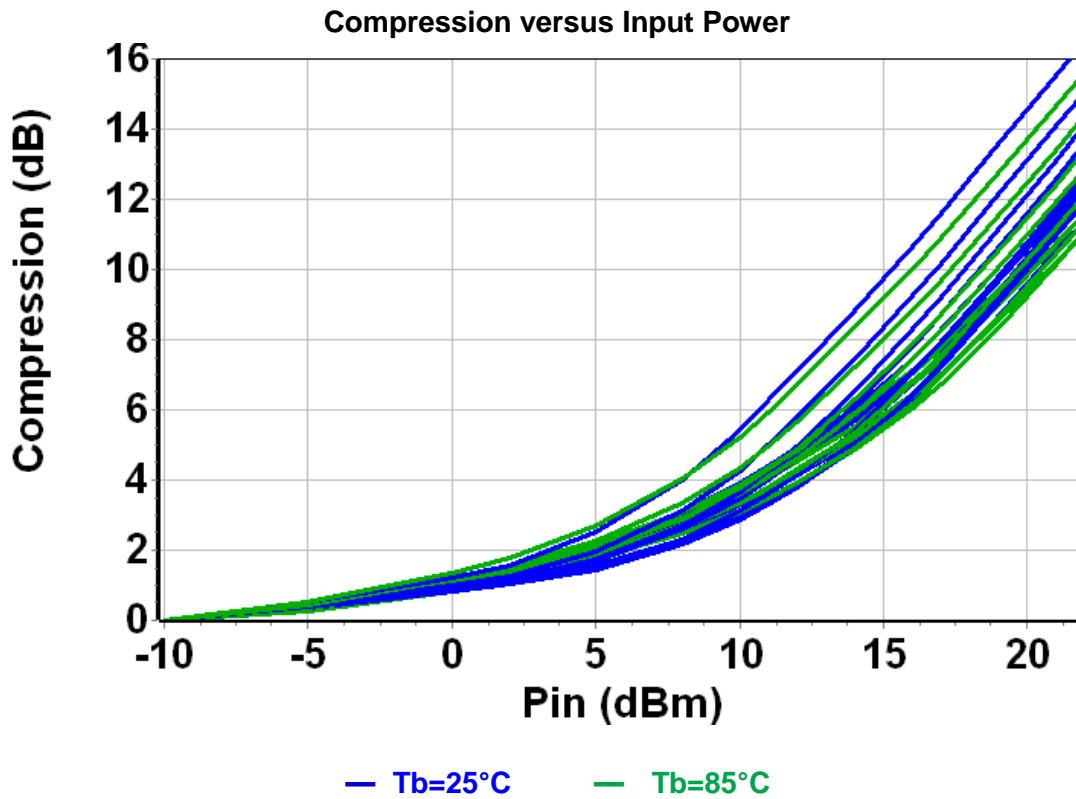
PAE versus Input Power



Typical Test Fixture Measurements: Non-linear Performances

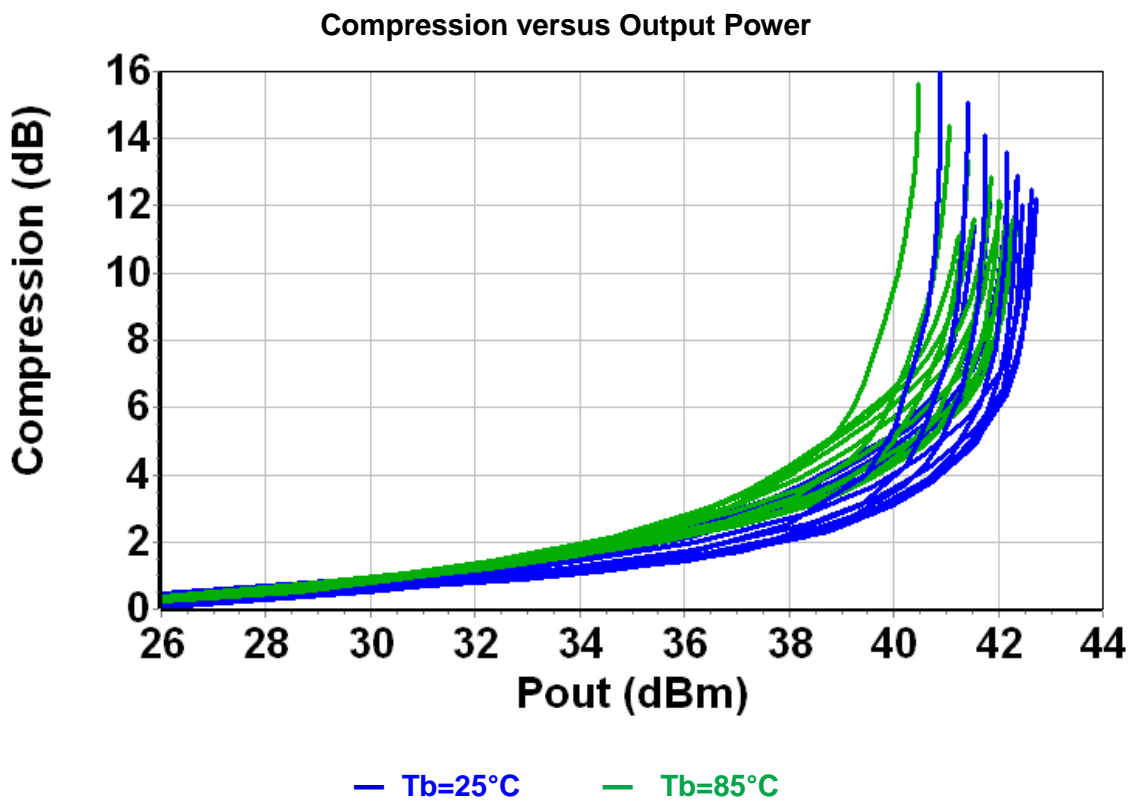
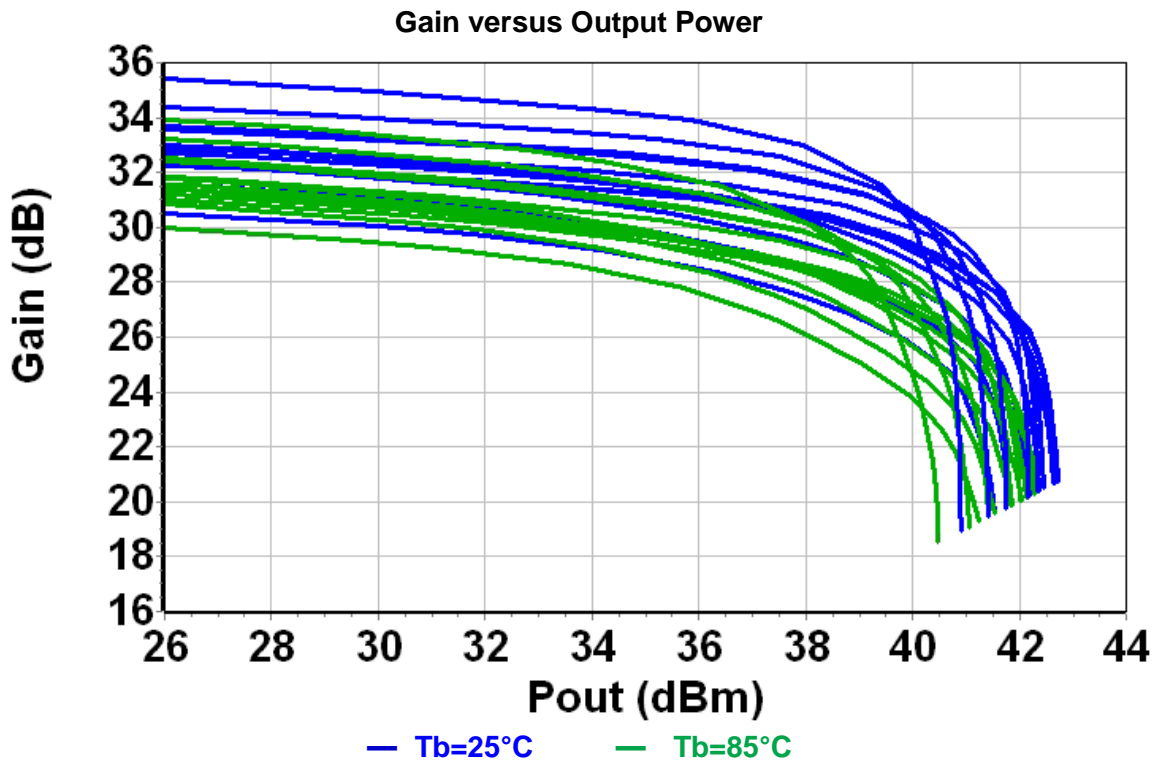
CW measurements: $V_d = +18V$, $I_{dQ} = 307mA$ (kept constant versus temperature)

Pin range : -10 to 22 dBm, Frequency range: 17.25-20.25 GHz step 0.25 GHz



Typical Test Fixture Measurements: Non-linear Performances

CW measurements: $V_d = +18V$, $I_{dq} = 307mA$ (kept constant versus temperature)
 Pin range : -10 to 22 dBm, Frequency range: 17.25-20.25 GHz step 0.25 GHz

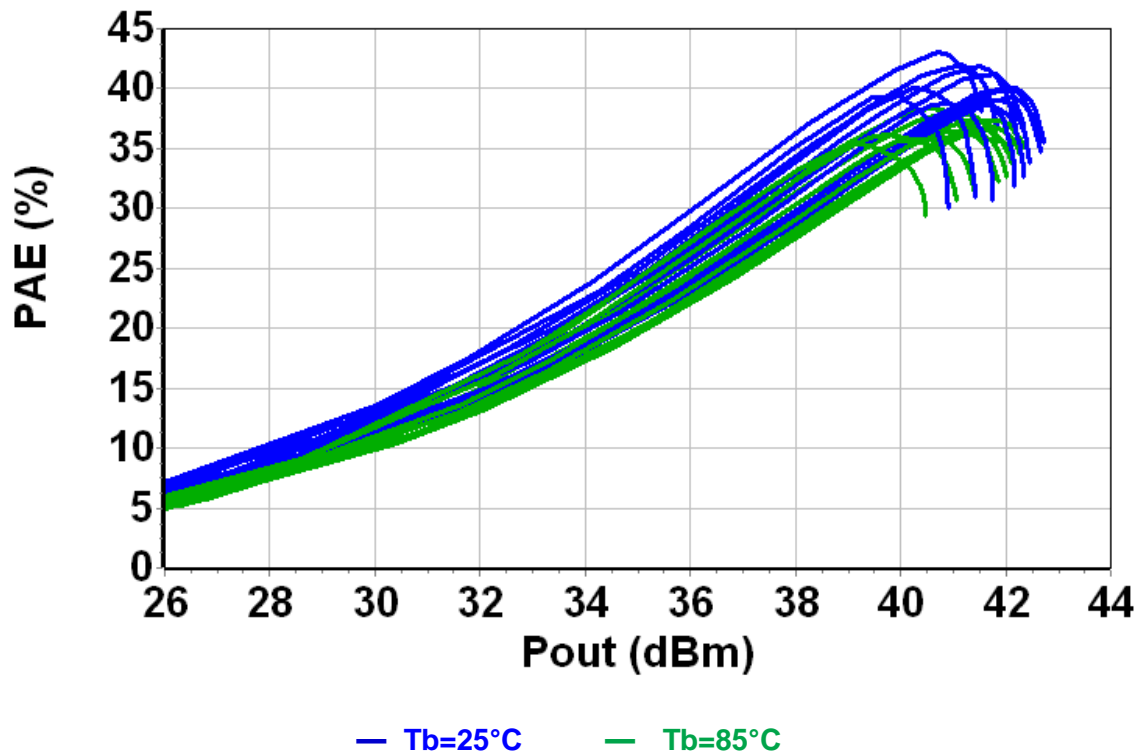


Typical Test Fixture Measurements: Non-linear Performances

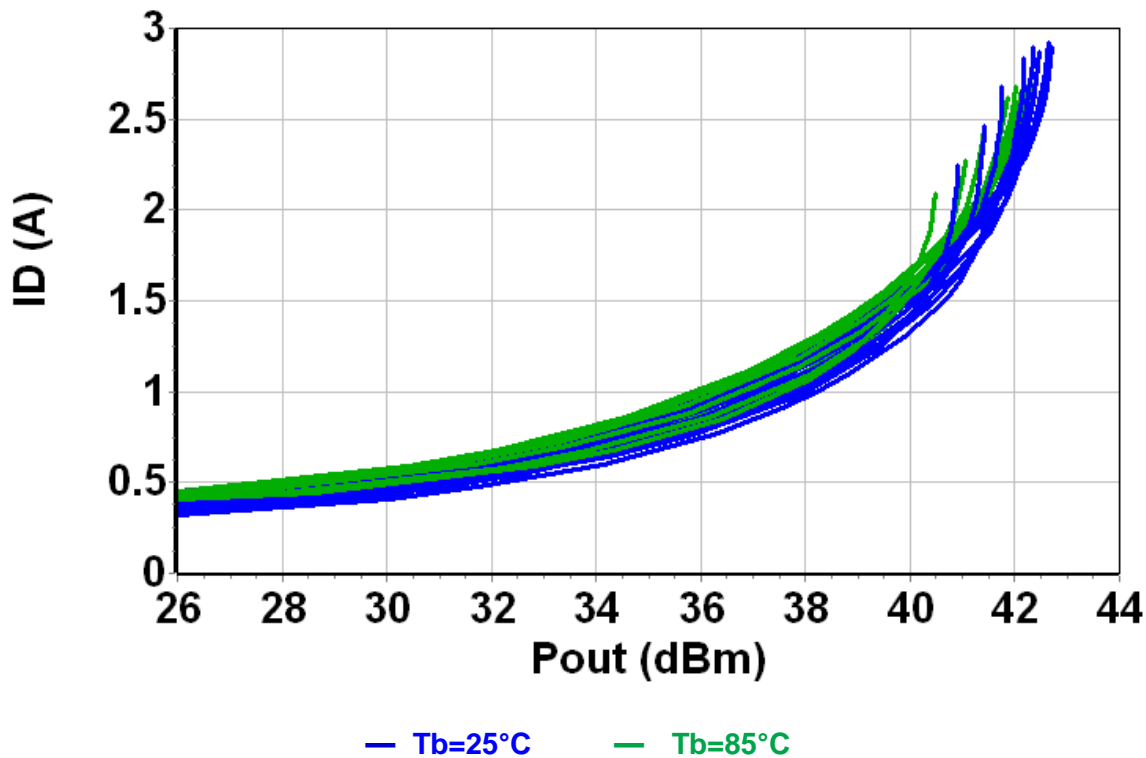
CW measurements: $V_d = +18V$, $I_{dq} = 307mA$ (kept constant versus temperature)

Pin range : -10 to 22 dBm, Frequency range: 17.25-20.25 GHz step 0.25 GHz

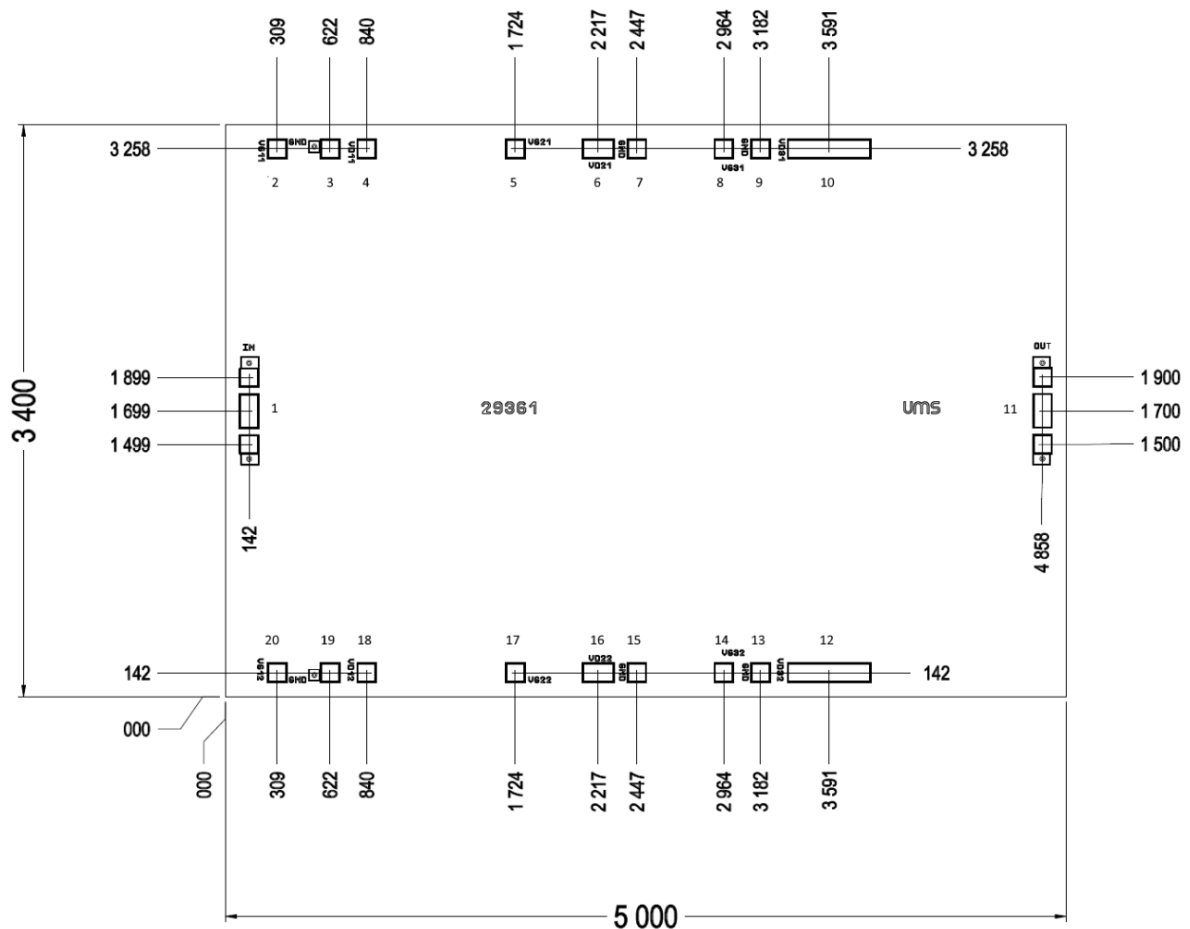
Power Added Efficiency versus Output Power



Drain current versus Output Power



Chip Mechanical data



All dimensions are in micrometres.

Chip size = 5000x3400 ±50µm

Chip thickness = 70µm ±10µm

Chip width and length are given with a tolerance of ±50µm

RF pads (1, 11) = 208 x 118µm²

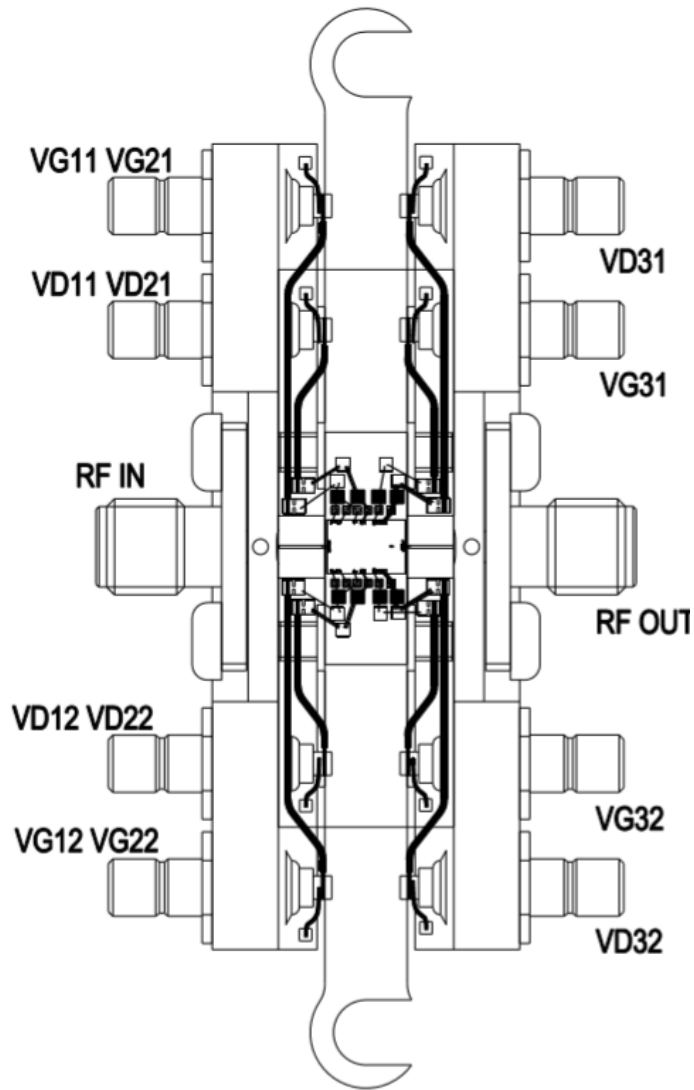
DC pads (2, 3, 4, 5, 7, 8, 9, 13, 14, 15, 17, 18, 19, 20) = 118 x 118µm²

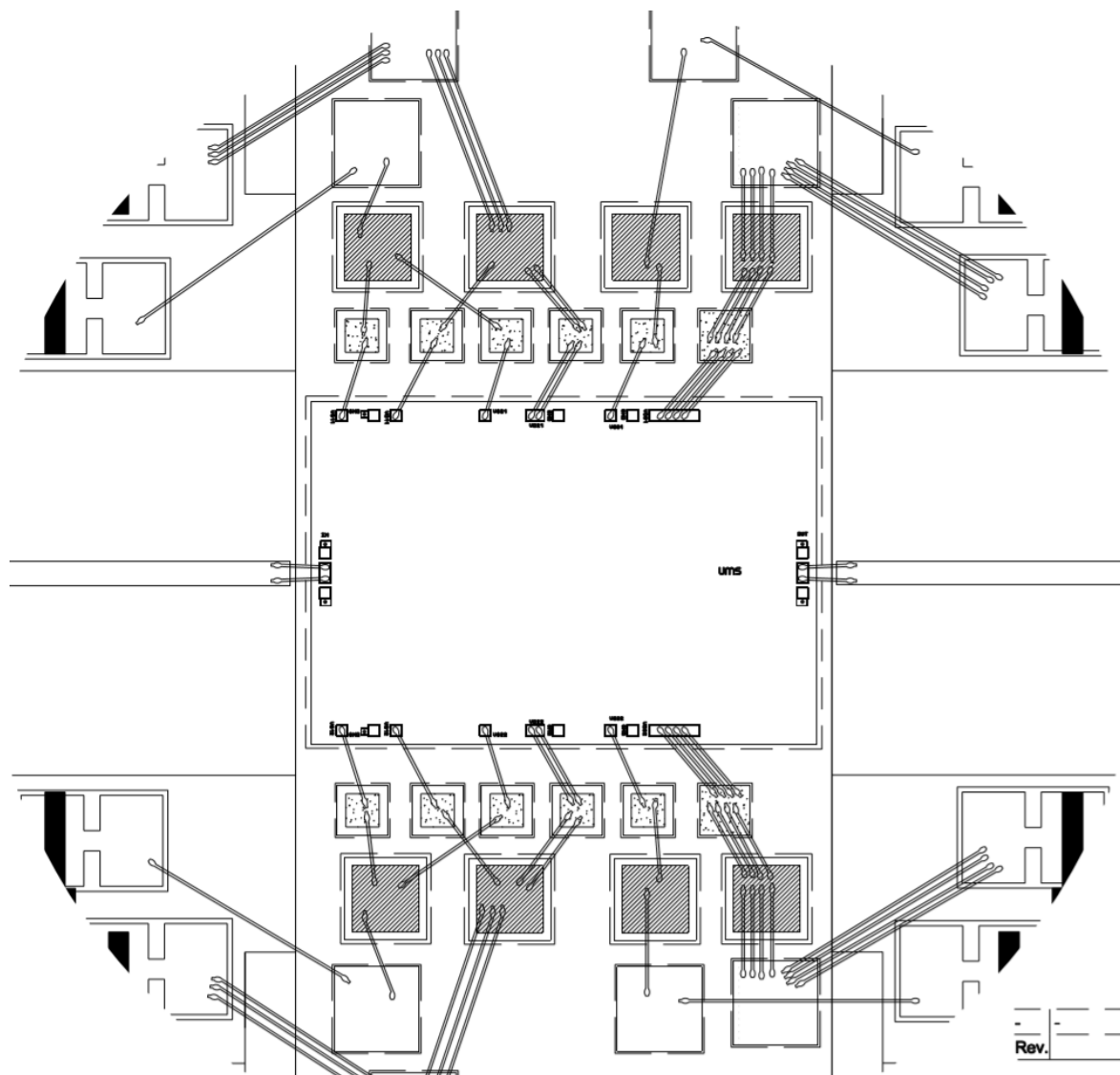
DC pads (6, 16) = 190 x 118µm²

DC pads (10, 12) = 500 x 118µm²

PAD Number	Name	Description
1	IN	RF input
3, 7, 9, 13, 15, 19	GND	Ground (Not connected)
2, 20	VG1	Gate voltage of 1 st stage
5, 17	VG2	Gate voltage of 2 nd stage
8, 14	VG3	Gate voltage of 3 rd stage
4, 18	VD1	Drain voltage of 1 st stage
6, 16	VD2	Drain voltage of 2 nd stage
10, 12	VD3	Drain voltage of 3 rd stage
11	OUT	RF output

Recommended Test Jig



Recommended assembly plan

3 levels of decoupling capacitor have been used:

First level of capacitor is 120pF, second level is 1nF, third level is 10nF and fourth level is 1 μ F. Only 120pF, 1nF and 10nF capacitors could be seen on the previous assembly drawing (close to the chip).

Note: Supply feed should be bypassed. 25 μ m diameter gold wire is to be preferred.

Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <https://www.ums-rf.com>.

Recommended reflow process assembly

Refer to the application note AN0001 available at <https://www.ums-rf.com> for die attach.

Ordering Information

Chip form:

CHA8252-99F/00

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