

## 17.7 - 19.7GHz Power Amplifier

### GaAs Monolithic Microwave IC in SMD leadless package

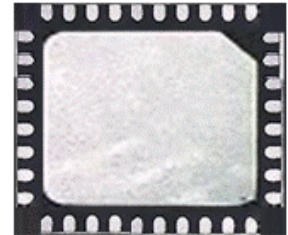
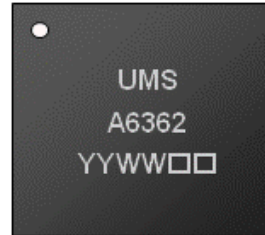
#### Description

The CHA6362-QXG is a three stage monolithic GaAs high power circuit producing 2.5 Watt output power. It integrates a power detector and allows gain control. ESD protections are included.

It is designed for Point To Point Radio or K-band Sat- Com application.

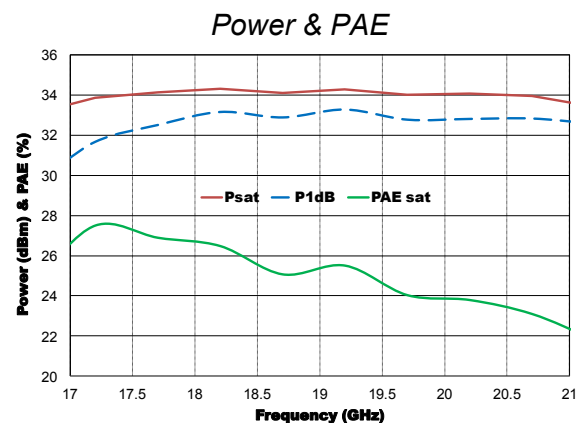
The circuit is manufactured with a pHEMT process, 0.15µm gate length.

It is supplied in RoHS compliant SMD package.



#### Main Features

- Frequency range: 17.7- 19.7GHz
- 34.5dBm saturated power
- 42dBm OIP3
- 22dB gain
- DC bias: Vd = 6.0Volt @ Id = 1.34A
- QFN5x6
- MSL3



#### Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	17.7		19.7	GHz
Gain	Linear Gain		22		dB
Psat	Saturated output power		34.5		dBm
OIP3	Output IP3		42		dBm

**Electrical Characteristics**

Tamb.= +25°C, Vd = +6V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	17.7		19.7	GHz
Gain	Small Signal Gain		22		dB
Psat	Saturated Output Power		34.5		dBm
P1dB	Output power at 1dB compression		33		dBm
$\Delta G$	Gain variation in temperature		+/- 0.034		dB/°C
OIP3	Output IP3		42		dBm
PAE	PAE at saturation		24		%
CG	Gain control range		15		dB
NF	Noise Figure @ nominal gain		6		dB
Rlin	Input Return Loss		14		dB
Rlout	Output Return Loss		18		dB
Dr	Detection dynamic range(for output power detection up to Psat)		30		dB
Vdetect	Voltage detection $V_{REF}$ - $V_{DET}$ up to Psat		10 to 2400		mV
Vg	DC gate Voltage		-0.85		V
Idet	Detector current		600		$\mu A$
Idq	Total drain current		1.34		A

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

**Absolute Maximum Ratings** <sup>(1)</sup>

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	6.5V	V
Id	Drain bias quiescent current	1700	mA
Vg	Gate bias voltage	-2 to 0	V
Pin	Maximum peak input power overdrive <sup>(2)</sup>	+20	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

<sup>(1)</sup> Operation of this device above anyone of these parameters may cause permanent damage.

<sup>(2)</sup> Thermal Resistance channel to ground paddle =9.4°C/W for Tamb. = +85°C with 6.0V & 1.34A.

**Typical Bias Conditions**

Tamb.= +25°C

Symbol	Pad N°	Parameter	Values	Unit
VD1	7, 20	DC Drain voltage 1 <sup>st</sup> stage	6.0	V
VD2	5, 22	DC Drain voltage 2 <sup>nd</sup> stage	6.0	V
VD3	3, 24	DC Drain voltage 3 <sup>rd</sup> stage	6.0	V
VG1	8, 19	DC Gate voltage 1 <sup>st</sup> stage	-0.85	V
VG2	6, 21	DC Gate voltage 2 <sup>nd</sup> stage	-0.85	V
VG3	4, 23	DC Gate voltage 3 <sup>rd</sup> stage	-0.85	V
DC	1	DC Detector voltage	6.0	V

## Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered). The temperature is monitored at the package back-side interface (Tcase) as shown below. The system maximum temperature must be adjusted in order to guarantee that Tcase remains below the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

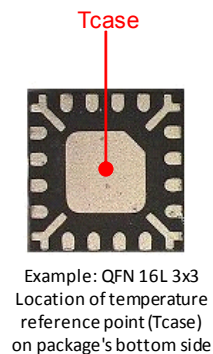
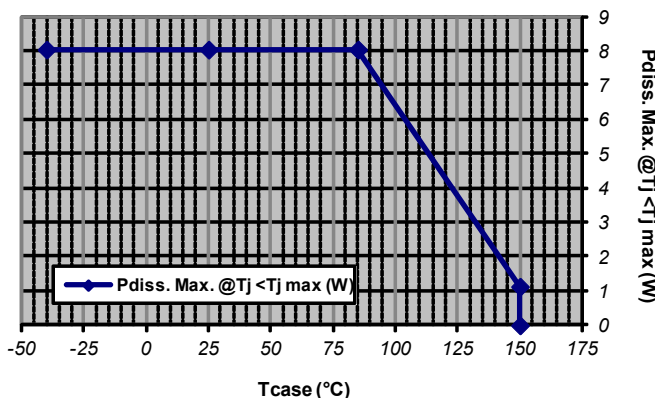
A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

DEVICE THERMAL SPECIFICATION : CHA6362-QXG	
Recommended max. junction temperature (Tj max)	: 161 °C
Junction temperature absolute maximum rating	: 175 °C
Max. continuous dissipated power (Pdiss. Max.)	: 8.0 W
=> Pdiss. Max. derating above Tcase <sup>(1)</sup> = 85 °C	: 106 mW/°C
Junction-Case thermal resistance (Rth J-C) <sup>(2)</sup>	: <9 °C/W
Minimum Tcase operating temperature <sup>(3)</sup>	: -40 °C
Maximum Tcase operating temperature <sup>(3)</sup>	: 85 °C
Minimum storage temperature	: -55 °C
Maximum storage temperature	: 150 °C

(1) Derating at junction temperature constant = Tj max.

(2) Rth J-C is calculated for a worst case considering the **hottest junction** of the MMIC and all the devices biased.

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).



### Typical Package Sij parameters

Tamb.= +25°C, Vd = +6V, Id = 1340mA

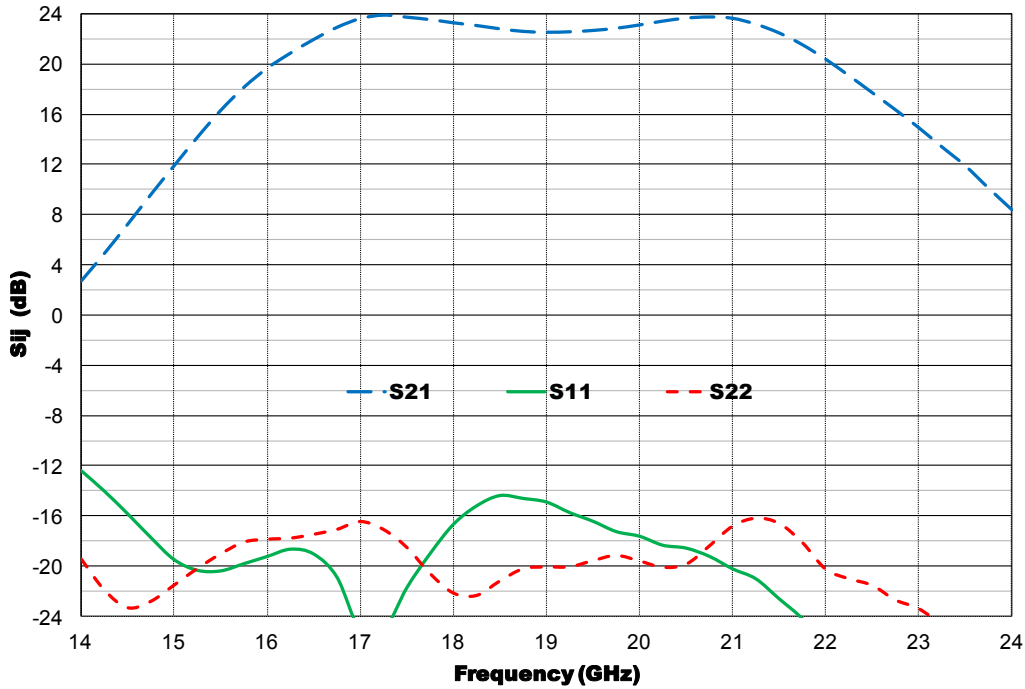
Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
2	-0.574	138.2	-69.730	48.9	-84.916	124.6	-0.454	132.3
3	-0.586	116.4	-71.295	8.4	-68.140	26.1	-0.467	107.8
4	-0.800	92.9	-67.912	7.3	-68.464	6.9	-0.724	81.2
5	-1.529	69.3	-67.363	-13.8	-69.051	-23.8	-1.493	55.2
6	-2.560	46.9	-75.436	-58.8	-70.542	-61.5	-2.241	30.6
7	-3.602	27.8	-77.305	-53.6	-87.120	-86.8	-3.082	7.1
8	-4.373	10.0	-71.044	-31.9	-68.044	-88.5	-3.609	-14.4
9	-4.552	-10.7	-70.287	-25.5	-66.322	-159.8	-3.885	-39.7
10	-4.861	-33.4	-64.902	-81.6	-47.924	108.6	-4.371	-67.7
11	-5.442	-58.0	-59.034	-121.7	-30.585	28.0	-5.064	-99.5
12	-6.287	-84.7	-55.548	164.0	-12.854	-92.5	-6.923	-136.8
13	-7.958	-114.9	-53.073	123.0	-5.223	132.2	-10.222	-175.4
14	-11.029	-150.6	-51.146	88.9	2.560	27.0	-16.984	157.0
15	-17.784	156.5	-49.783	43.4	11.830	-87.5	-18.626	173.3
16	-23.840	-0.7	-52.011	6.4	19.708	136.0	-16.116	136.3
17	-23.099	-95.3	-69.142	-82.1	23.643	-8.9	-17.738	82.9
18	-18.490	-41.9	-48.662	33.7	23.276	-145.3	-29.078	52.4
19	-13.720	-98.1	-48.815	-30.0	22.439	96.8	-23.463	57.1
20	-14.076	-144.8	-55.035	-39.6	23.090	-16.3	-26.826	25.3
21	-21.429	139.5	-52.354	-12.4	23.517	-146.1	-21.096	28.4
22	-23.910	-82.2	-52.463	-21.4	20.350	73.4	-20.968	-37.7
23	-20.298	-134.1	-49.410	8.1	14.758	-55.6	-21.910	-59.1
24	-22.738	-160.4	-44.421	-20.7	8.300	179.4	-21.053	-94.3
25	-24.459	-130.3	-42.946	-45.0	0.616	53.2	-20.130	-132.3
26	-15.259	-123.5	-42.193	-61.1	-9.132	-88.0	-19.493	-176.1
27	-9.522	-153.5	-39.625	-76.7	-29.329	146.6	-20.365	171.3
28	-5.994	169.3	-37.889	-112.4	-40.918	-103.0	-16.120	154.1
29	-4.229	133.3	-37.608	-147.7	-38.621	-146.8	-12.399	121.3
30	-3.265	98.8	-42.998	-171.2	-42.716	-172.7	-9.795	76.5
31	-3.166	63.5	-46.728	-165.8	-44.087	-152.8	-8.716	17.6
32	-3.575	23.0	-43.589	-143.3	-41.232	-134.2	-8.158	-57.1
33	-5.455	-33.3	-36.975	-151.7	-37.377	-158.2	-7.055	-139.3
34	-9.281	-117.7	-36.564	169.7	-36.801	169.2	-7.727	149.3
35	-11.673	148.3	-36.286	148.6	-36.974	146.3	-12.787	-171.1
36	-17.418	81.0	-39.685	126.1	-38.767	120.5	-4.760	139.5
37	-15.018	-166.1	-39.708	124.5	-39.563	129.8	-2.929	115.9
38	-5.630	146.6	-40.348	105.2	-39.554	97.7	-1.583	89.6
39	-2.813	108.7	-40.075	95.1	-41.444	107.1	-1.082	67.4
40	-1.604	78.6	-40.391	92.6	-40.769	84.2	-0.779	47.7

Typical board Measurements

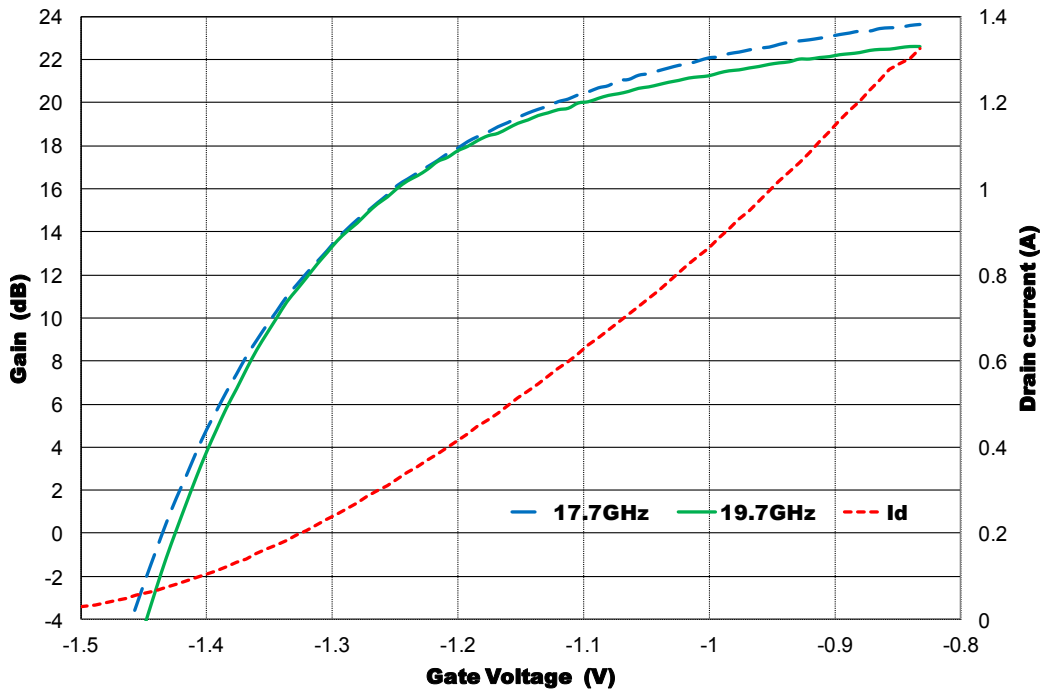
Tamb.= +25°C, Vd = +6V, Id = 1340mA

Measurement in the plan of the QFN, using the proposed land pattern & board, as defined in paragraph "Evaluation mother board"

S parameters versus Frequency



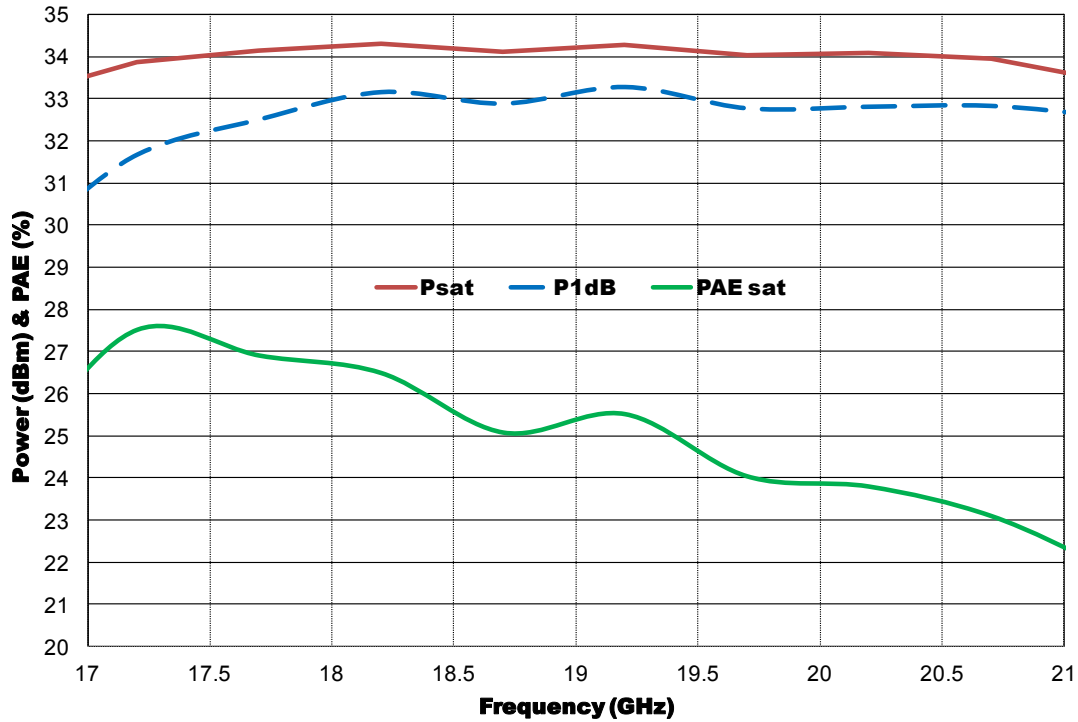
Linear Gain & current versus Gate Voltage



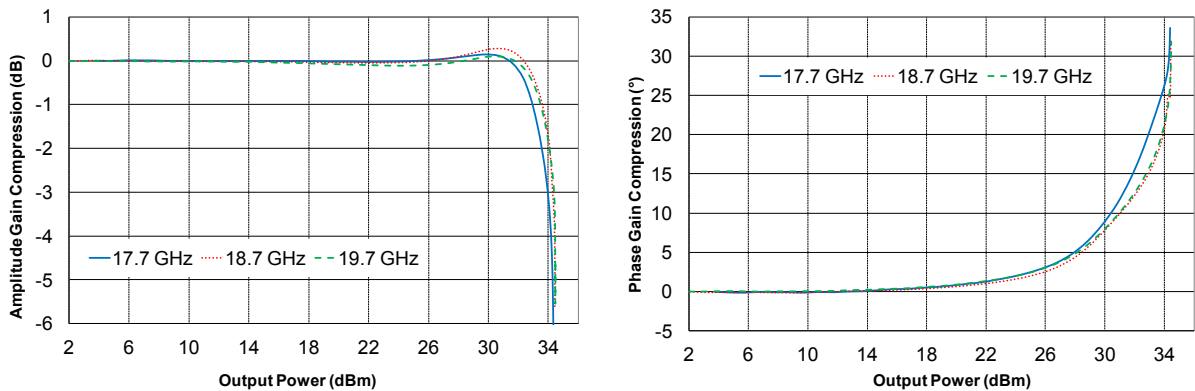
Typical Board Measurements

Tamb.= +25°C, Vd = +6V, Id = 1340mA

Output power and PAE versus Frequency



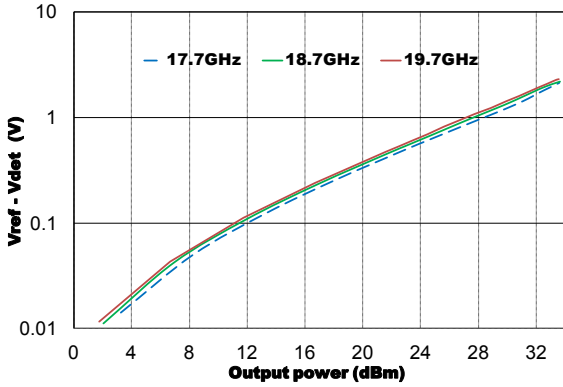
Amplitude & Phase variation versus Output Power



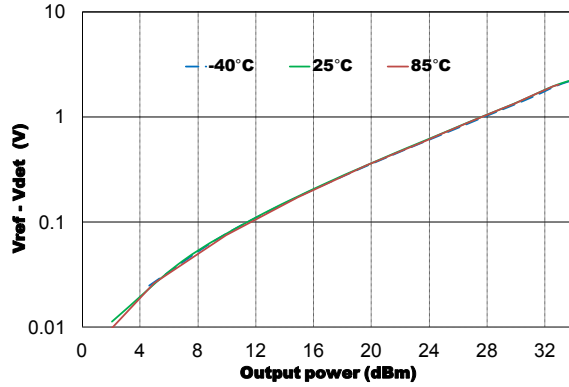
## Typical board Measurements

Tamb.= +25°C, Vd = +6V, Id = 1340mA

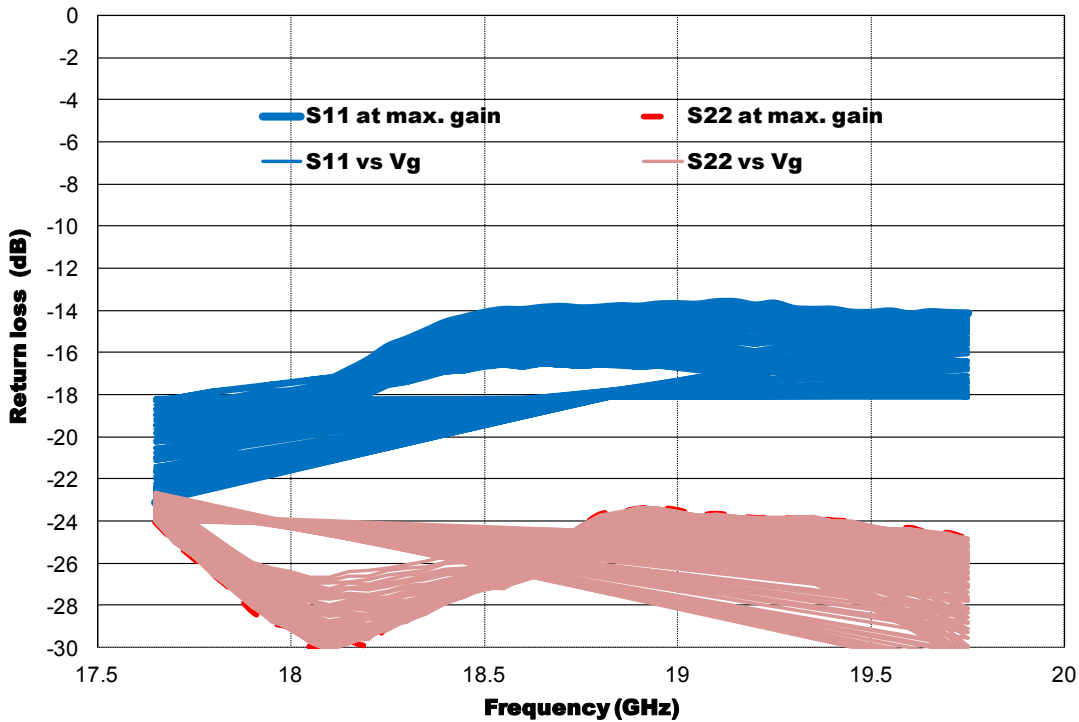
**Power Detector versus Pout & Frequency**



**Power Detector versus Pout & Temperature**



**Return Losses versus Gain Control**

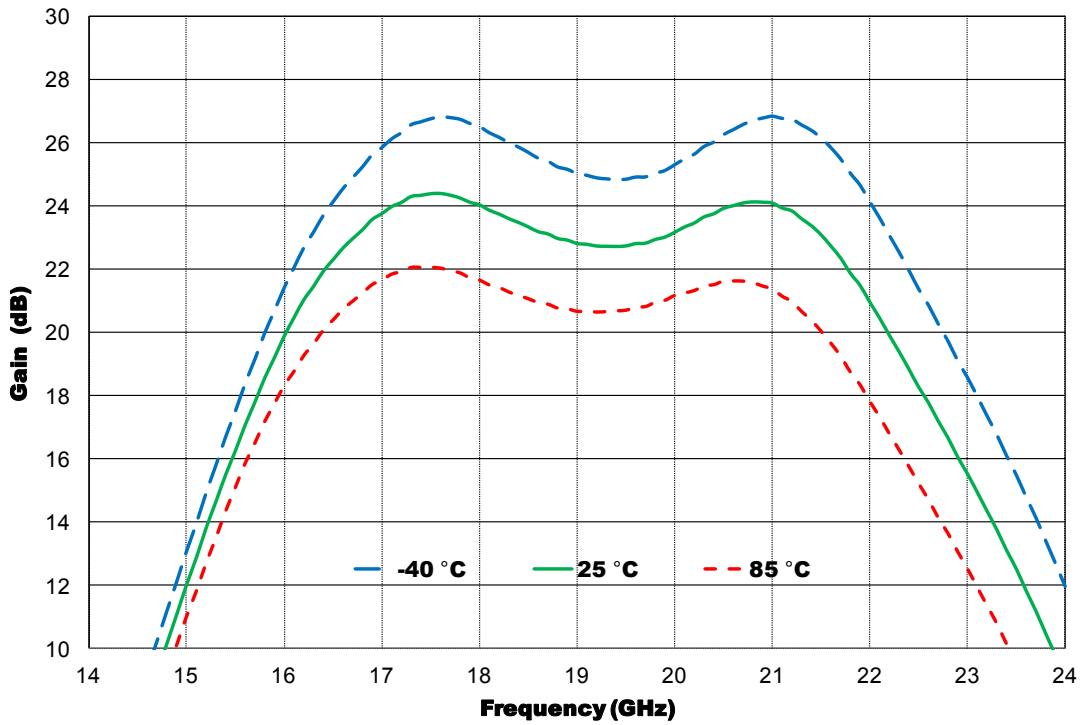




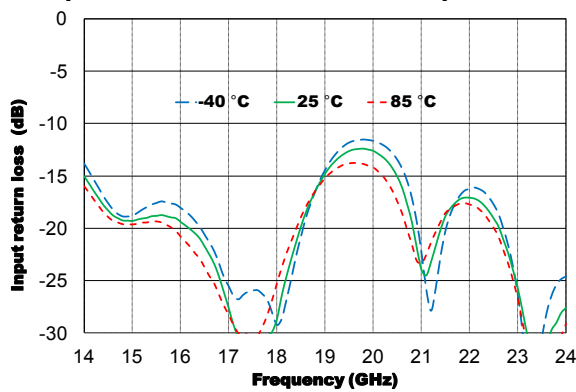
Typical board Measurements

Tamb.= +25°C, Vd = +6V, Id = 1340mA

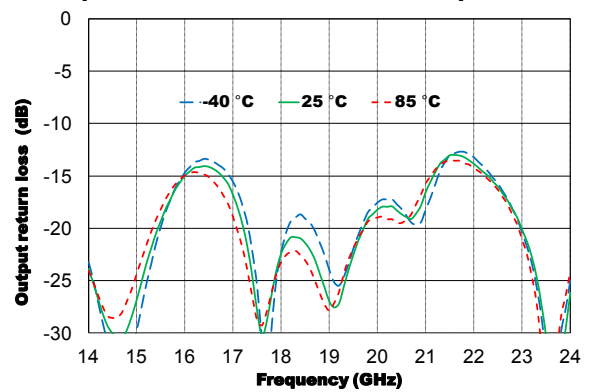
Linear Gain versus Frequency & Temperature



Input return loss versus Temperature



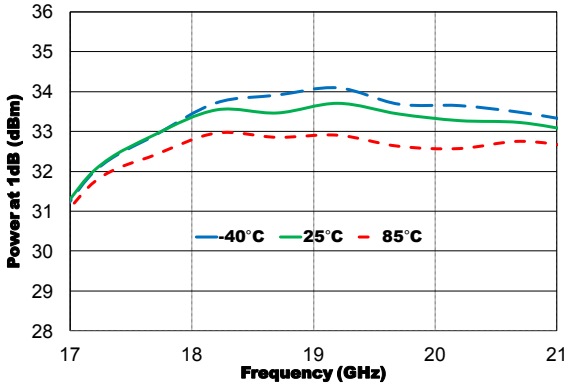
Output return loss versus Temperature



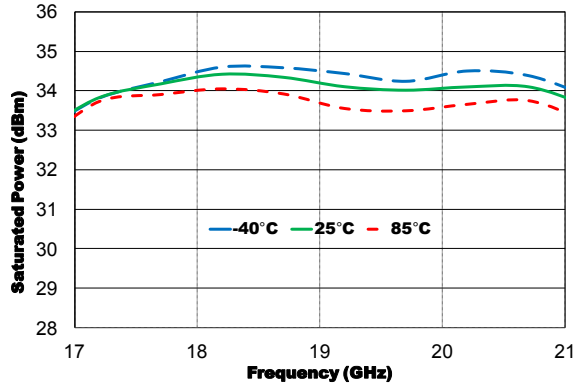
### Typical Board Measurements

Tamb.= +25°C, Vd = +6V, Id = 1340mA

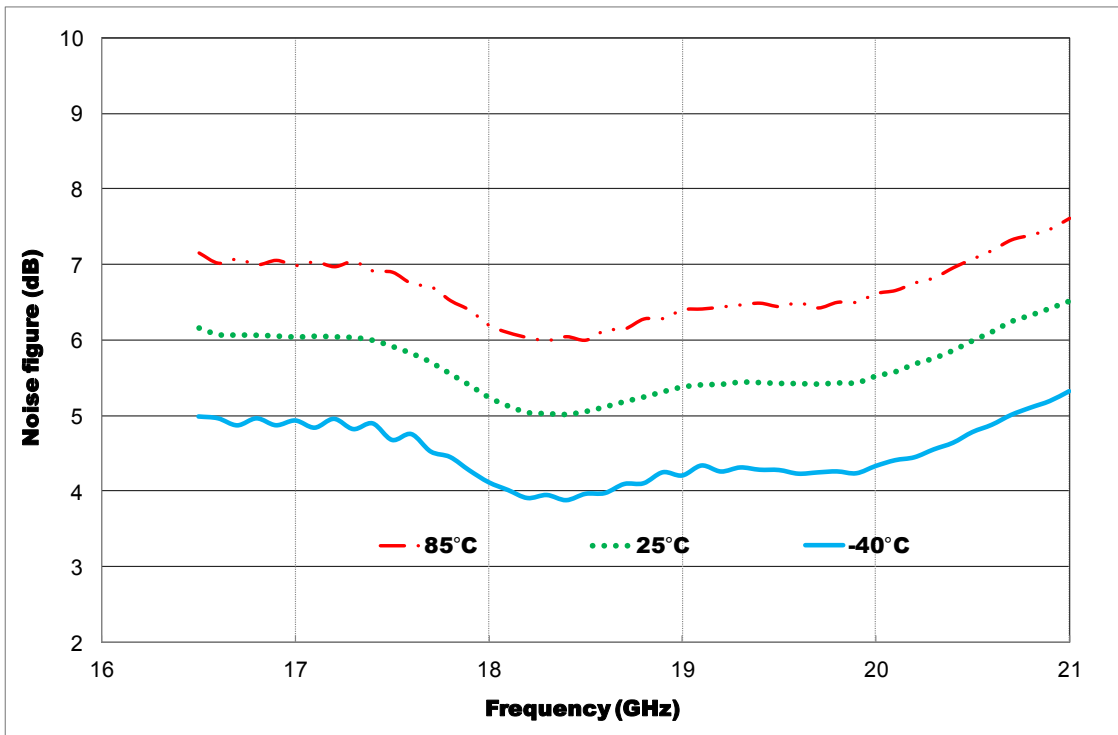
**Power at 1dB compression versus Temperature**



**Saturated Power versus Temperature**



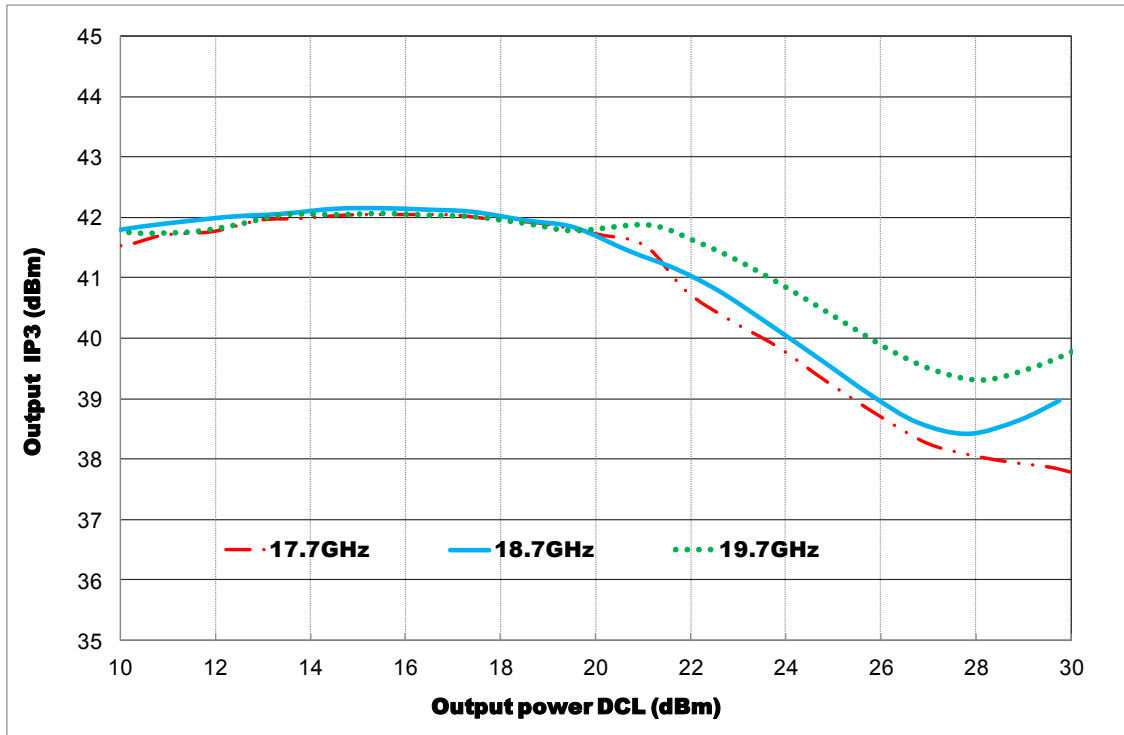
**Noise Figure versus Frequency & Temperature**



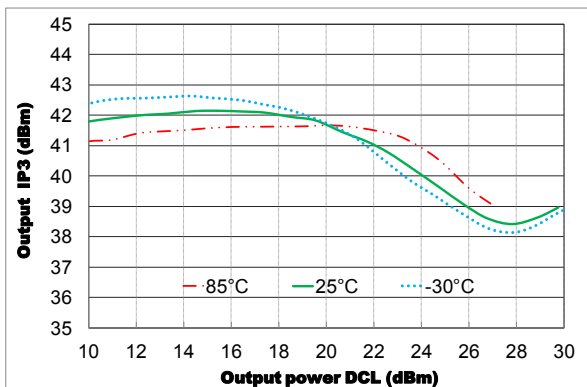
Typical Board Measurements

Tamb.= +25°C, Vd = +6V, Id = 1340mA

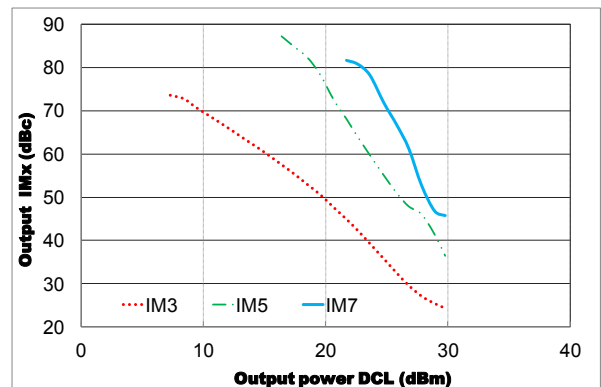
Output IP3 versus Output Power



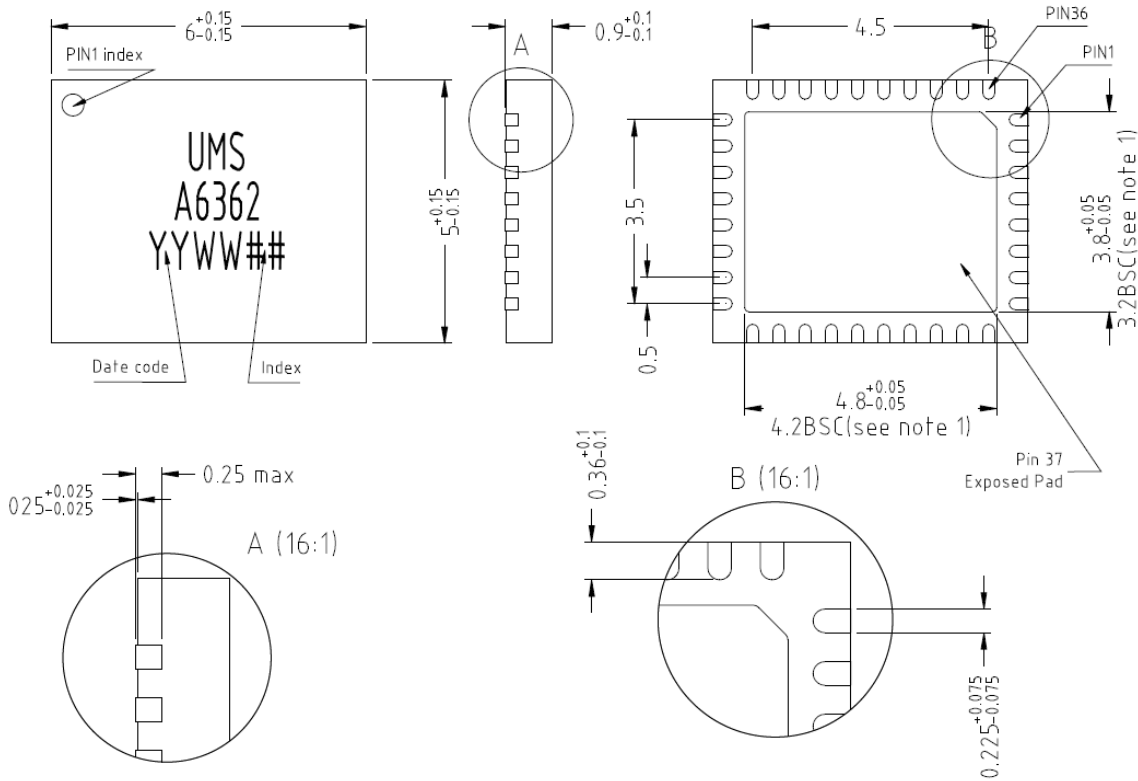
OIP3 versus temperature at 18.7GHz



IMD versus Output Power at 18.7GHz



## Package outline <sup>(1)</sup>



Note s : 1- The dimension of the exposed pad could be slightly different for fast prototyping and engineering samples:

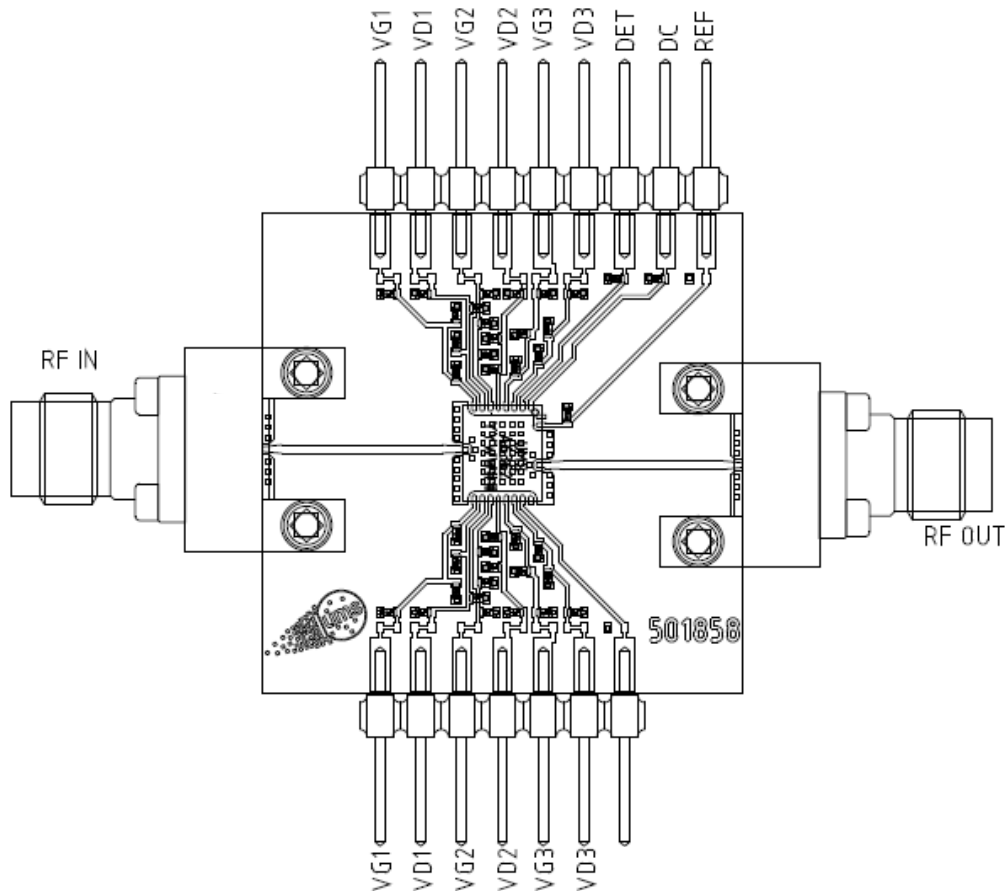
Matte tin, Lead Free (Green)	1- DC	13- RF in	25- Gnd <sup>(2)</sup>
Units : mm	2- DET	14- Gnd <sup>(2)</sup>	26- Nc
From the standard : JEDEC MO-220 (VGGD)	3- VD3	15- Nc	27- Gnd <sup>(2)</sup>
	4- VG3	16- Nc	28- Nc
37- GND	5- VD2	17- Nc	29- Gnd <sup>(2)</sup>
	6- VG2	18- Nc	30- RF out
	7- VD1	19- VG1	31- Nc
	8- VG1	20- VD1	32- Nc
	9- Nc	21- VG2	33- Nc
	10- Nc	22- VD2	34- Nc
	11- Nc	23- VG3	35- REF
	12- Nc	24- VD3	36- Nc

<sup>(1)</sup> The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (<http://www.ums-gaas.com>) for exact package dimensions.

<sup>(2)</sup> It is strongly recommended to ground all pins marked "Gnd" through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

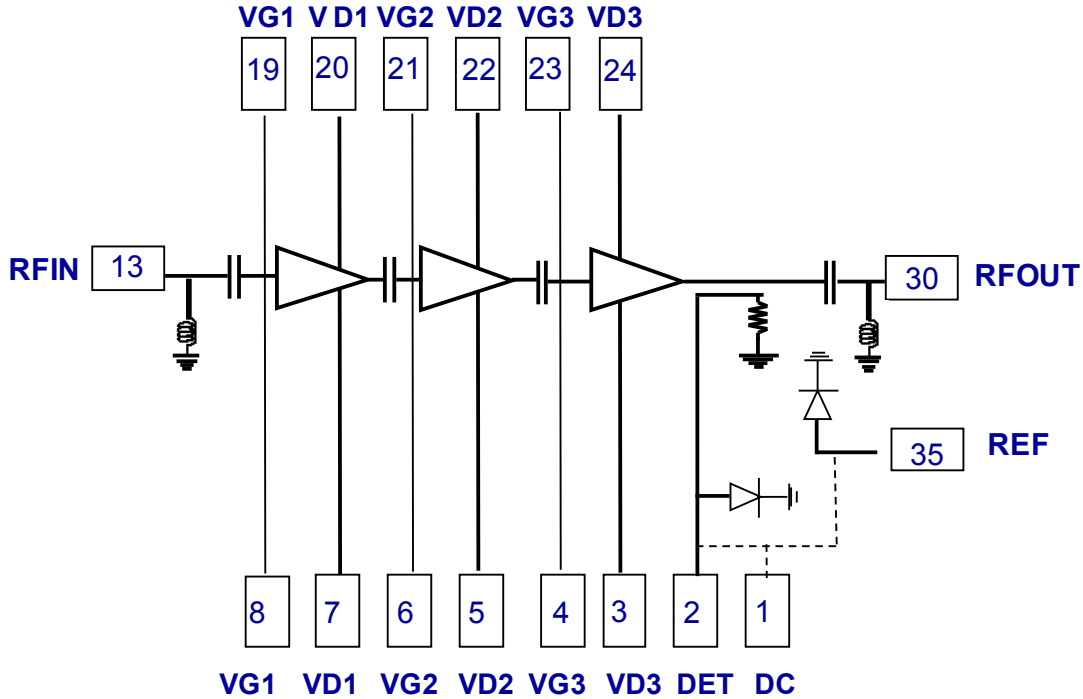
### Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4350 / 10mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 100pF  $\pm$ 5%, 10nF  $\pm$ 10% and 1 $\mu$ F  $\pm$ 10% are recommended for all DC accesses.
- A 10K $\Omega$  resistor is recommended on VREF & VDET accesses for the detector
- See application note AN0017 for details.



### Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.



The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (100pF, 10nF, 1µF) on the PC board, as close as possible to the package.

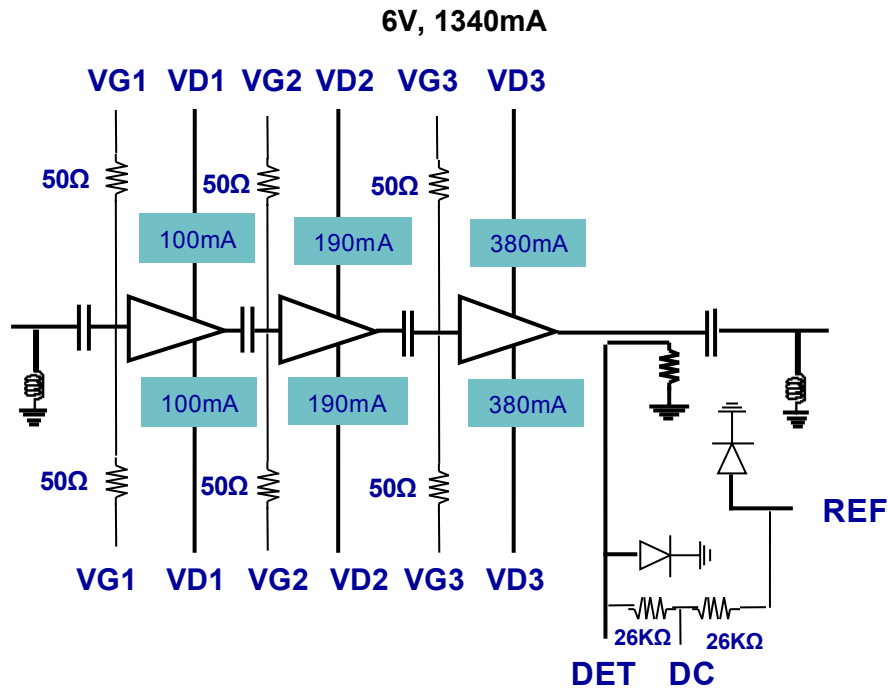
A 10KΩ resistor is recommended in parallel to VDET, and VREF accesses.

The circuit includes ESD protections on all RF and DC leads

### Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% matte tin ( Sn)
MSL Rating	MSL3

**DC Schematic**



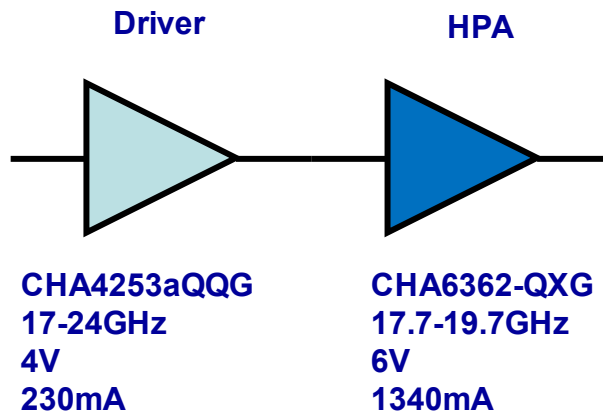
**Recommended UMS Power chain**

The CHA6362-QXG could be associated with the CHA4253aQQG as driver.

Total Gain: 46dB

Gain control: 30dB with the both amplifiers.

For more information, please see the datasheet CHA4253aQQG



## Recommended package footprint

Refer to the application note AN0017 available at <http://www.ums-gaas.com> for package footprint recommendations.

## SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

## Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <http://www.ums-gaas.com>.

## Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS package products.

## Ordering Information

QFN 5x6 package:

CHA6362-QXG/XY

Stick: XY = 20

Tape & reel: XY = 21

Information furnished is believed to be accurate and reliable. However **United Monolithic Semiconductors S.A.S.** assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of **United Monolithic Semiconductors S.A.S.** Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. **United Monolithic Semiconductors S.A.S.** products are not authorised for use as critical components in life support devices or systems without express written approval from **United Monolithic Semiconductors S.A.S.**