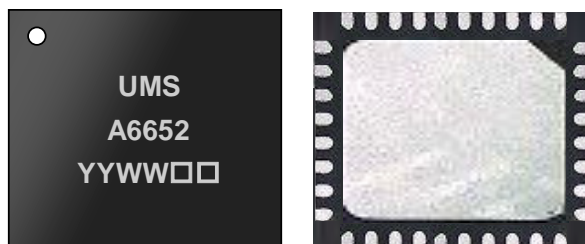


21- 27.5GHz Power Amplifier

GaAs Monolithic Microwave IC in SMD leadless package

Description

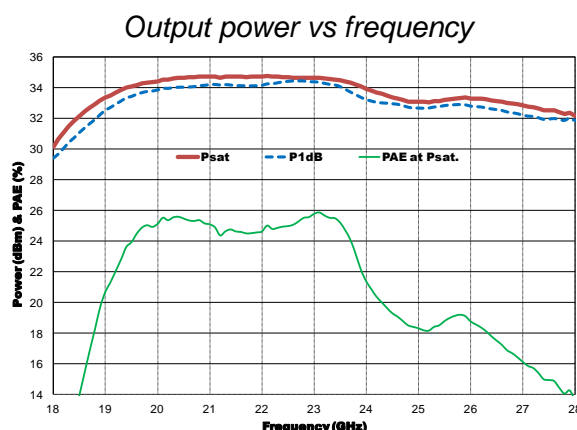
The CHA6652-QXG is a three stage monolithic GaAs high power circuit producing 2 Watt output power. It is highly linear, with possible gain control and integrates a power detector. ESD protections are included. It is designed for Point To Point Radio. The circuit is manufactured with a pHEMT process, 0.15µm gate length. It is supplied in RoHS compliant SMD package.



36 lead 6x5 mm QFN package

Main Features

- Broadband performances: 21- 27.5GHz
- 33dBm saturated power
- 41dBm OIP3
- 20dB gain
- DC bias: Vd = 6.0Volt @ Id = 1.3A
- QFN 6x5
- MSL3



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	21		27.5	GHz
Gain	Linear Gain		20		dB
Psat	Saturated output power		33		dBm
OIP3	Output IP3		41		dBm

Electrical Characteristics

Tamb.= +25°C, Vd = +6.0V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	21		27.5	GHz
Gain	Small Signal Gain in 21 - 24GHz		22		dB
	Small Signal Gain in 24.25 - 27.5GHz		20		
ΔG	Gain variation in temperature		± 0.03		dB/°C
Psat	Saturated Output Power in 21 - 24GHz		34.5		dBm
	Saturated Output Power in 24.25 - 26.5GHz		33		
	Saturated Output Power in 26.75 - 27.5GHz		32.5		
OIP3	Output IP3 in 21 - 26.5GHz		41		dBm
	Output IP3 in 26.75 - 27.5GHz		39		
PAE	PAE at saturation in 21 - 24GHz		25		%
	PAE at saturation in 24.25 - 27.5GHz		18		
CG	Gain control range		15		dB
Rlin	Input Return Loss in 21 - 24GHz		12		dB
	Input Return Loss in 24.25 - 27.5GHz		15		
Rlout	Output Return Loss		25		dB
NF	Noise figure at nominal gain		5		dB
Dr	Detection dynamic range(for output power detection up to Psat)		30		dB
Vdetect	Voltage detection $V_{REF} - V_{DET}$ up to Psat		10 to 1500		mV
Vg	DC gate Voltage		-0.65		V
Idq	Total drain current		1.3		A

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

Absolute Maximum Ratings ⁽¹⁾

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	DC Drain bias voltage without RF	8	V
Id	Drain bias quiescent current	1600	mA
Vg	Gate bias voltage	-2 to 0	V
Pin	Maximum Input Power	+15	dBm
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

⁽¹⁾ Operation of this device above any one of these parameters may cause permanent damage.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad N°	Parameter	Values	Unit
Vd1	7, 20	DC Drain voltage 1 st stage	6.0	V
Vd2	5, 22	DC Drain voltage 2 nd stage	6.0	V
Vd3	3, 24	DC Drain voltage 3 rd stage	6.0	V
Vg1	8, 19	DC Gate voltage 1 st stage	-0.65	V
Vg2	6, 21	DC Gate voltage 2 nd stage	-0.65	V
Vg3	4, 23	DC Gate voltage 3 rd stage	-0.65	V

Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is only cooled down by conduction through the package thermal pad (no convection mode considered).

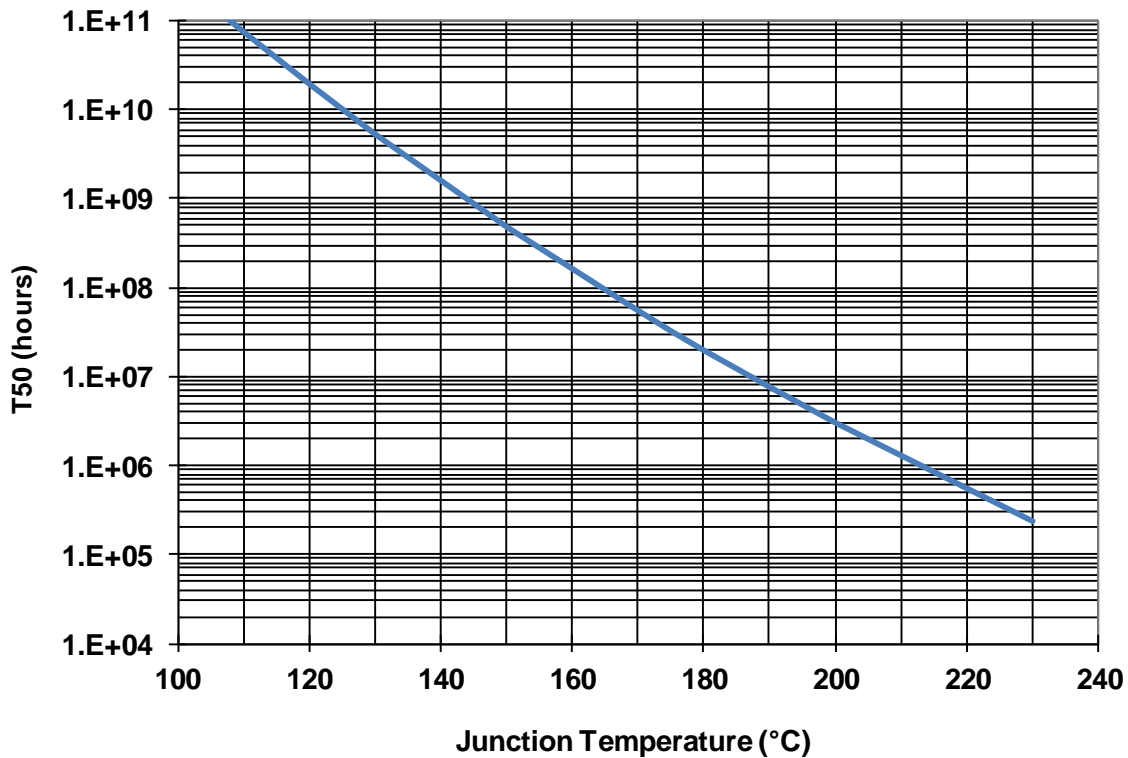
The temperature is monitored at the package back-side interface (Tcase).

The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Absolute Maximum Ratings table.

So, the system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	Tjunction (°C)	R _{TH} (°C/W)	T50 (hours)
R _{TH} ⁽¹⁾ Thermal Resistance (Junction to Case)	Vd= 6V Id= 1300mA Pdis= 7.8W	176	11.8	3.0E+07

⁽¹⁾ Assuming 85°C Tcase



Typical Package Sij parameters

Tamb.= +25°C, Vd = +6.0V, Id = 1300mA

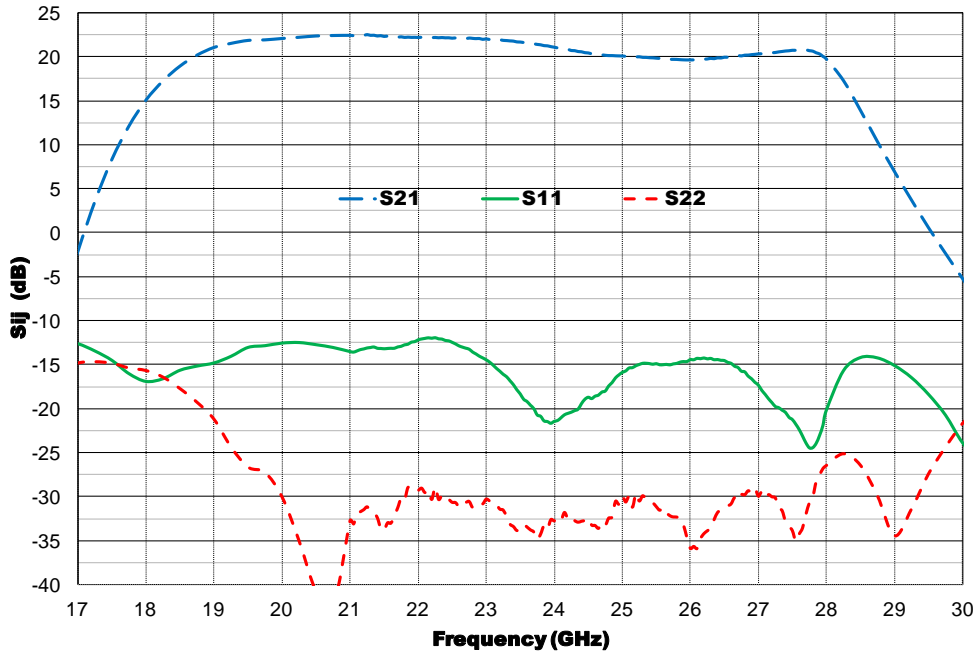
Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
1	-0.169	161.7	-87.033	51.9	-78.505	59.9	-0.208	160.9
2	-0.183	143.3	-71.756	63.1	-72.361	38.4	-0.293	141.9
3	-0.239	124.9	-74.904	64.1	-70.501	40.0	-0.312	122.6
4	-0.296	105.7	-67.935	49.1	-63.022	15.6	-0.375	102.5
5	-0.308	86.5	-68.950	-2.6	-57.334	-33.3	-0.484	82.2
6	-0.534	64.8	-64.421	-25.0	-50.447	-127.7	-0.655	60.5
7	-0.985	42.9	-64.244	-52.2	-46.006	120.2	-0.985	38.1
8	-2.043	19.3	-71.085	-89.8	-42.426	26.7	-1.692	17.5
9	-4.367	2.9	-69.740	-36.9	-42.000	-63.5	-2.071	-1.4
10	-4.249	-3.6	-68.116	-86.7	-45.429	-127.0	-2.176	-22.2
11	-3.477	-26.1	-62.689	-123.3	-42.508	177.7	-2.314	-45.8
12	-3.701	-54.8	-66.773	-156.6	-51.614	30.9	-2.668	-71.2
13	-5.133	-88.3	-56.036	-173.3	-57.289	-177.9	-3.360	-101.4
14	-8.956	-128.4	-48.460	104.5	-48.238	102.2	-5.214	-138.5
15	-24.424	-177.0	-48.849	60.2	-47.219	57.0	-10.275	-179.9
16	-14.597	-47.5	-50.514	31.7	-29.625	21.2	-24.490	-154.0
17	-12.631	-94.0	-50.703	-3.8	-2.099	-104.4	-14.846	-143.6
18	-16.922	-101.9	-50.198	-18.5	15.073	74.5	-15.697	176.7
19	-14.816	-96.1	-49.794	-37.3	21.049	-96.2	-21.241	127.7
20	-12.559	-115.3	-49.906	-71.8	22.066	123.3	-30.079	89.9
21	-13.530	-134.7	-53.073	-134.0	22.421	2.0	-32.742	-43.7
22	-12.188	-151.3	-60.703	15.2	22.183	-110.7	-29.328	-123.0
23	-14.467	169.1	-48.472	-18.1	22.017	141.1	-30.319	-155.3
24	-21.466	-179.6	-48.853	-28.7	21.074	33.2	-32.789	-174.3
25	-15.895	-167.5	-47.864	-27.5	20.073	-68.1	-29.963	131.8
26	-14.439	159.9	-42.218	-48.5	19.630	-172.9	-35.908	23.1
27	-17.337	118.3	-38.879	-86.8	20.312	71.5	-29.981	-12.7
28	-20.184	171.8	-43.908	-118.7	19.736	-83.8	-26.490	-27.2
29	-15.111	102.5	-40.171	-118.8	6.952	131.2	-34.483	155.2
30	-23.891	79.3	-37.658	-140.3	-5.205	36.1	-21.718	2.0
31	-19.903	128.1	-36.130	-165.6	-16.093	-51.1	-15.452	-62.0
32	-14.856	90.5	-37.695	155.3	-25.483	-135.8	-11.802	-118.4
33	-13.093	31.4	-40.644	136.3	-32.569	156.5	-9.894	-171.7
34	-11.357	-43.0	-41.742	133.4	-38.565	114.5	-9.805	138.4
35	-7.736	-115.1	-41.327	144.2	-43.173	141.7	-13.682	92.7
36	-4.822	-171.1	-38.996	125.3	-39.500	135.9	-23.947	146.1
37	-2.986	146.2	-43.049	98.0	-42.143	107.0	-11.253	160.1
38	-1.917	110.9	-43.547	129.2	-42.192	126.1	-4.672	129.7
39	-1.526	81.2	-38.211	116.0	-37.937	117.8	-2.085	90.3
40	-1.307	55.3	-34.786	95.5	-35.185	93.7	-1.474	59.7

Typical Board Measurements

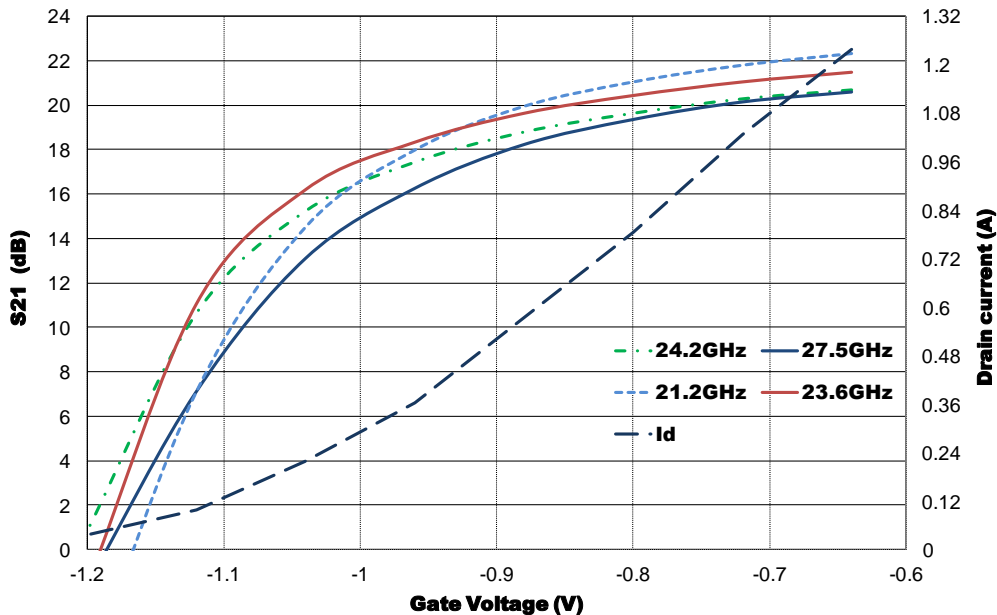
Tamb.= +25°C, Vd = +6.0V, Id = 1300mA

Measurement performed in the access plans of the QFN, using the proposed land pattern & board, as defined in paragraph "Evaluation mother board"

Gain & Return Loss versus Frequency

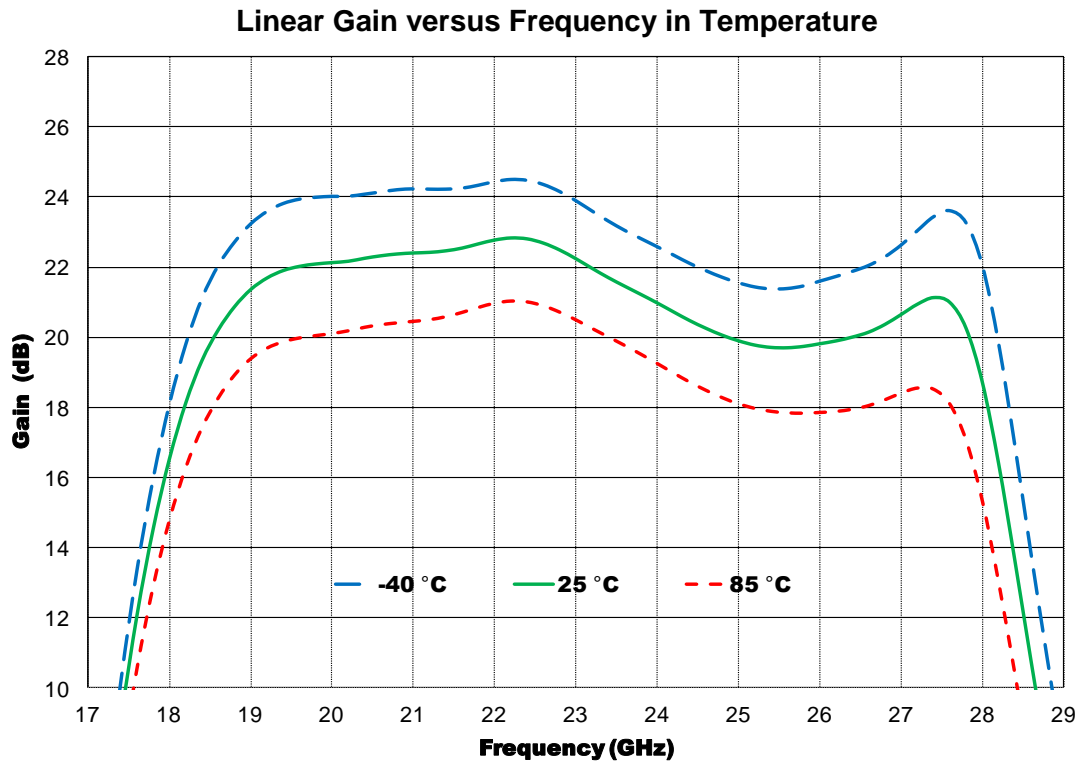
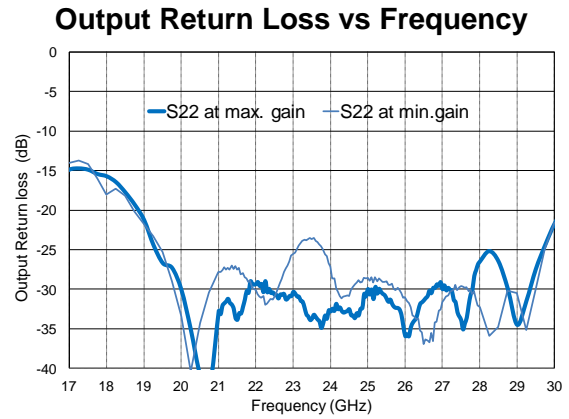
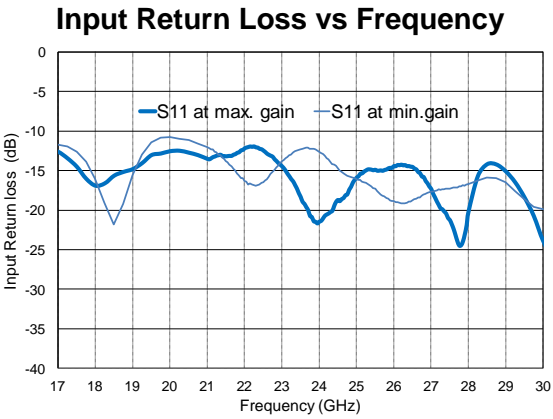


Gain control & current versus Gate Voltage



Typical Board Measurements

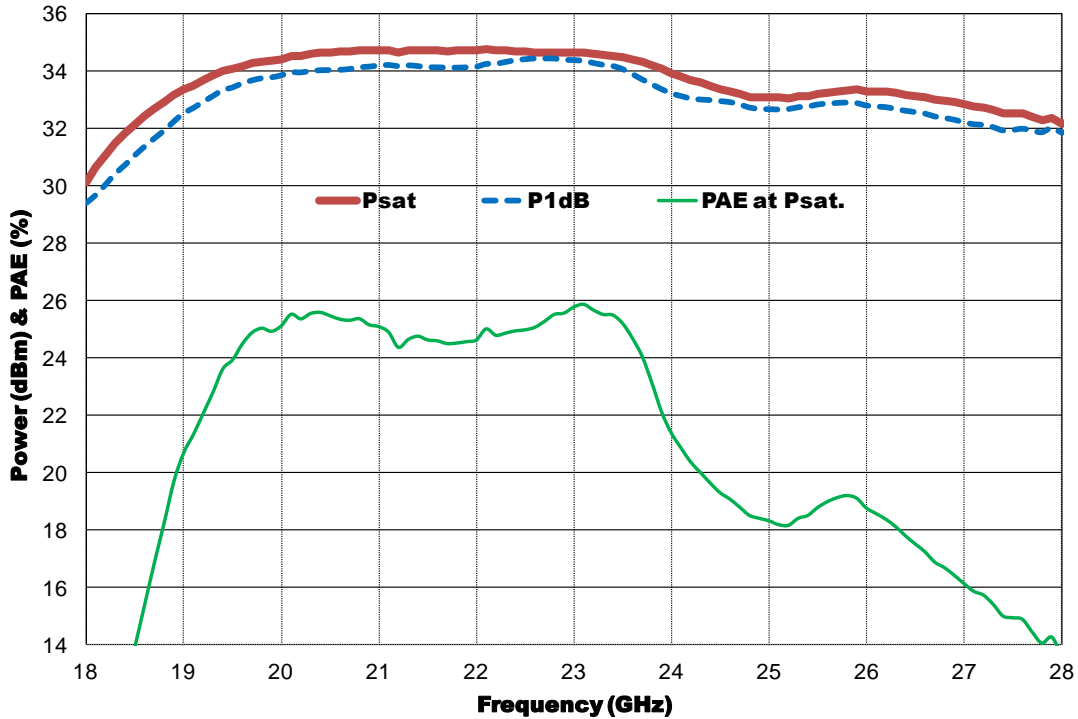
Tamb.= +25°C, Vd = +6.0V, Id = 1300mA



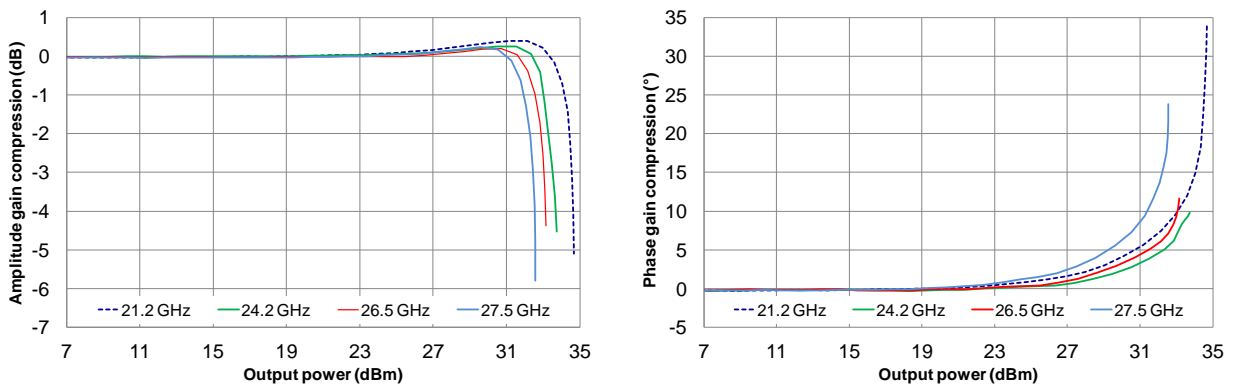
Typical Board Measurements

Tamb.= +25°C, Vd = +6.0V, Id = 1300mA

Output power & PAE versus Frequency

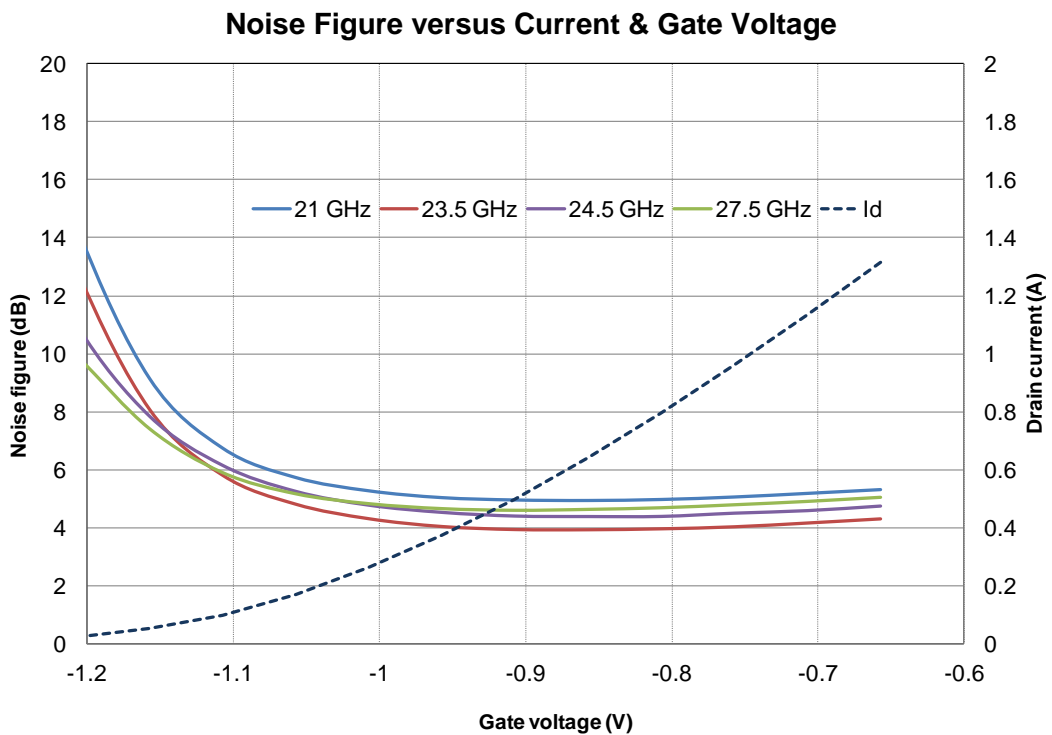
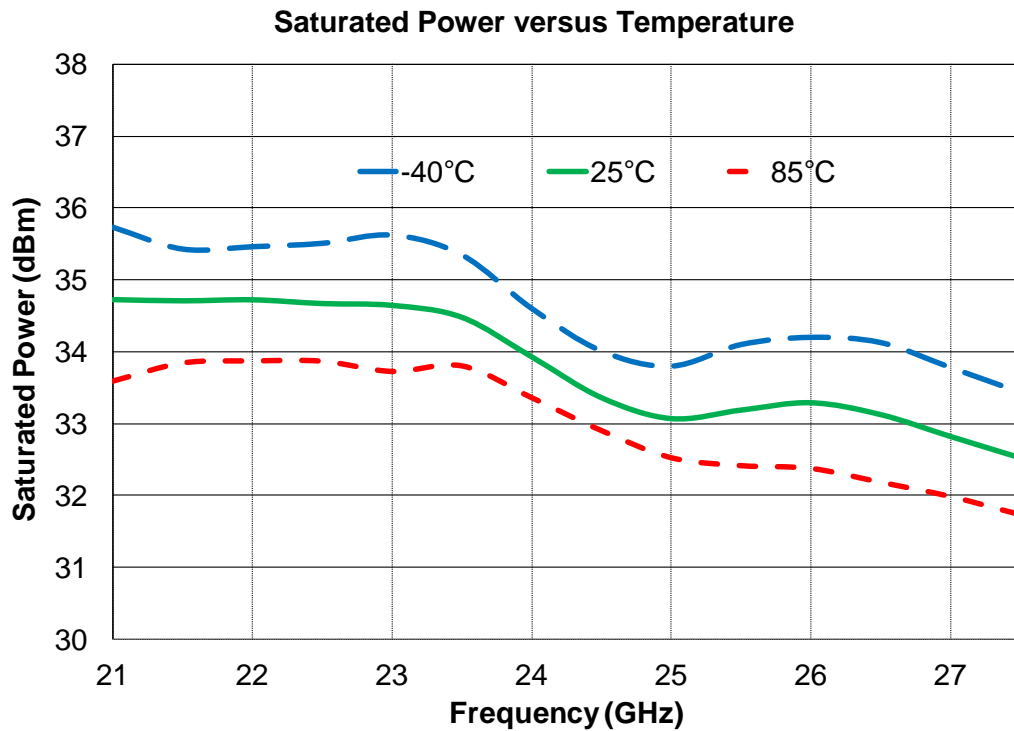


Amplitude & Phase variation versus Output Power



Typical Board Measurements

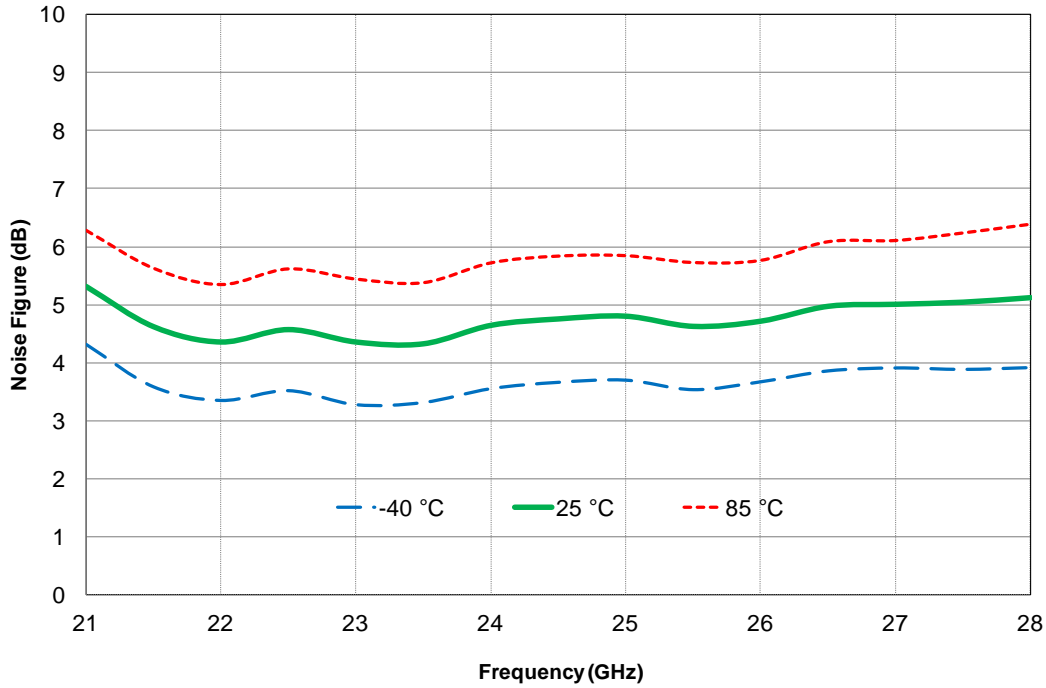
Tamb.= +25°C, Vd = +6.0V, Id = 1300mA



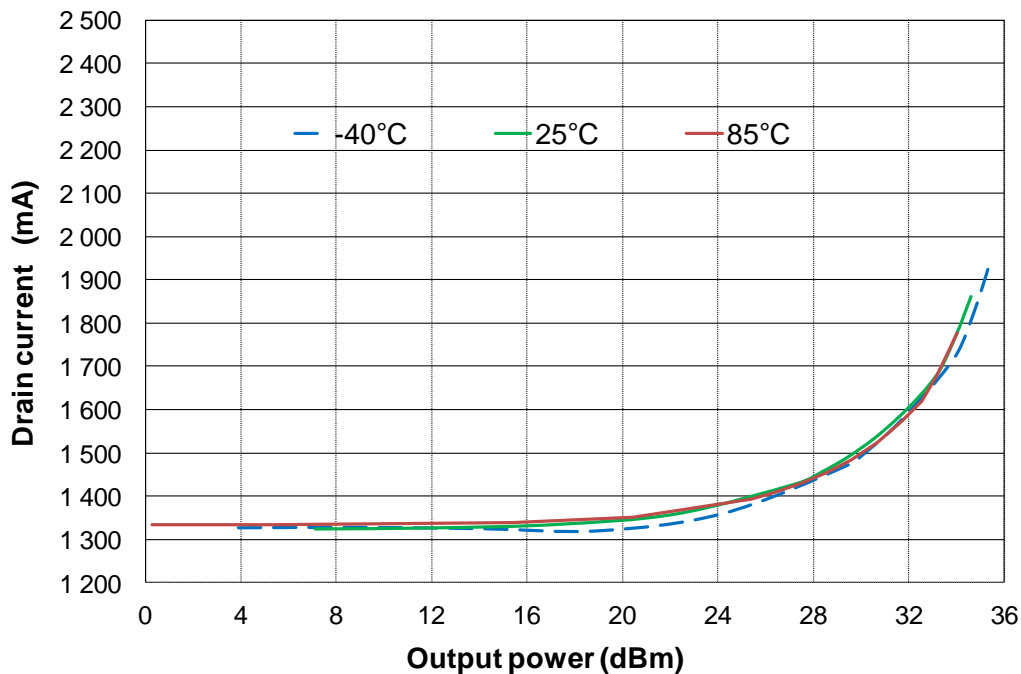
Typical Board Measurements

Tamb.= +25°C, Vd = +6.0V, Id = 1300mA

Noise figure versus Temperature



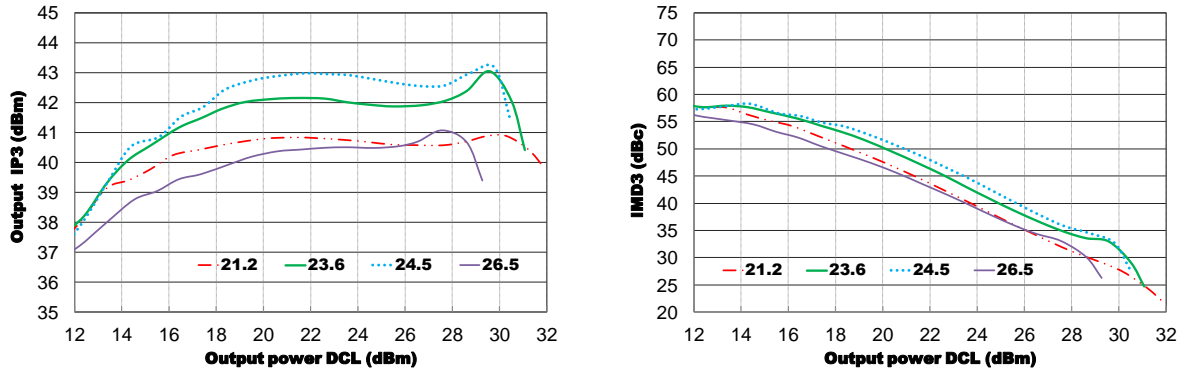
Drain current versus Output Power



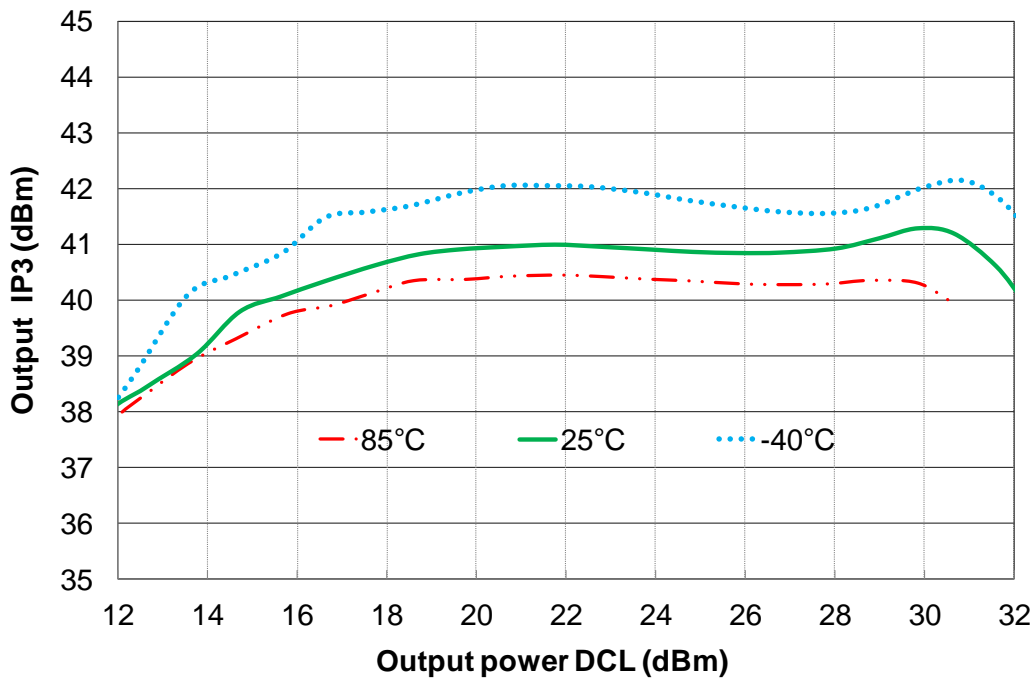
Typical Board Measurements

Tamb.= +25°C, Vd = +6.0V, Id = 1300mA

Output IP3 & IMD3 versus Output Power

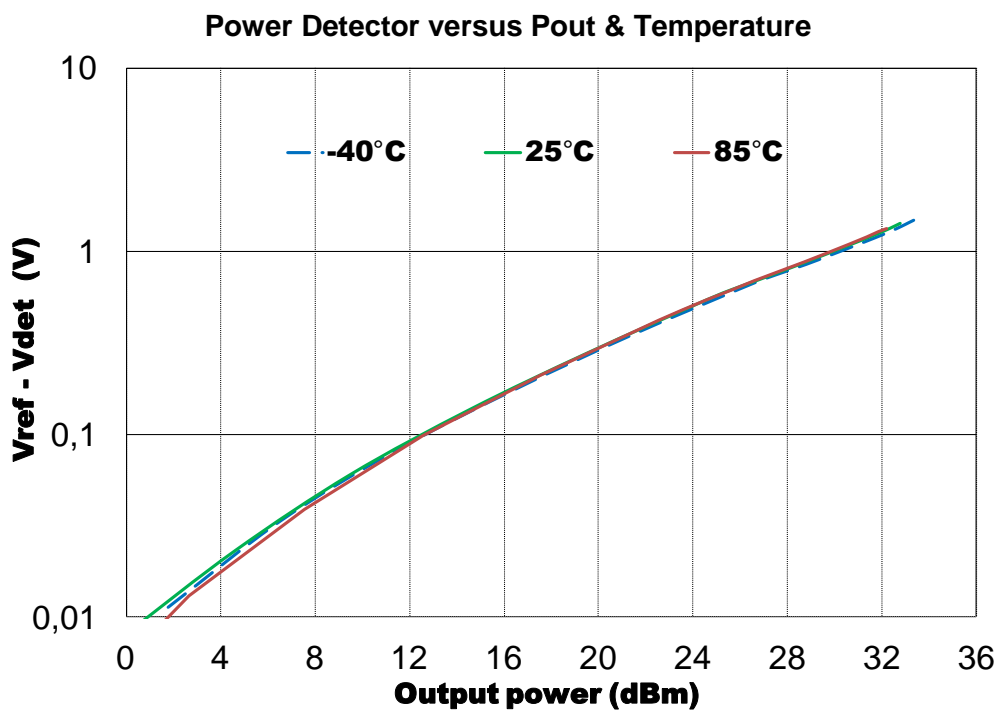
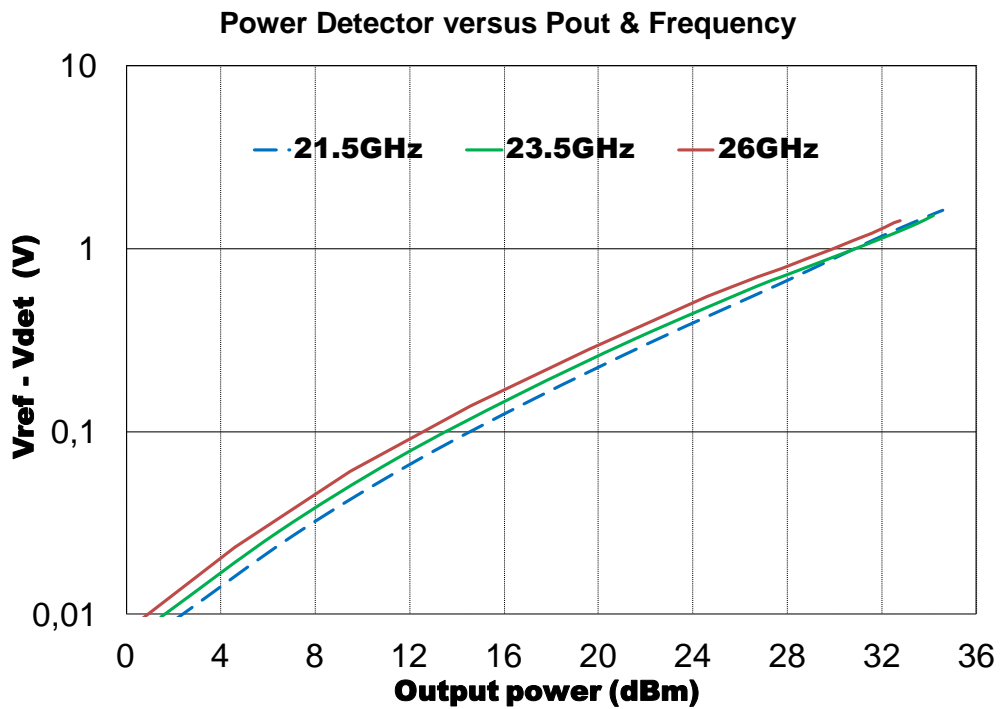


Output IP3 with temperature at 21.2GHz

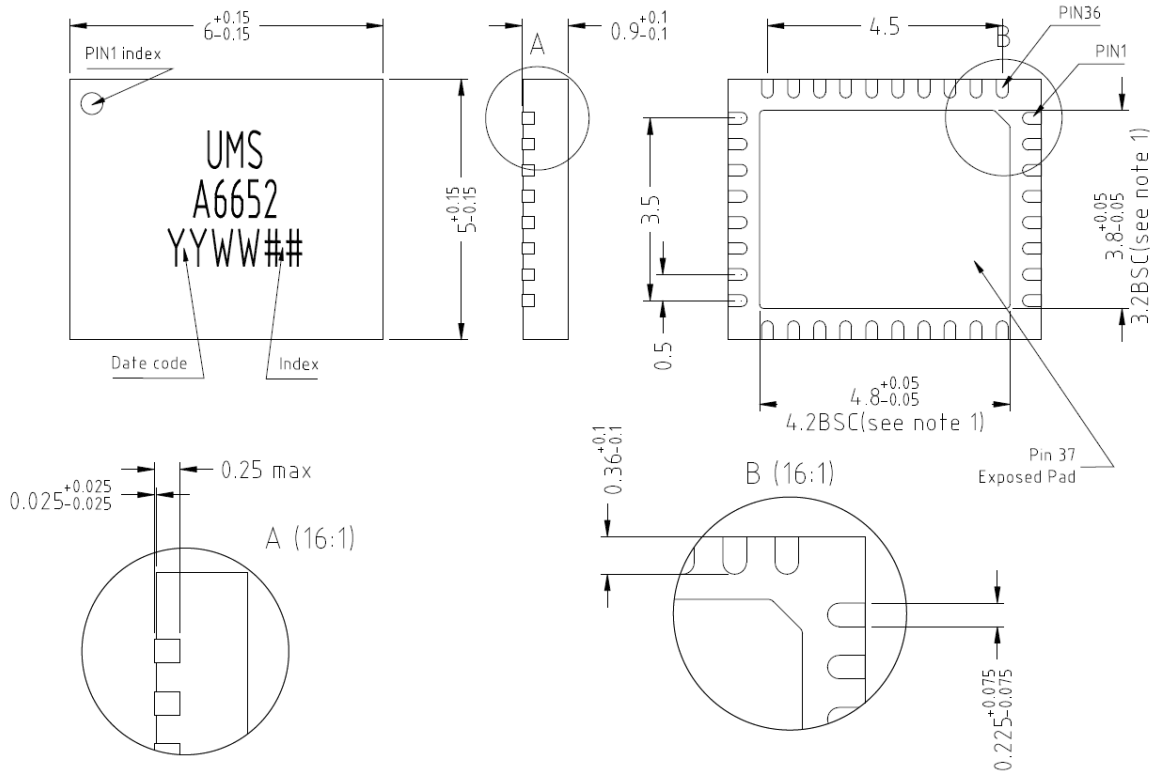


Typical Board Measurements

Tamb.= +25°C, Vd = +6.0V, Id = 1300mA



Package outline ⁽¹⁾



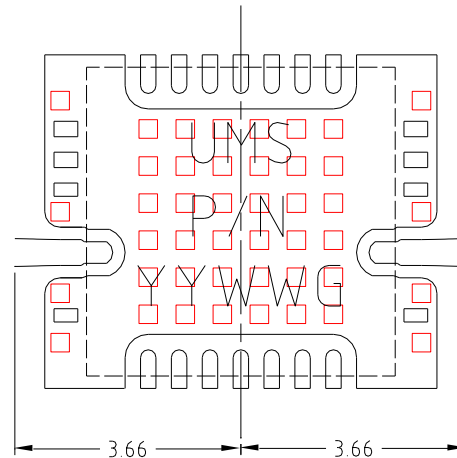
Matte tin, Lead Free (Green)	1- NC	13- RF in	25- NC
Units : mm	2- DET	14- Gnd ⁽²⁾	26- NC
From the standard : JEDEC MO-220 (VGGD)	3- Vd3	15- NC	27- Gnd ⁽²⁾
	4- Vg3	16- NC	28- NC
37- GND	5- Vd2	17- NC	29- Gnd ⁽²⁾
	6- Vg2	18- NC	30- RF out
	7- Vd1	19- Vg1	31- NC
	8- Vg1	20- Vd1	32- NC
	9- NC	21- Vg2	33- NC
	10- NC	22- Vd2	34- NC
	11- NC	23- Vg3	35- REF
	12- NC	24- Vd3	36- NC

⁽¹⁾ The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (<http://www.ums-gaas.com>) for exact package dimensions.

⁽²⁾ It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.66mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".



ESD sensitivity

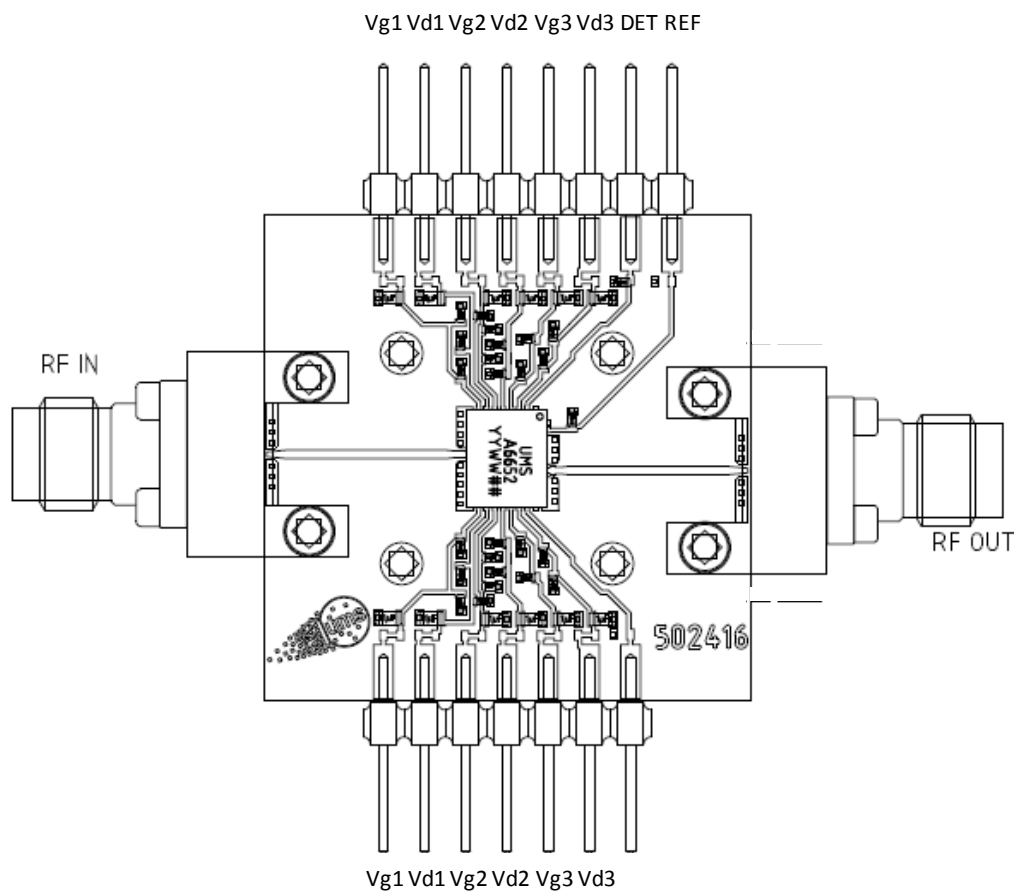
Standard	Value
MIL-STD-1686C	HBM Class 1 (<2000V)

Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% matte tin (Sn)
MSL Rating	MSL3

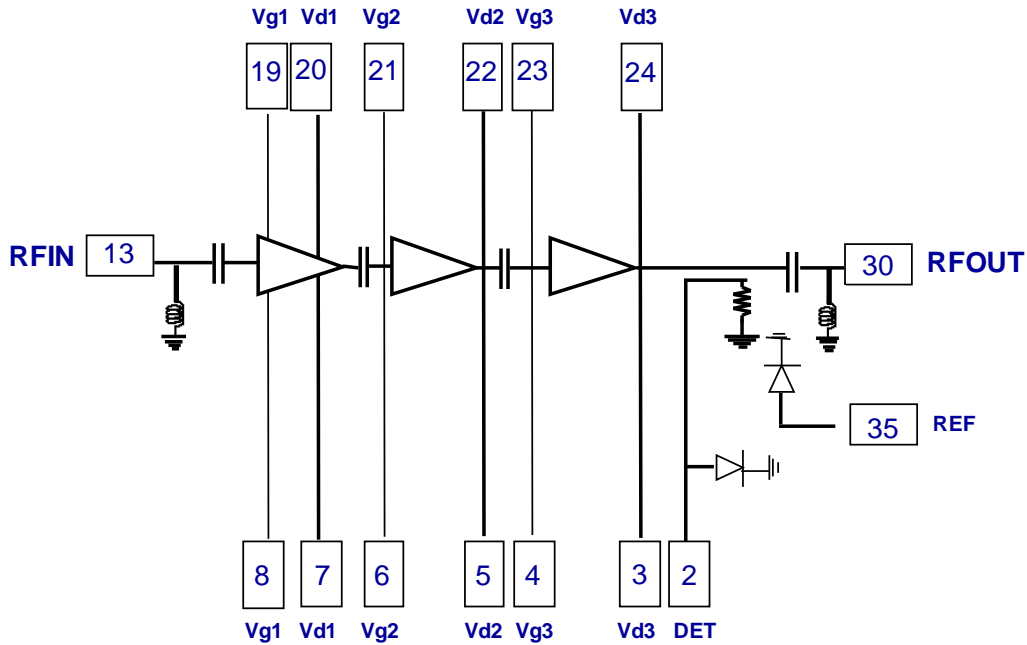
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4350 / 10mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 22pF $\pm 5\%$, 10nF $\pm 10\%$ and 1 μ F $\pm 10\%$ are recommended for the gate accesses.
- Decoupling capacitors of 100pF $\pm 5\%$, 10nF $\pm 10\%$ and 1 μ F $\pm 10\%$ are recommended for the drain accesses.
- A 10K Ω resistor is recommended on VREF & VDET accesses for the detector
- See application note AN0017 for details.



Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.



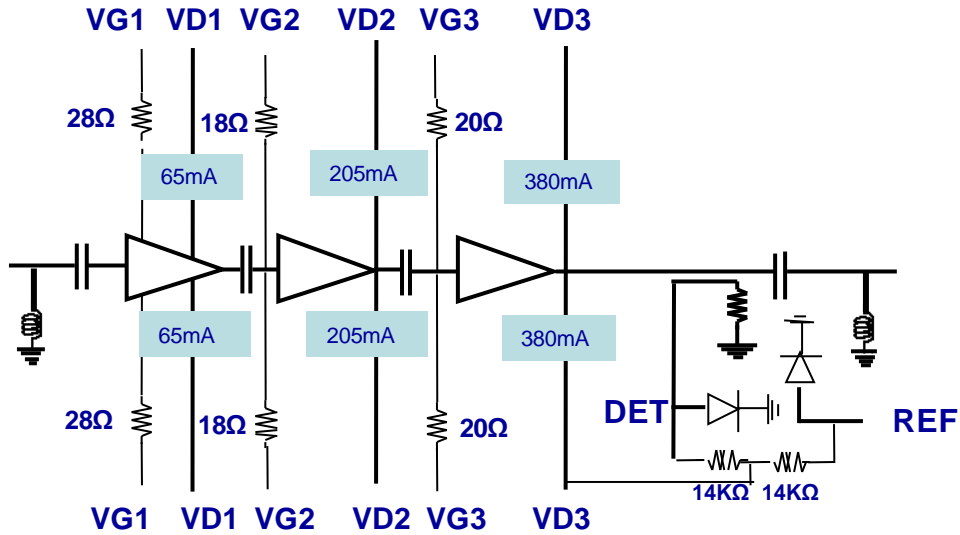
The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (See paragraph “Evaluation mother board”) on the PC board, as close as possible to the package.

A 10KΩ resistor is recommended in parallel to VDET, and VREF accesses.

The circuit includes ESD protections on all RF and DC leads

DC Schematic

6V, 1300mA



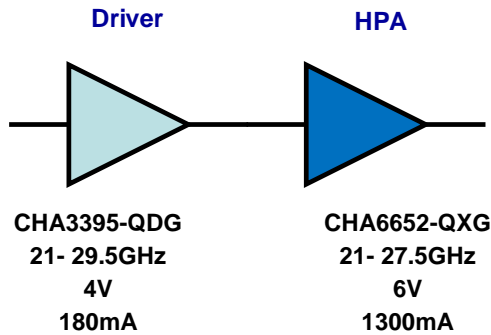
Recommended UMS Power chain

The CHA6652-QXG is recommended with the CHA3395-QDG as driver.

Total Gain: 44dB

Gain control: 30dB with the both amplifiers.

For more information about the CHA3395-QDG, see our web site www.ums-gaas.com



Recommended package footprint

Refer to the application note AN0017 available at <http://www.ums-gaas.com> for package footprint recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <http://www.ums-gaas.com>.

Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 6x5 package:

CHA6652-QXG/XY

Stick: XY = 20

Tape & reel: XY = 21

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