United Monolithic Semiconductors

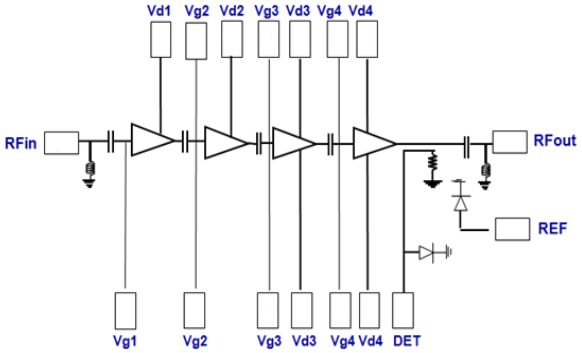
# CHA6653-98F

# 27-34GHz Power Amplifier

## GaAs Monolithic Microwave IC

## Description

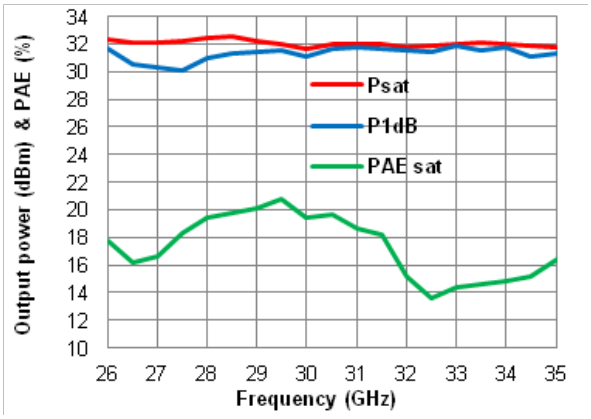
The CHA6653-98F is a four stages monolithic GaAs High Power Amplifier producing 1.8 Watt output power. It is highly linear, with gain control capability and integrates a power detector. ESD protections are included.
It is designed for Telecommunication application.
The circuit is manufactured with a pHEMT process, 0.15µm gate length.




## Main Features

- Broadband performances: 27-34GHz
- 32dBm saturated power
- 38dBm OIP3
- 23dB gain
- DC bias: Vd = 6.0Volt @ Idq = 0.9A
- Chip size 3.61x3.46x0.07mm

Output power & PAE vs frequency




## Main Electrical Characteristics

Tamb.= +25°C

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Freq | Frequency range | 27 | | 34 | GHz |
| Gain | Linear Gain | | 23 | | dB |
| Psat | Saturated output power | | 32 | | dBm |
| OIP3 | Output IP3 | | 38 | | dBm |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## Specifications

Tamb.= +25°C, Vd = +6.0V

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Fop | Operating frequency range | 27 | | 34 | GHz |
| Gain | Small Signal Gain | | 23 | | dB |
| ΔG | Gain variation in temperature | | ± 0.04 | | dB/°C |
| Psat | Saturated Output Power | | 32 | | dBm |
| OIP3 | Output IP3 | | 38 | | dBm |
| P1dB | Pout at 1dB of compression | | 31 | | dBm |
| PAE | PAE at saturation | | 17 | | % |
| CG | Gain control range | | 15 | | dB |
| Rlin | Input Return Loss | | 8 | | dB |
| Rlout | Output Return Loss | | 10 | | dB |
| Dr | Detection dynamic range(for output power detection up to Psat) | | 30 | | dB |
| Vdetect | Voltage detection $V_{REF}$- $V_{DET}$ up to Psat | | 20 to 2000 | | mV |
| Vg | DC gate Voltage | | -0.65 | | V |
| Idq | Total drain current | | 0.9 | | A |

These values are representative of on-board measurements.
Electrostatic discharge sensitive device observe handling precautions!



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## Absolute Maximum Ratings [1, 2]

Tamb.= +25°C

| Symbol | Parameter | Values | Unit |
|---|---|---|---|
| Vd | Drain bias voltage | 8 | V |
| Id | Drain bias current | 2050 | mA |
| Vg | Gate bias voltage | -2 to 0 | V |
| Vdg | External drain-gate excursion | 10 | V |
| Pin | Maximum Input Power | +15 | dBm |
| Tj | Maximum Junction temperature | 175 | °C |

[1] Operation of this device above anyone of these parameters may cause permanent damage.

[2] These are stress rating only, and functional operation of the devices at these conditions is not implies.

## Recommanded Operating Range [3, 4]

| Symbol | Parameter | Values | Unit |
|---|---|---|---|
| Vd | Drain bias voltage | 5 to 6 | V |
| Id | Drain bias current | 730 to 900 | mA |
| Vg | Gate bias voltage | -2 to 0 | V |
| Pin | Maximum peak input power overdrive | 15 | dBm |
| Ta | Operating temperature range | -40 to 95 | °C |

[3] Electrical performances are defined for specified test conditions

[4] Electrical performances are not guaranteed over all recommended operating conditions

## Temperature Range

| | | | |
|---|---|---|---|
| Ta | Operating temperature range | -40 to +95 | °C |
| Tstg | Storage temperature range | -55 to +150 | °C |

## Typical Bias Conditions

Tamb= +25°C

| Symbol | Parameter | Values | Unit |
|---|---|---|---|
| Vd1 | DC Drain voltage 1st stage | 6V | V |
| Vd2 | DC Drain voltage 2nd stage | 6V | V |
| Vd3 | DC Drain voltage 3rd stage | 6V | V |
| Vd4 | DC Drain voltage 4th stage | 6V | V |
| Vg1 | DC Gate voltage 1st stage | -0.65 | V |
| Vg2 | DC Gate voltage 2nd stage | -0.65 | V |
| Vg3 | DC Gate voltage 3rd stage | -0.65 | V |
| Vg4 | DC Gate voltage 4th stage | -0.65 | V |



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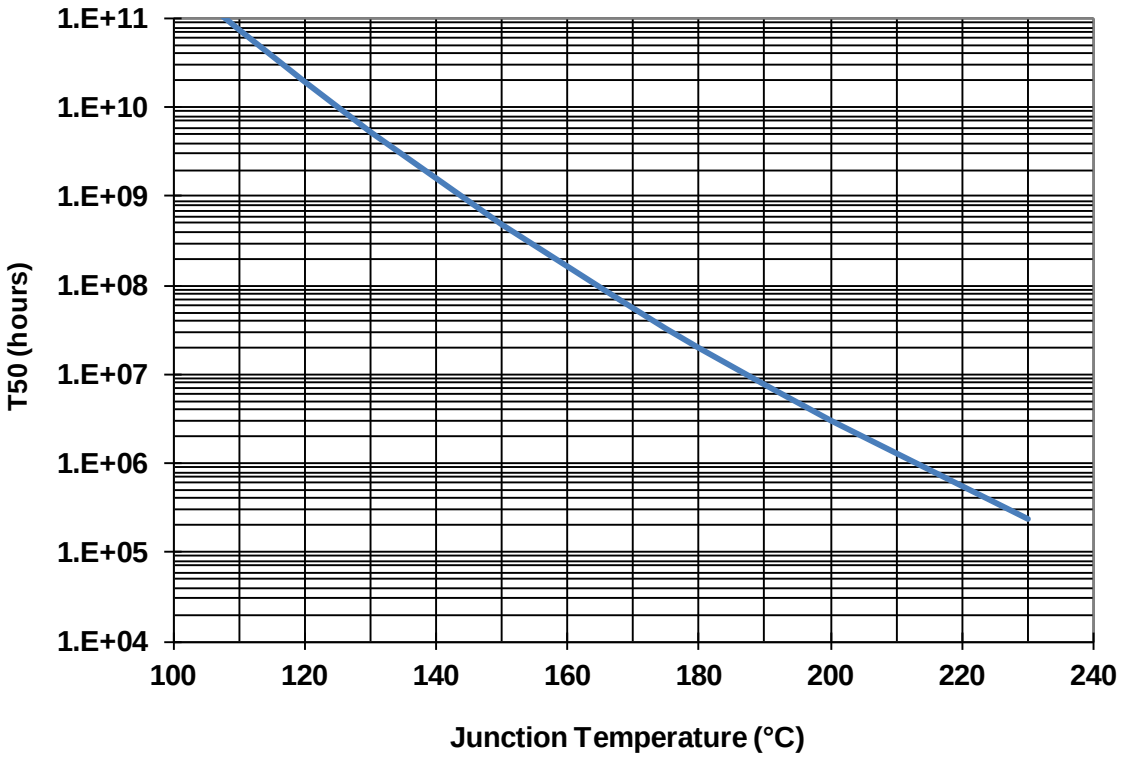
## Device thermal performances

The device thermal performances below are based on UMS rules to evaluate the junction temperature.
The temperature $Tb_{chip}$ is defined as the chip back side temperature.
The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Absolute Maximum Ratings table.
So, the PCB system must be designed to comply with this requirement.

| Parameter | Biasing conditions | Tjunction (°C) | $R_{TH}$ ( °C/W) | T50 ( hours) |
|---|---|---|---|---|
| $R_{TH}$ (1) Thermal Resistance (Back of the chip) | Vd= 6V<br>Idq = 900mA<br>Pdiss= 5.4W | 165 | 14.9 | 9.E+07 |

(1) Assuming 85°C $Tb_{chip}$



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## Typical on-wafer Sij parameters (Pulsed mode)

Tamb.= +25°C, Vd = +6.0V, Id = 900mA, Pulse width = 25µs, Duty cycle = 10%

| Freq (GHz) | S11 (dB) | PhS11 (°) | S12 (dB) | PhS12 (°) | S21 (dB) | PhS21 (°) | S22 (dB) | PhS22 (°) |
|---|---|---|---|---|---|---|---|---|
| 1 | -0,1 | 177,3 | -75,4 | 77,7 | -76,4 | -64,2 | -0,1 | 176,9 |
| 3 | 0,0 | 171,4 | -83,2 | -48,5 | -62,7 | -1,6 | -0,2 | 172,2 |
| 4 | -0,1 | 169,0 | -84,8 | -37,6 | -66,6 | -112,6 | -0,2 | 169,5 |
| 5 | -0,1 | 166,0 | -86,3 | 60,3 | -65,2 | -166,2 | -0,2 | 166,8 |
| 6 | -0,1 | 162,9 | -84,2 | 40,8 | -70,6 | -13,8 | -0,2 | 164,0 |
| 7 | -0,1 | 159,9 | -76,0 | 159,5 | -66,1 | 45,1 | -0,2 | 160,8 |
| 8 | -0,1 | 156,7 | -70,3 | -125,3 | -64,9 | -86,4 | -0,2 | 157,8 |
| 9 | -0,1 | 153,1 | -80,8 | -103,3 | -59,1 | -34,7 | -0,2 | 154,3 |
| 10 | -0,1 | 149,3 | -73,6 | -134,5 | -56,7 | 38,0 | -0,2 | 150,3 |
| 11 | -0,1 | 145,5 | -71,7 | -127,0 | -65,1 | -149,1 | -0,2 | 146,4 |
| 12 | -0,1 | 141,3 | -71,7 | -168,2 | -64,7 | -165,9 | -0,3 | 141,6 |
| 13 | -0,1 | 136,5 | -67,4 | 174,7 | -63,9 | 126,7 | -0,3 | 135,3 |
| 14 | -0,1 | 131,2 | -62,7 | 102,9 | -68,6 | -115,4 | -0,7 | 125,5 |
| 15 | -0,1 | 125,0 | -73,4 | 119,3 | -57,5 | 163,0 | -4,9 | 112,5 |
| 16 | -0,1 | 117,9 | -60,2 | 105,5 | -52,9 | 80,9 | -2,6 | 144,2 |
| 17 | -0,1 | 109,2 | -59,7 | 22,4 | -50,5 | 7,4 | -1,2 | 133,5 |
| 18 | -0,2 | 98,6 | -65,3 | 18,2 | -49,9 | -23,8 | -0,9 | 124,4 |
| 19 | -0,3 | 84,6 | -76,8 | -135,5 | -51,7 | -47,0 | -0,7 | 114,5 |
| 20 | -0,5 | 65,3 | -75,0 | 3,2 | -46,2 | 5,2 | -0,7 | 102,9 |
| 21 | -1,1 | 42,7 | -74,7 | -114,4 | -26,8 | 15,1 | -0,9 | 89,3 |
| 22 | -2,5 | 4,0 | -77,9 | -169,2 | -9,8 | -52,5 | -1,5 | 71,2 |
| 23 | -5,3 | -52,7 | -73,4 | -3,0 | 3,3 | -146,8 | -2,9 | 48,5 |
| 24 | -8,6 | -137,5 | -69,2 | -151,3 | 12,7 | 110,7 | -5,7 | 22,3 |
| 25 | -10,2 | 140,5 | -54,6 | -153,1 | 19,3 | 5,0 | -11,2 | -4,6 |
| 26 | -13,2 | 78,8 | -57,6 | 161,4 | 24,1 | -101,8 | -21,8 | 17,2 |
| 27 | -15,6 | 35,7 | -52,0 | 115,5 | 26,0 | 145,9 | -14,4 | 31,6 |
| 28 | -15,0 | -25,8 | -53,1 | 83,3 | 25,3 | 50,7 | -15,3 | -24,1 |
| 29 | -14,1 | -76,5 | -55,8 | 42,8 | 25,1 | -34,8 | -18,8 | -69,8 |
| 30 | -14,1 | -90,9 | -49,9 | -1,5 | 24,4 | -119,2 | -18,9 | -47,3 |
| 31 | -11,8 | -104,7 | -49,7 | -28,6 | 24,0 | 162,8 | -12,8 | -75,1 |
| 32 | -10,8 | -129,4 | -48,2 | -28,9 | 24,4 | 82,4 | -11,2 | -104,5 |
| 33 | -13,9 | -142,8 | -47,9 | -74,4 | 24,5 | -2,5 | -11,8 | -121,6 |
| 34 | -18,2 | -105,3 | -52,8 | -95,6 | 25,0 | -94,5 | -14,4 | -130,5 |
| 35 | -11,2 | -86,9 | -53,0 | -159,9 | 25,2 | 158,1 | -22,5 | -87,0 |
| 36 | -6,9 | -90,5 | -54,2 | -178,0 | 21,9 | 31,1 | -8,0 | -67,7 |
| 37 | -3,6 | -108,7 | -65,5 | 26,1 | 13,3 | -97,6 | -4,1 | -96,2 |
| 38 | -2,7 | -126,8 | -56,5 | -99,6 | 0,1 | 163,7 | -3,1 | -113,7 |
| 39 | -2,3 | -136,9 | -49,1 | -173,1 | -12,5 | 93,5 | -2,3 | -129,1 |
| 40 | -2,0 | -143,8 | -53,4 | 92,0 | -24,1 | 27,6 | -2,0 | -140,5 |



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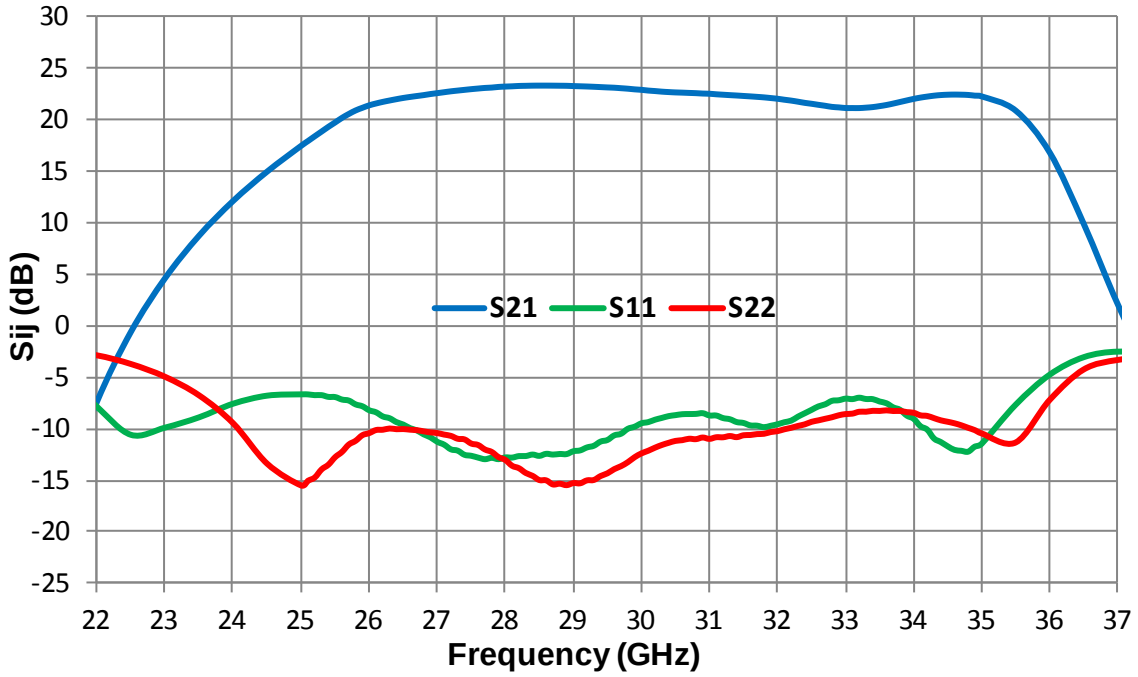
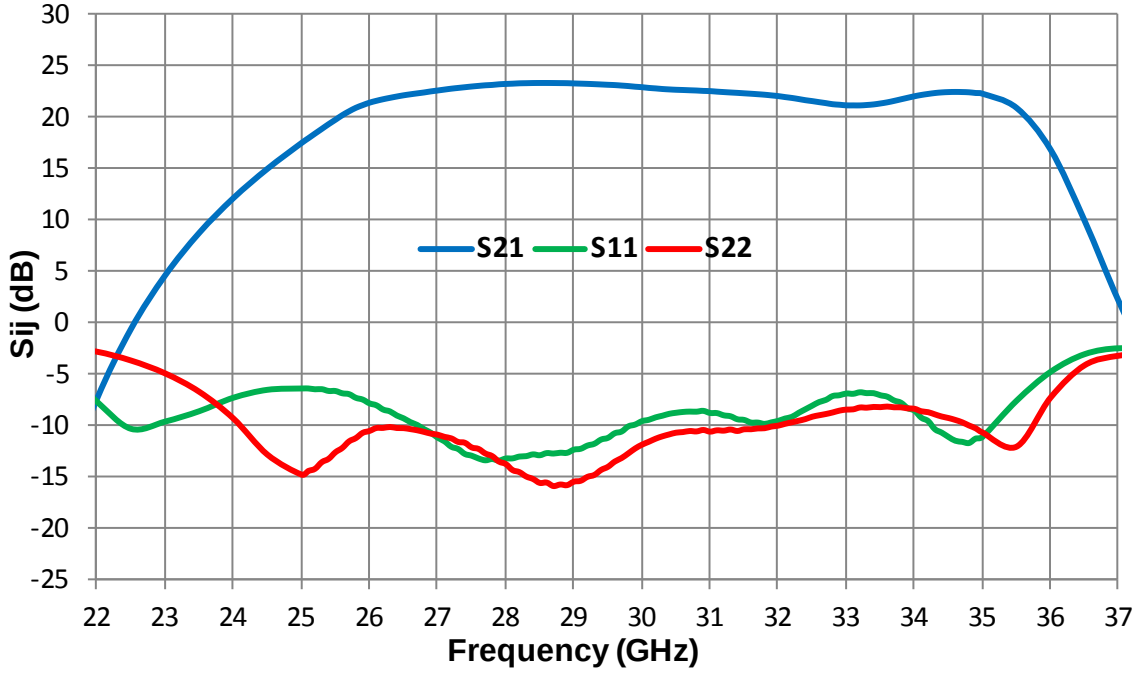
## Typical Board Measurements (CW)

Tamb.= +25°C, Vd = +6V, Idq = 900mA & Vd = +5V, Idq = 730mA
Measurement performed in the access plans of the die.

**Gain & Return Losses versus Frequency**
Vd = +6V, Idq = 900mA




**Gain & Return Losses versus Frequency**
Vd = +5V, Idq = 730mA



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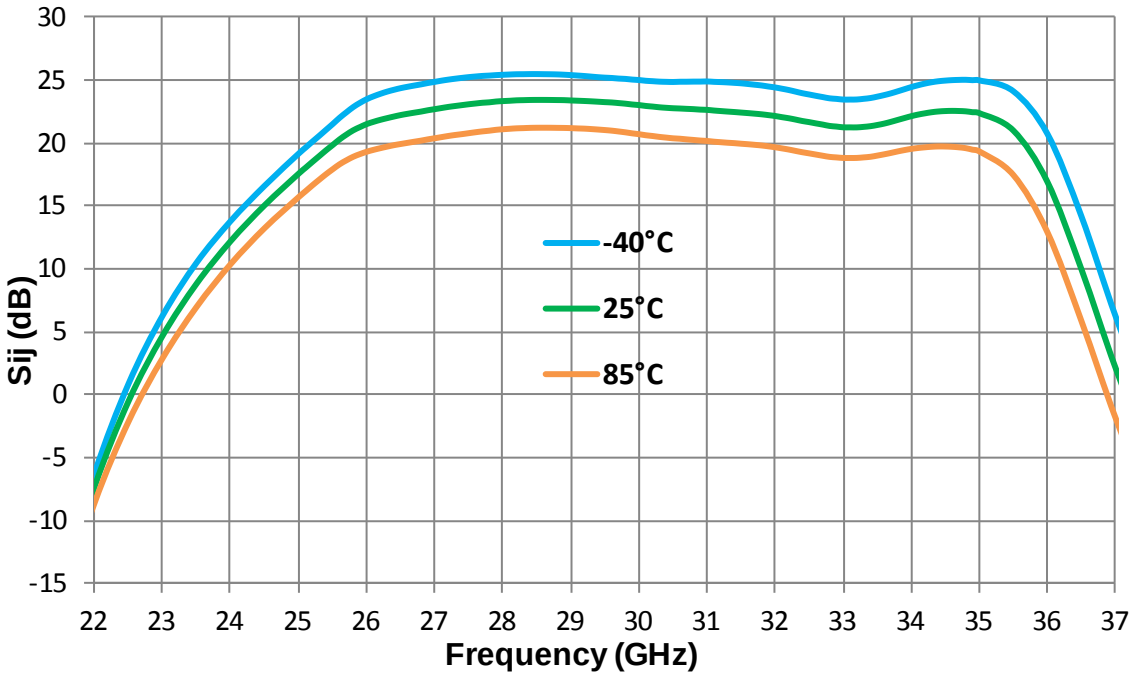
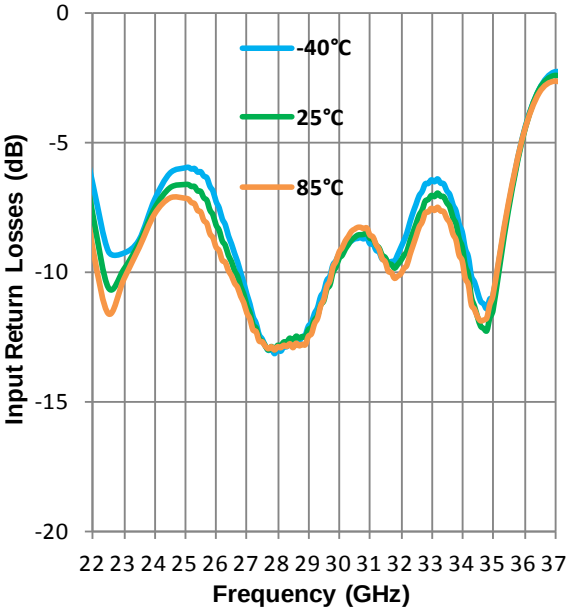
## Typical Measurements on a probe compatible Board (CW)

Tamb.= +25°C, Vd = +6.0V, Idq = 900mA
Measurement performed in the access plans of the die.

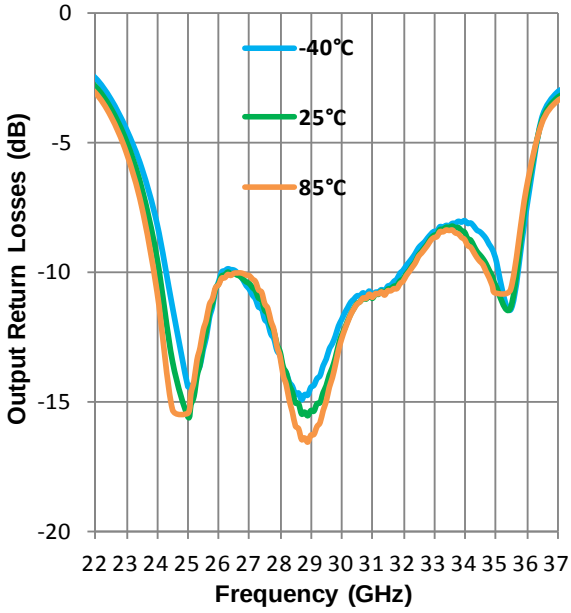
**Gain versus Frequency in Temperature**




**Input Return Losses versus Frequency in Temperature**




**Output Return Losses versus Frequency in Temperature**



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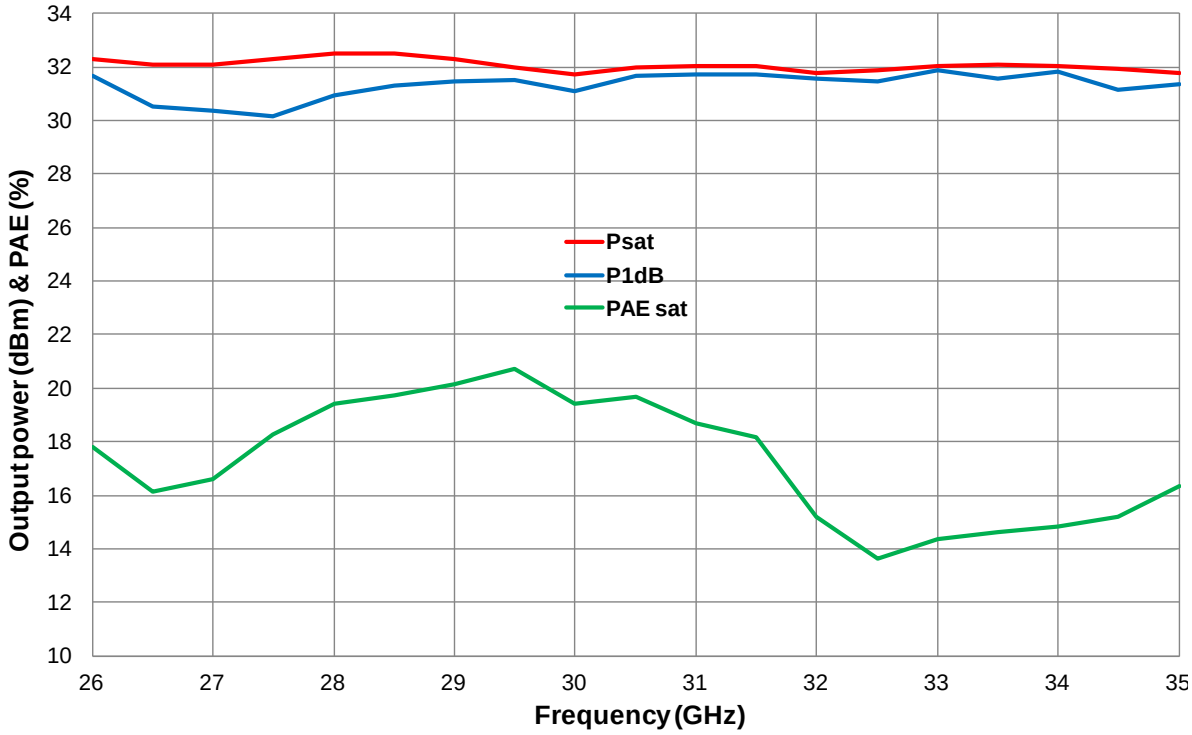
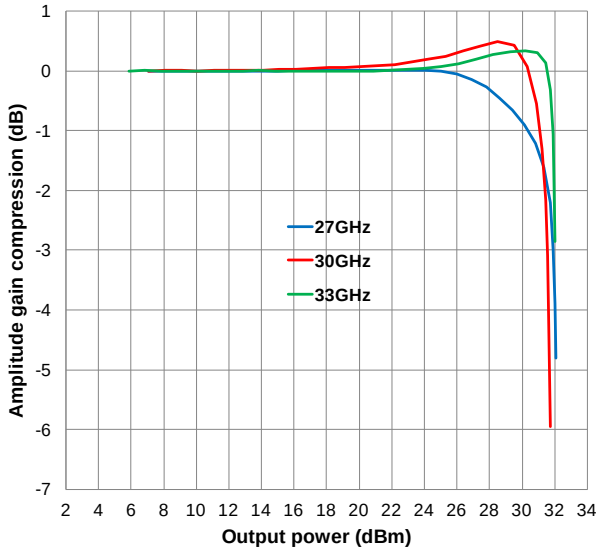
## Typical Board Measurements (CW)

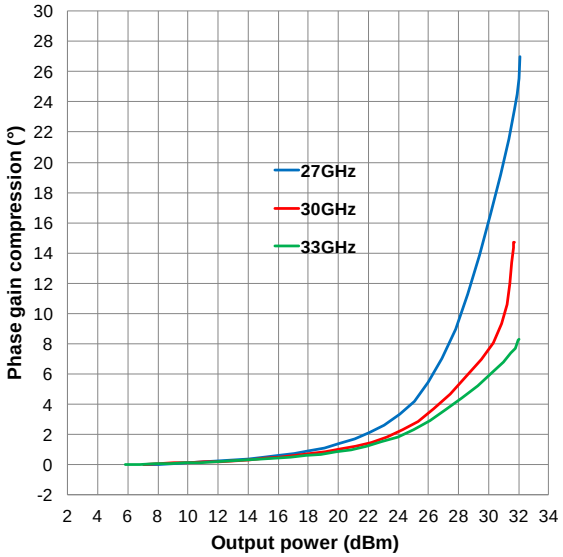
Tamb.= +25°C, Vd = +6.0V, Idq = 900mA
Measurement performed in the access plans of the die.

**Output Power & PAE versus Frequency**




**Gain Amplitude & Gain Phase variation versus Output Power**



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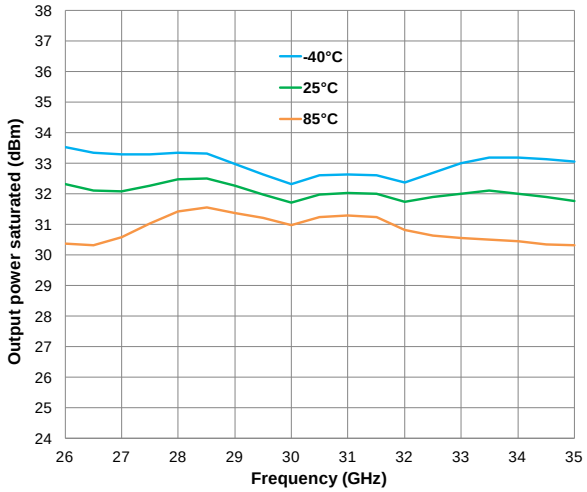
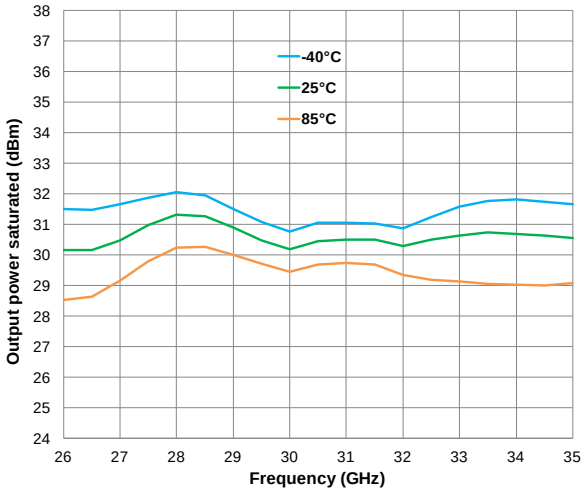
## Typical Board Measurements (CW)

Tamb.= +25°C, Vd = +6.0V, Idq = 900mA & Vd = +5V, Idq = 730mA

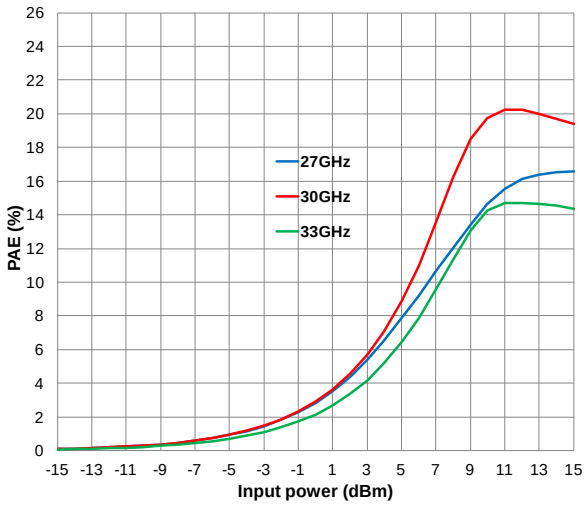
**Saturated Power versus Frequency in Temperature**
Vd = +6V, Idq = 900mA



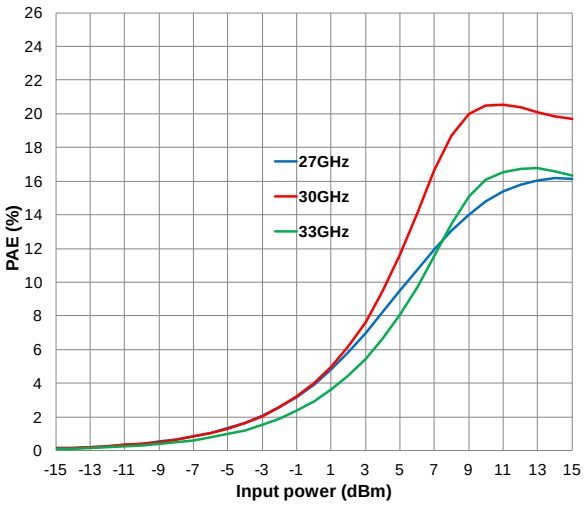

**Saturated Power versus Frequency in Temperature**
Vd = +5V, Idq = 730mA




**PAE versus Input Power**
Vd = +6V, Idq = 900mA




**PAE versus Input Power**
Vd = +5V, Idq = 730mA



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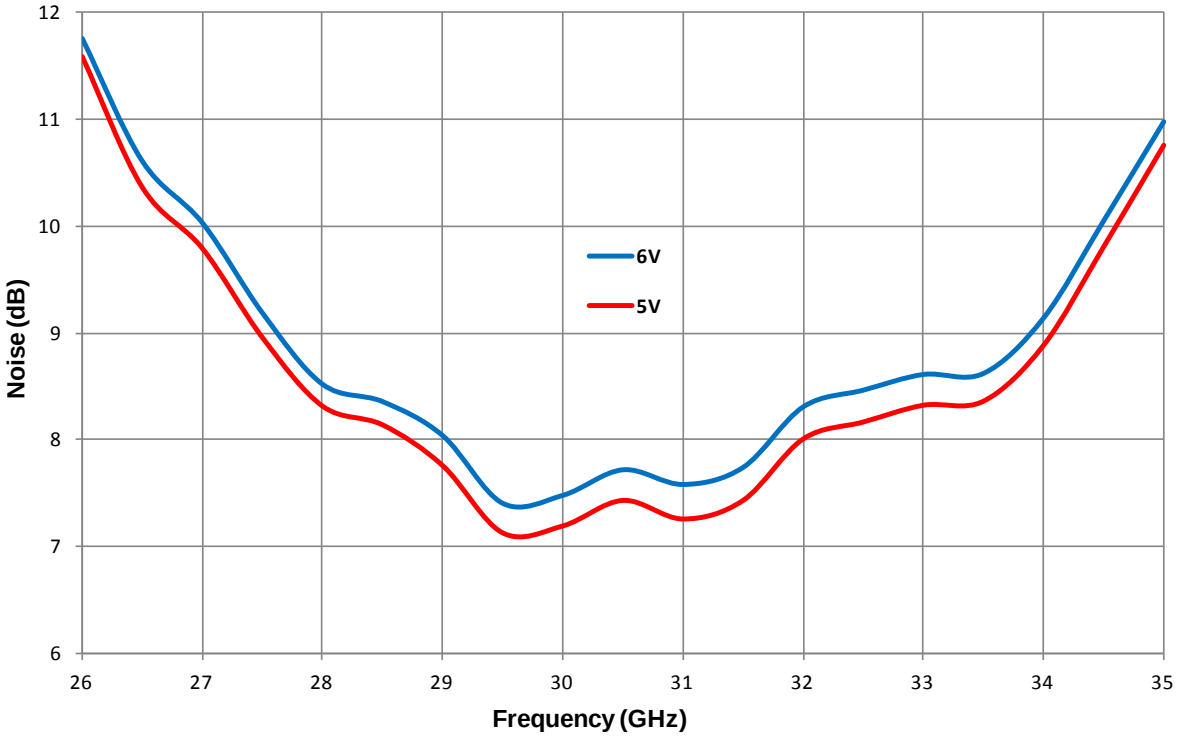
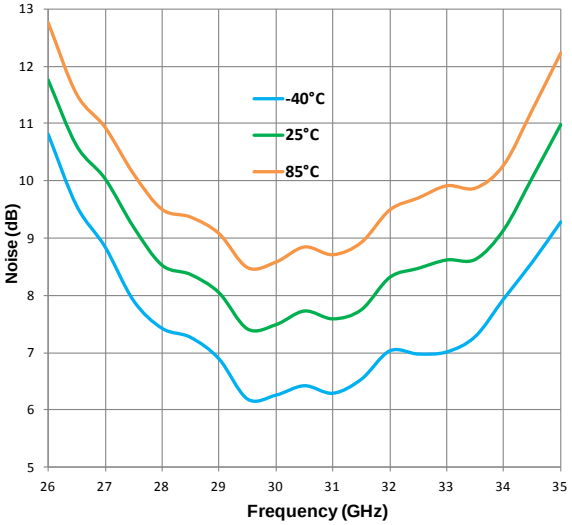
## Typical Board Measurements (CW)

Tamb.= +25°C, Vd = +6.0V, Idq = 900mA & Vd = +5V, Idq = 730mA

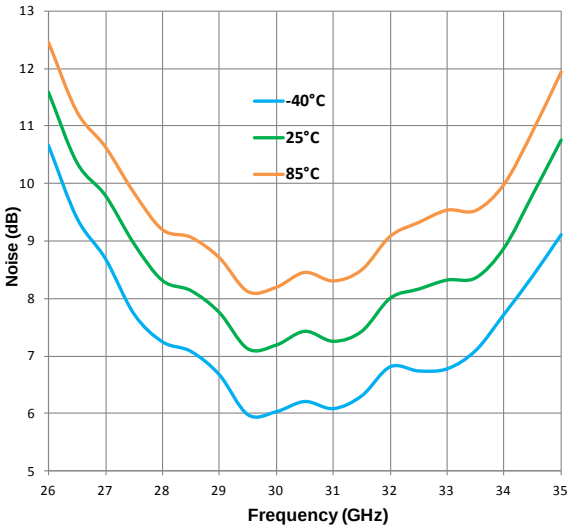
**Noise Figure versus Frequency**
Vd = +6V, Idq = 900mA
Vd = +5V, Idq = 730mA




**Noise Figure versus Frequency in Temperature**
Vd = +6V, Idq = 900mA




**Noise Figure versus Frequency in Temperature**
Vd = +5V, Idq = 730mA



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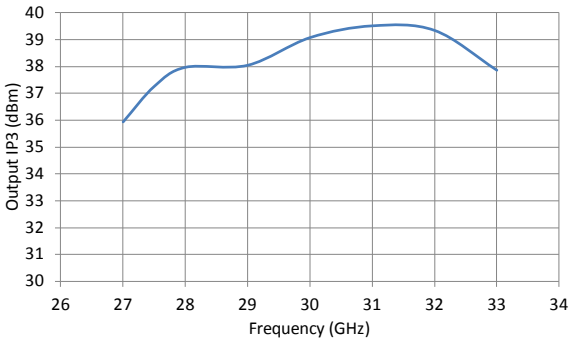
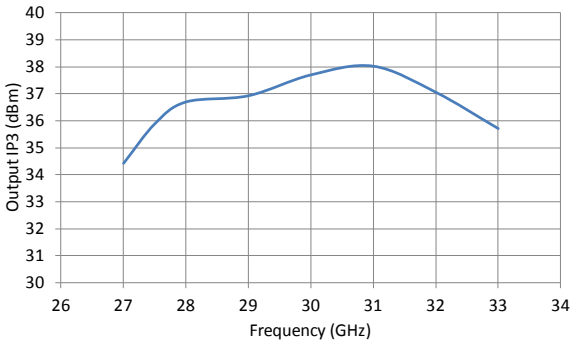
## Typical Board Measurements (CW)

Tamb.= +25°C, Vd = +6.0V, Idq = 900mA & Vd = +5V, Idq = 730mA

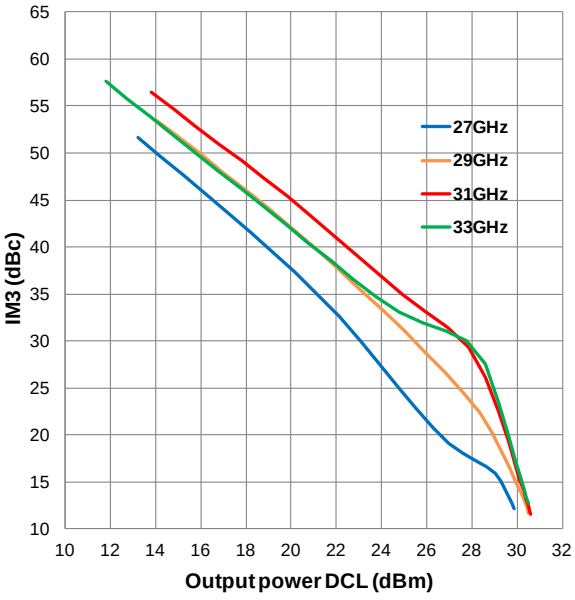
**Output IP3 versus Frequency**
Vd = +6V, Idq = 900mA



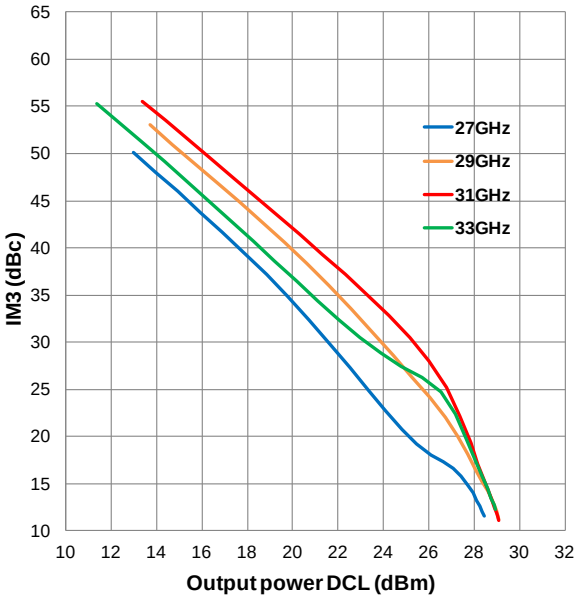

**Output IP3 versus Output Power**
Vd = +5V, Idq = 730mA




**Output IM3 versus Output Power**
Vd = +6V, Idq = 900mA




**Output IM3 versus Output Power**
Vd = +5V, Idq = 730mA



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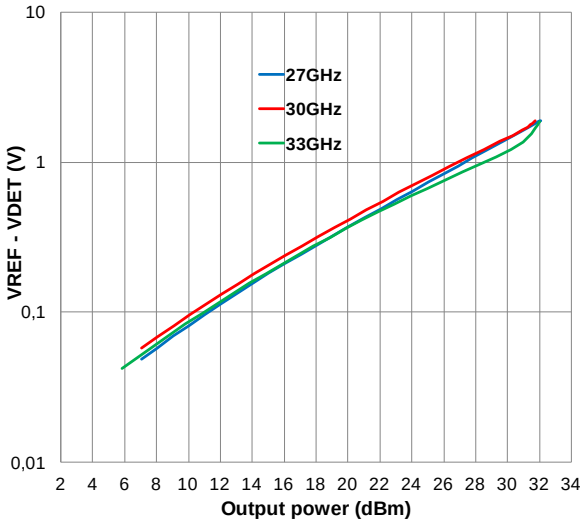
## Typical Board Measurements (CW)

Tamb.= +25°C, Vd = +6.0V, Idq = 900mA & Vd = +5V, Idq = 730mA

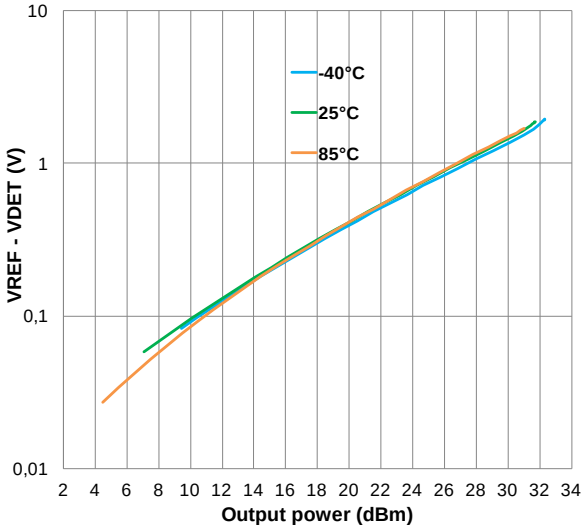
### Power Detector versus Output Power

Vd = +6V, Idq = 900mA



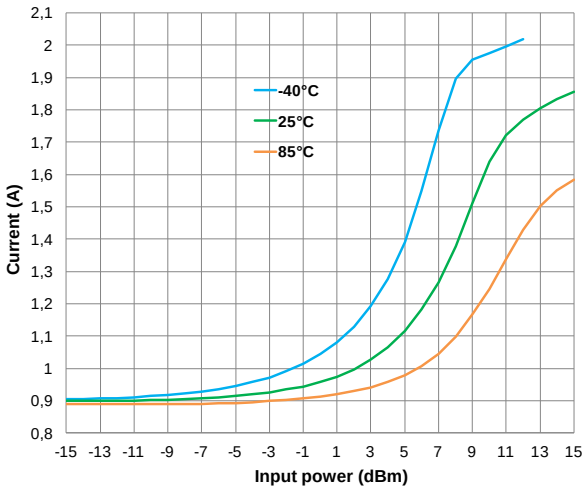

### Power Detector versus Output Power & Temperature at 30GHz

Vd = +6V, Idq = 900mA



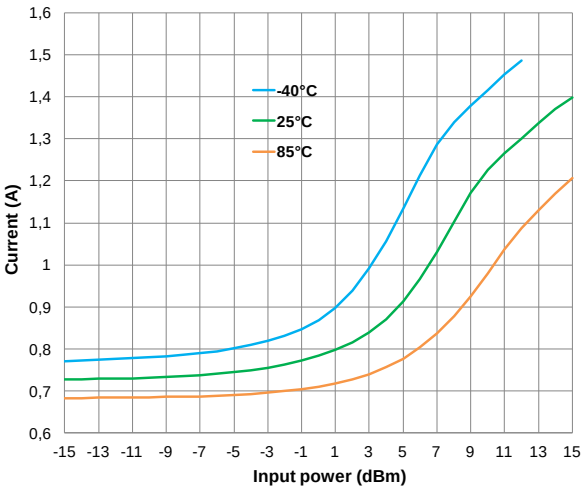

### Total Drain Current versus Output Power at 32.5GHz

Vd = +6V, Idq = 900mA




### Total Drain Current versus Output Power at 32.5GHz

Vd = +5V, Idq = 730mA



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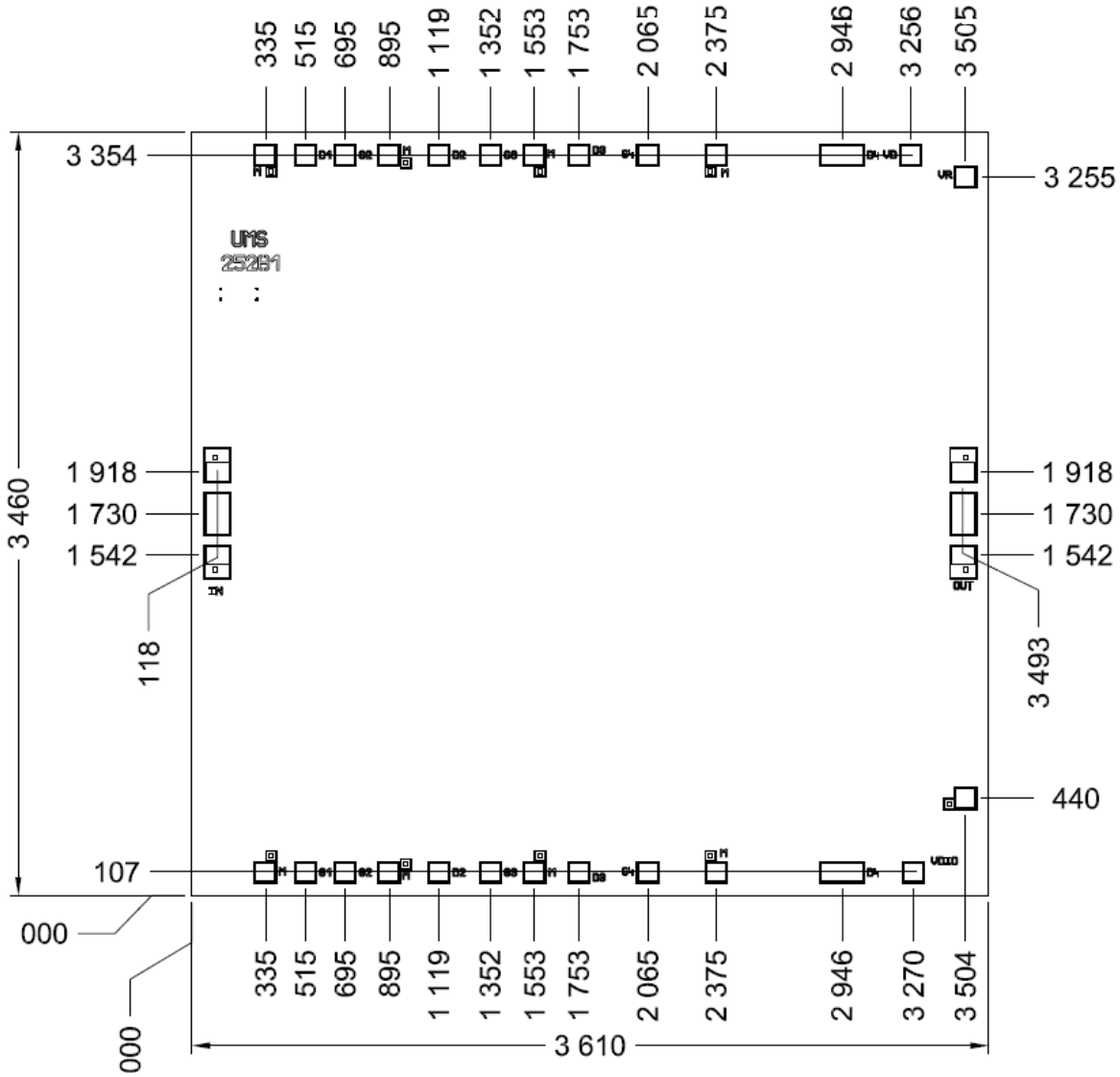
## Mechanical data




Chip thickness: 70µm.
All dimensions are in micrometers
DC pad size: 83um x 83 um (BCB opening)
RF pad size: 105um x 186 um (BCB opening)



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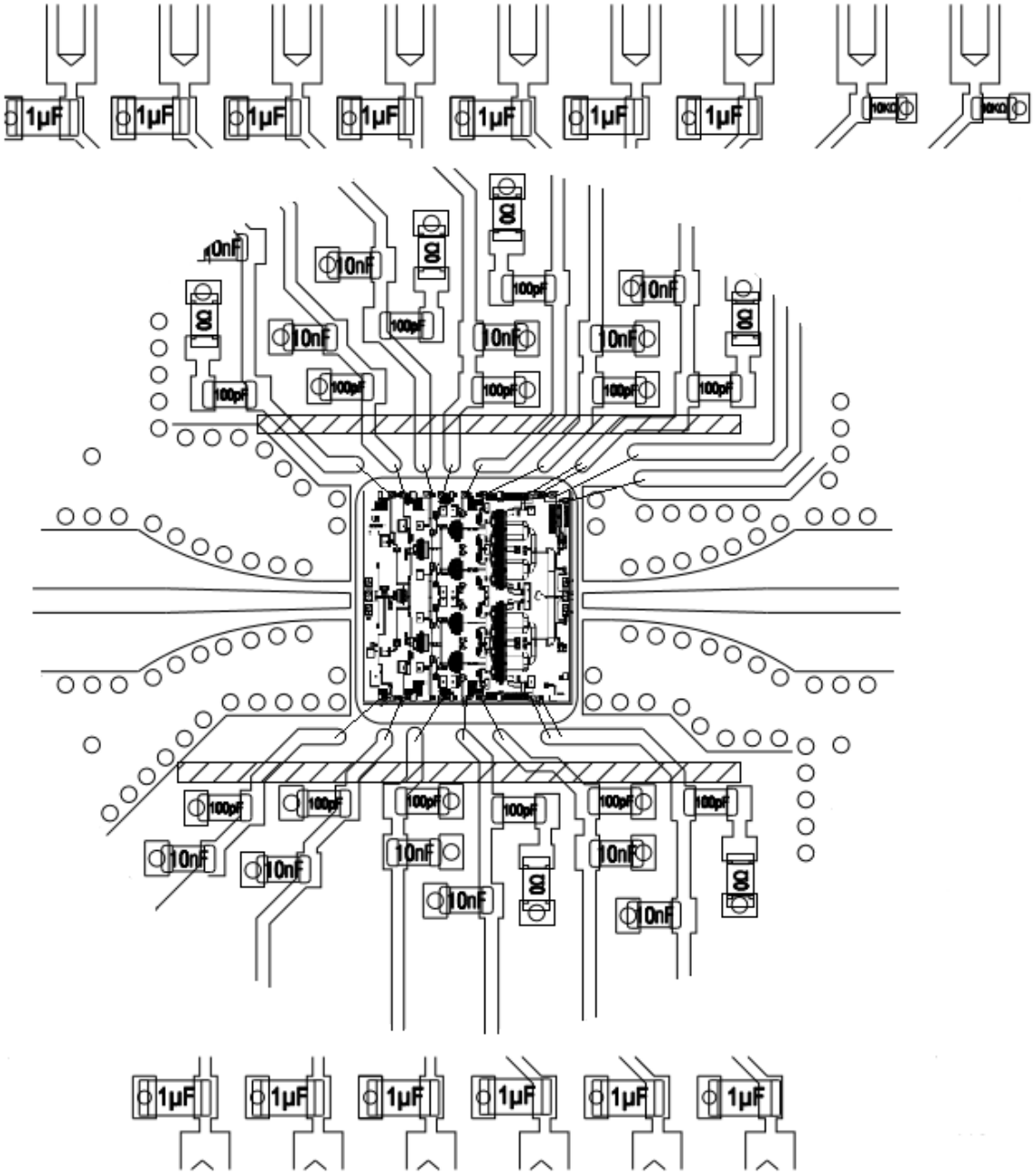
## Recommended assembly plan




Decoupling capacitors: 100pF, 10nF & 1µF (on gate & drain access)

Note: Supply feed should be bypassed. 25µm diameter gold wire is to be preferred.



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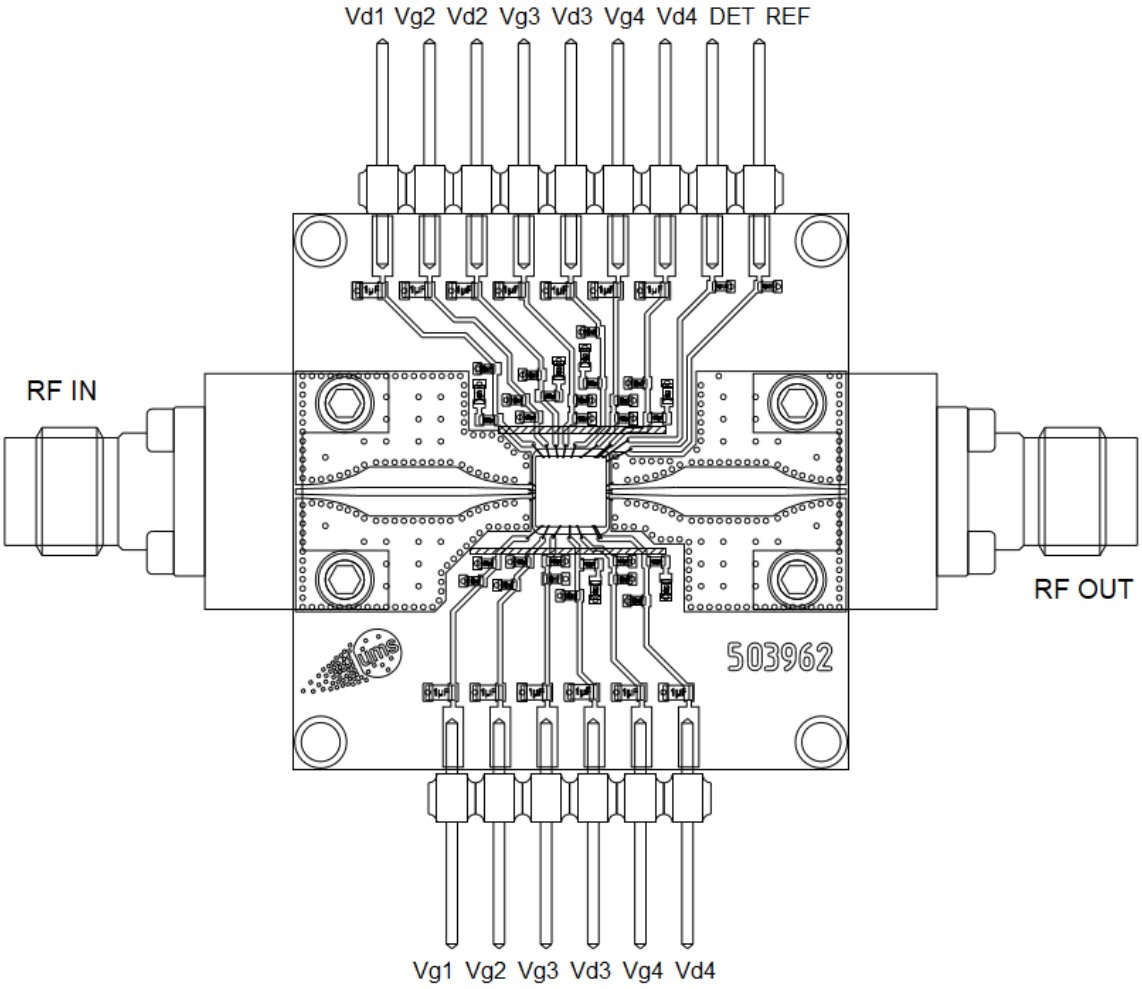
## Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically RF35P / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the chip.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 100pF ±5%, 10nF ±10% and 1µF ±10% are recommended for the gate and drain accesses.
- A 10KΩ resistor is recommended on V_REF & V_DET accesses for the detector
- Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.



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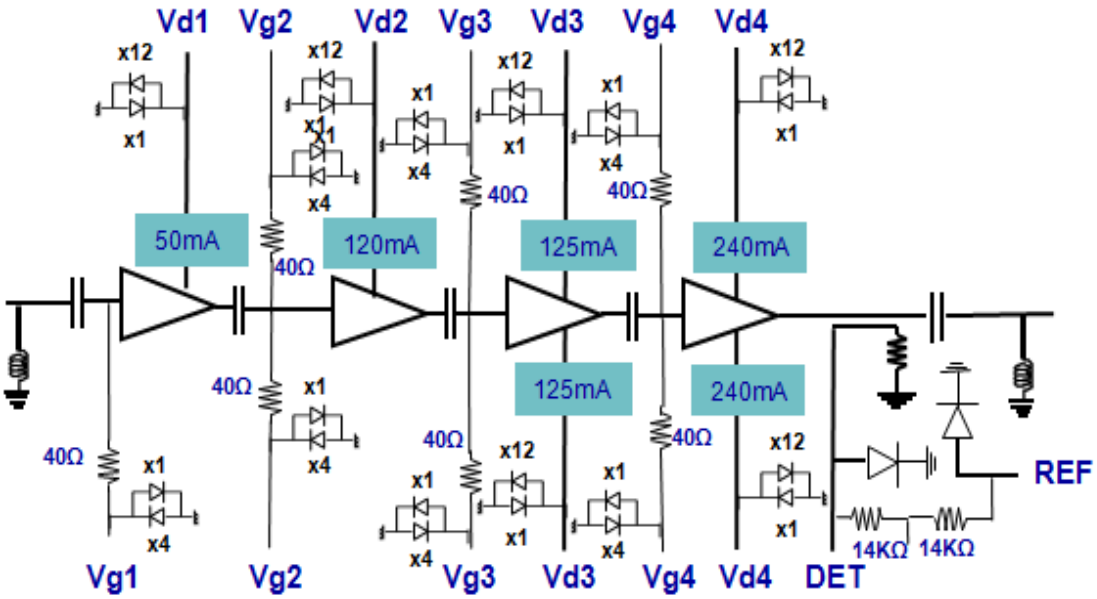
## DC Schematic

**HPA : 6V, 900mA**




## Biasing procedure

Device Power Up instructions:

1. Ground the device
2. Bias HPA gate voltage at Vgs close to Vpinch-off (example: Vg ≈ -2V)
3. Apply Vds quiescent bias voltage (Example: Vd = 6V)
4. Increase slowly Vgs up to quiescent bias drain current Idq (pulsed applied on the gate)
5. Apply RF input power

Device Power Up instructions:

1. Remove RF input power
2. Decrease HPA gate voltage up to Vgs -2V
3. Decrease drain voltage up to 0V



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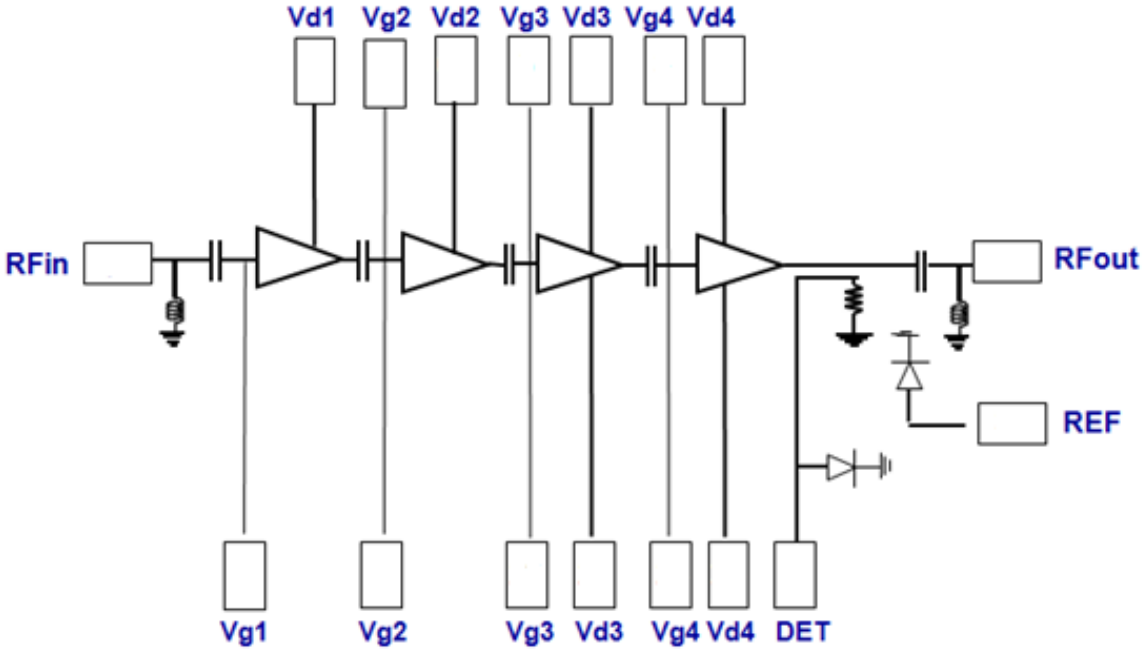
## Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage potentially present on the RF accesses.




Limited DC decoupling is implemented on chip. Additional external DC decoupling (100pF, 10nF, 1µF) on the PC Board, as close as possible to the bare die, is required.

A 10KΩ resistor is recommended in parallel to V_DET, and V_REF accesses.

The circuit includes ESD protections on all RF and DC accesses.



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## Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS products.

## Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

## Ordering Information

| | |
|---|---|
| Chip form: | CHA6653-98F/00 |

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