

## 35.5-40.5GHz 9W High Power Amplifier

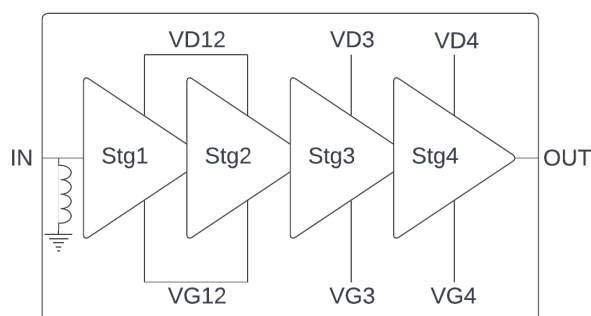
### GaN Monolithic Microwave IC

#### Description

The CHA7452-99F is a four stage High Power Amplifier operating between 35.5 and 40.5 GHz and providing typically 9W of saturated output power and 24 % of power added efficiency. The typical power supply is 20V/290mA (quiescent current). Thanks to a low drain voltage biasing, the CHA7452-99F provides a junction temperature below 160°C, even in saturation.

The circuit is manufactured on a space evaluated 0.15µm gate length GaN-on-SiC HEMT process and is available in bare die form.

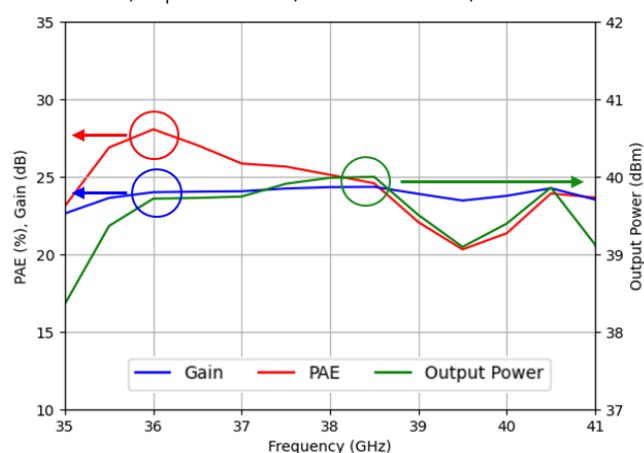
It is firstly dedicated to space applications and well suited for a wide range of microwave applications and systems.



#### Main Features

- Frequency range: 35.5 – 40.5 GHz
- High output power: 9 W
- High PAE: 24 %
- Linear Gain: 29 dB
- DC bias: Vd=20V @Id=290 mA
- Chip size: 3.6x2.9 mm
- Available in bare die form

V<sub>D</sub> = 20 V, I<sub>dq</sub> = 290 mA, Pin = 15 dBm, T<sub>case</sub> = 25 °C



#### Main Electrical Characteristics

T<sub>case</sub> = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	35.5		40.5	GHz
Gain	Linear Gain		29		dB
Pout	Saturated Output Power		39.5		dBm
PAE	Power Added Efficiency		24		%

## Specifications

Tcase = +25°C, Vd = +20V, CW excitation

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	35.5		40.5	GHz
Gain	Linear Gain		29		dB
Pout	Saturated Output Power		39.5		dBm
PAE	Power Added Efficiency		24		%
Id	Drain current at saturation		2.5		A
S11	Input Return Loss		-12		dB
S22	Output return loss		-8		dB
Idq	Quiescent current		290		mA
Vd	Drain Voltage		20		V

These values are representative of on-board measurements as defined on the drawing in paragraph "Evaluation mother board".

## Absolute Maximum Ratings <sup>(1)</sup>

Tcase = +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	27	V
Id	Drain bias current	800	mA
Vg	Gate bias voltage	-7 to -1	V
Tj	Maximum Junction temperature <sup>(2)(3)</sup>	200	°C

<sup>(1)</sup> Operation of this device above any one of these parameters may cause permanent damage

<sup>(2)</sup> See Device thermal performances section.

<sup>(3)</sup> Same as Recommended Operating Range

## Recommended Operating Range <sup>(4), (5)</sup>

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	18 to 25	V
Id	Drain bias current	100 to 450	mA
Vg	Gate bias voltage	-3.5 to -2.5	V
Tj	Maximum Junction temperature	200	°C

<sup>(4)</sup> Electrical performances are defined for specified test conditions

<sup>(5)</sup> Electrical performances are not guaranteed over all recommended operating conditions

## Temperature Range

Tcase	Operating temperature range at MMIC backside level	-40 to +95	°C
Tstg	Storage temperature range	-55 to +150	°C

**Typical Bias Conditions**

Tcase=+25°C

Symbol	Pad N°	Parameter	Values	Unit
Vg	3, 5, 7, 25, 27, 29	Gate voltage tuned for Idq~290mA	-3.1	V
Vd	9, 11, 13, 19, 21, 23	Drain Voltage	20	V

**“Power ON” sequence**

1. Bias HPA gate voltage at Vg close to Vpinch-off (Typically: Vg ≈ -5)
2. Apply Vds bias voltage (Typically: Vd = 20V)
3. Increase Vgs up to quiescent bias drain current Idq (pulsed applied on the gate)
4. Apply RF signal

**“Power OFF” sequence**

1. Turn off RF signal
2. Bias HPA gate voltage at Vg close to Vpinch-off (Typically: Vg ≈ -5)
3. Turn Vds bias voltage to 0V
4. Turn Vgs bias voltage to 0V

## Device thermal performances

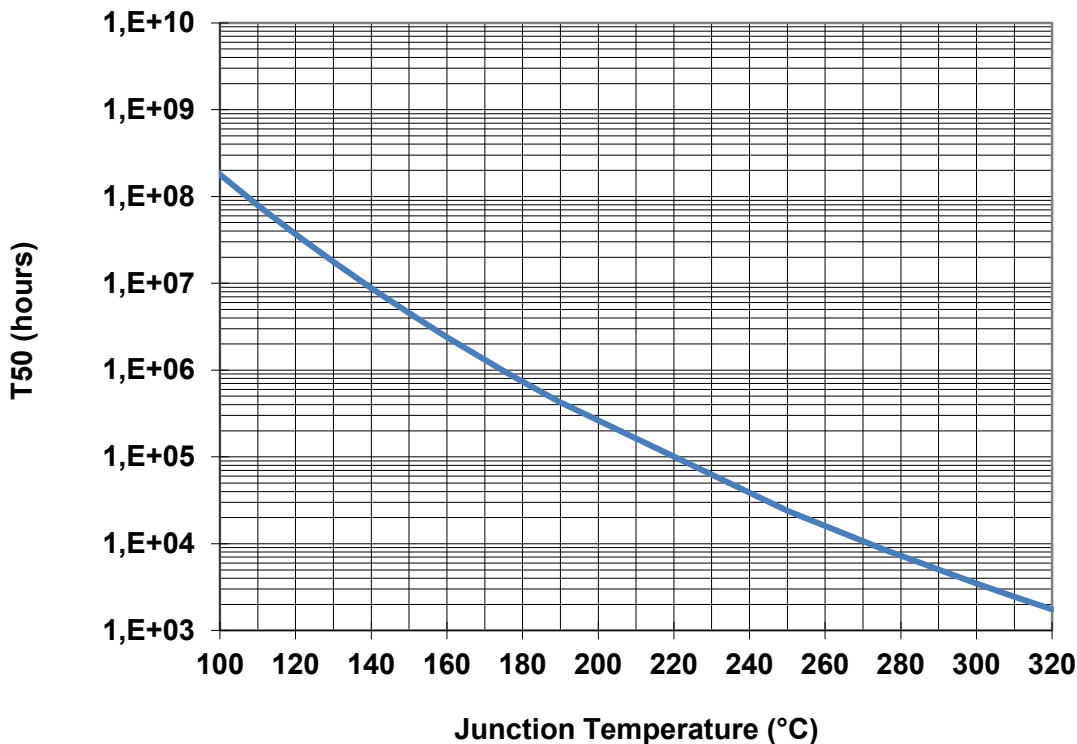
The device thermal performances below are based on UMS rules to evaluate the junction temperature.

This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHA7452-99F is manufactured (GaN HEMT 0.15µm).

The temperature  $T_{case}$  is defined as the chip backside temperature. The thermal resistance ( $R_{th\_eq}$ ), given in the following table, is for the full circuit in CW mode.

Thermal Resistance <sup>(1)</sup>	$R_{th\_eq}$	$T_{case} = 85^{\circ}C,$ $Vd = 20V, Idq = 290\text{ mA},$ $Pin = 18\text{ dBm}, Freq = 40GHz,$ $Pdiss = 28\text{ W}$	2.36	$^{\circ}C/W$
Junction Temperature	$T_j$		151	$^{\circ}C$
Median Life	T50		4.5E6	Hrs
Thermal Resistance <sup>(1)</sup>	$R_{th\_eq}$	$T_{case} = 85^{\circ}C,$ $Vd = 25V, Idq = 290\text{ mA},$ $Pin = 18\text{ dBm}, Freq = 40GHz,$ $Pdiss = 28\text{ W}$	2.45	$^{\circ}C/W$
Junction Temperature	$T_j$		183	$^{\circ}C$
Median Life	T50		7E5	Hrs

<sup>1</sup> Thermal resistance measured at the backside of the chip



**Typical On Wafer Measurement Sij parameters**T<sub>case</sub> = +25°C, V<sub>D</sub> = 20V, I<sub>dq</sub> = 290mA

Frequency (GHz)	dBS11 (dB)	PhS11 (°)	dBS12 (dB)	PhS12 (°)	dBS21 (dB)	PhS21 (°)	dBS22 (dB)	PhS22 (°)
1	-8.33	-161.66	-77.88	-84.28	-65.38	-56.32	-0.29	-87.76
2	-5.61	-152.85	-70.49	153.04	-72.11	147.26	-0.22	-127.51
3	-2.65	-158.74	-68.91	47.75	-68.4	109.4	-0.23	-147.41
4	-1.01	-176.86	-70.41	86.83	-58.47	123.13	-0.17	-160.34
5	-1.58	165.11	-101.27	144.16	-57.85	42.11	-0.23	-169.51
6	-3.52	153.13	-70.58	-177.97	-54.27	18.33	-0.35	-176.41
7	-6.18	149.43	-93.3	19.07	-49.77	13.52	-0.41	177.55
8	-9.43	161.29	-71.64	56.58	-40.53	-14.08	-0.43	171.83
9	-9.22	-161.51	-75.17	-76.99	-28.37	-64.89	-0.45	165.34
10	-4.19	-165.24	-64.61	-160.89	-18.59	146.45	-0.78	154.36
11	-3.22	-167.54	-69.04	136.36	-21.42	7.12	-11.57	127.81
12	-1.86	-174.38	-65.52	-142.63	-42.9	-103.43	-0.58	177.69
13	-1.18	177.11	-62.77	-175.92	-72.55	-122.44	-0.2	165
14	-0.94	168.92	-57.82	125.87	-52.31	113.62	-0.19	158.13
15	-0.86	162.32	-65.94	102.44	-40.61	28.35	-0.18	151.92
16	-0.91	156.74	-56.17	79.31	-43.36	-43.84	-0.16	147
17	-1	151.13	-56.9	32.98	-39.56	-89.64	-0.16	141.77
18	-1.13	145.73	-56.85	-4.35	-45.73	174.82	-0.17	136.3
19	-1.29	141.21	-62.41	-63.49	-53.64	147.12	-0.16	130.5
20	-1.45	136.77	-72.38	161.12	-55.11	121.03	-0.22	124.32
21	-1.65	132.01	-69.79	-44.67	-60.92	122.96	-0.27	117.41
22	-1.75	127.29	-67.77	-113.53	-64.45	-127.37	-0.37	109.92
23	-1.93	123.11	-72.15	49.67	-65.42	-124.07	-0.26	101.33
24	-2.21	117.56	-70.21	39.52	-52.18	-113.2	-0.33	90.3
25	-2.38	112.38	-56.48	113.23	-48.5	-136.31	-0.34	75.98
26	-2.61	106.15	-52.2	25.91	-39.13	-164.61	-0.57	58.54
27	-2.94	99.52	-67.65	15.57	-34.31	-179.37	-0.9	36.01
28	-3.09	92.84	-58.23	-25.66	-26.36	149.02	-1.26	4.71
29	-3.45	84.96	-59.35	-126.2	-18.63	115.7	-1.71	-34.57
30	-3.62	77.47	-66.07	-95.25	-10.87	72.62	-2.28	-80.73
31	-4.53	65.48	-71.36	-42.17	-3.11	24.29	-2.59	-126
32	-4.93	52.46	-57.73	-64.35	5.83	-30.61	-2.77	-165.98
33	-6.86	37.01	-50.52	-4.76	15.66	-103.78	-3.98	159.01
34	-10.07	38.32	-52.03	-62.84	24.48	149.83	-7.21	117.63
35	-8.46	24.6	-56.47	-79.03	28.26	28.89	-24.9	137.74
36	-10.04	-4.42	-51	-158.21	28.22	-86.54	-8.72	-175.29

# CHA7452-99F

## 35.5-40.5GHz 9W HPA

37	-14.22	-26.24	-50.75	-177.7	25.31	174.72	-7.85	147.64
38	-13.89	-36.11	-60.8	109.37	23.31	95.27	-9.14	129.75
39	-13.52	-72.25	-53.46	-174.46	22.98	15.18	-9.47	111.97
40	-12.8	-118.55	-56.79	-97.61	24.31	-76.33	-9.82	69.01
42	-12.9	178.38	-52.72	66.55	18.67	1.27	-5.66	-79.89
43	-11.67	159.88	-55.36	88.03	5.5	-116.51	-3.99	-116.17
44	-10.59	137.71	-53.3	151.7	-8.81	156.36	-3.01	-136.34
45	-12.07	121.51	-50.12	93.21	-22.34	92.34	-2.4	-153.91
46	-11.91	96.33	-47.34	129.03	-35.2	51.93	-1.78	-166.26
47	-11.72	85.74	-44.88	72.19	-40.76	19.69	-1.39	-177.91
48	-10.84	71.25	-54	86.79	-40.99	-7.78	-1.23	172.55
49	-8.08	48.34	-44.91	36.7	-44.8	-73.43	-1.38	164.41
50	-6.65	12.78	-45.71	21.09	-40.12	-6.87	-1.32	156.93
51	-5.86	-15.55	-45.65	-18.19	-39.33	23.72	-1.08	150.91
52	-5.7	-34.88	-49.29	-20.06	-43.36	-42.42	-1.69	143.71
53	-5.55	-56.52	-58.5	142.32	-40.28	41.47	-1.19	137.66
41	-12.57	-144.89	-62.04	139.14	25.9	157.31	-8.82	-10.41
54	-5.18	-72.92	-54.49	75.62	-37.41	-53.87	-1.01	133.6
55	-4.66	-92.72	-52.29	5.21	-33.76	26.13	-1.51	127.06
56	-4.42	-100.57	-48.96	-10.93	-39.54	-109.37	-1.41	114.13
57	-4.9	-110.1	-43.42	-41.14	-45.15	-168.5	-1.08	107.79
58	-4.17	-123.55	-43.16	-37	-36.06	50.47	-0.8	99.41
59	-3.37	-130.56	-46.58	-72.88	-42.12	-50.2	-1.86	86.04
60	-3.16	-138.51	-58.6	-67.95	-37.3	36.32	-4.97	60.63

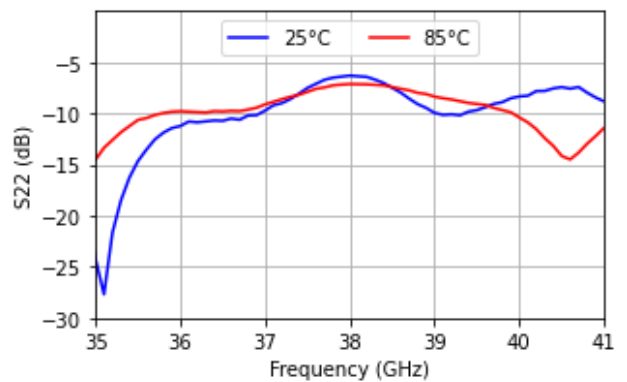
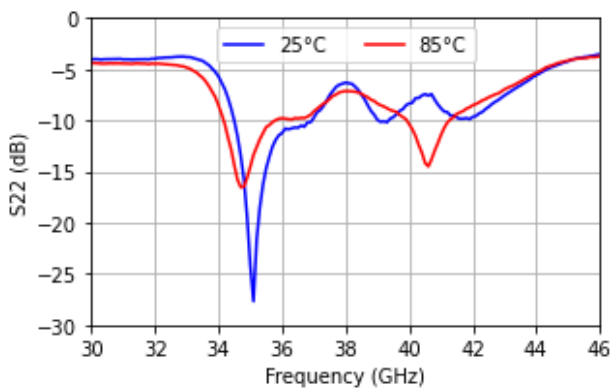
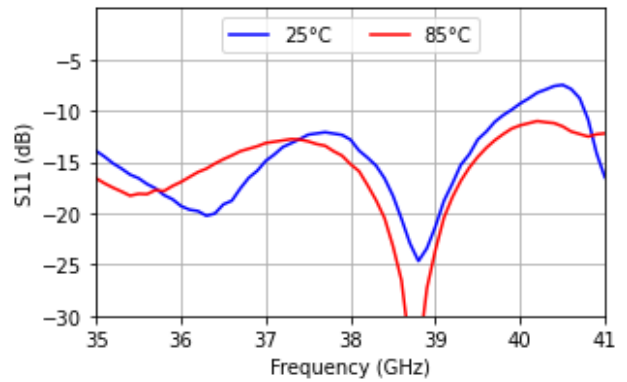
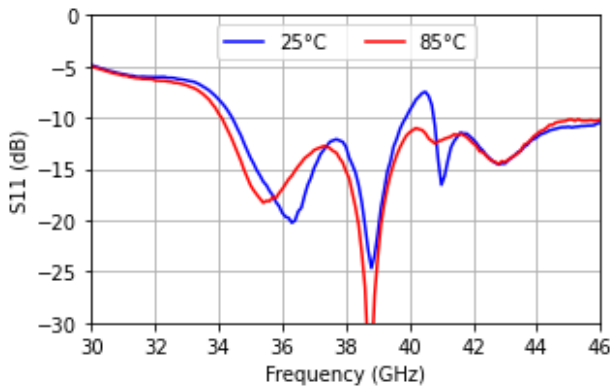
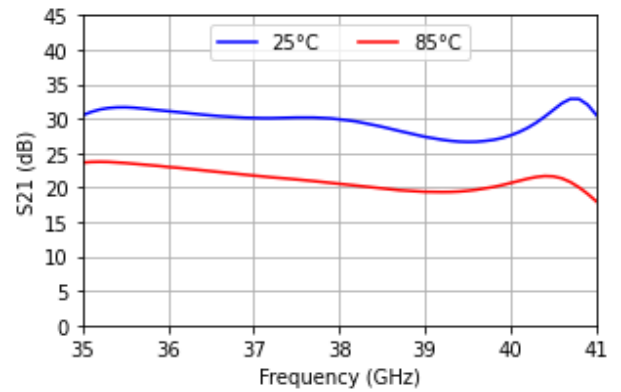
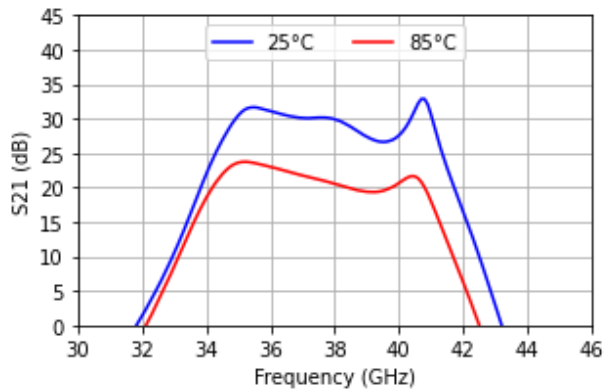


**Typical Board Measurements : Large Signal Performances**

Measurements reference plane is de-embedded at the wire-bondings plane on the RF feed line.

**Performance versus temperature**

**Test conditions :**  $V_D = 20V$ ,  $I_{dq} = 290mA$ ,  $T_{case} = 25^\circ C / 85^\circ C$

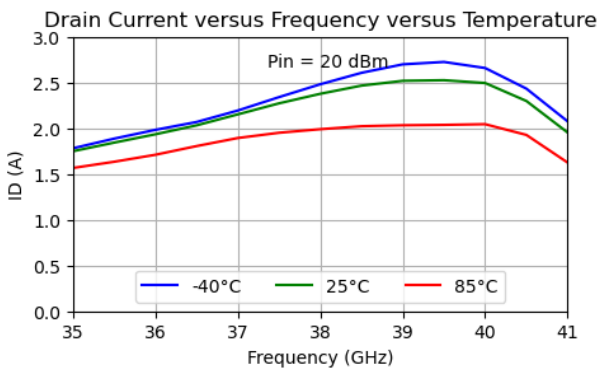
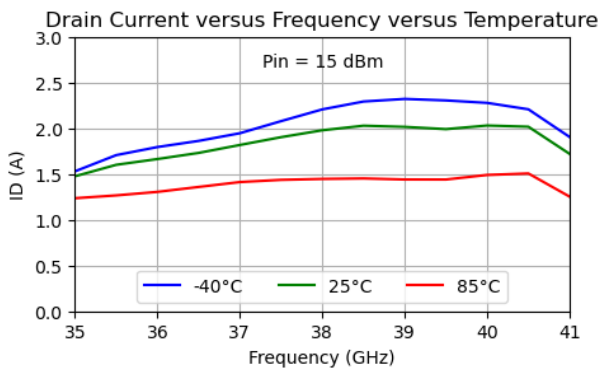
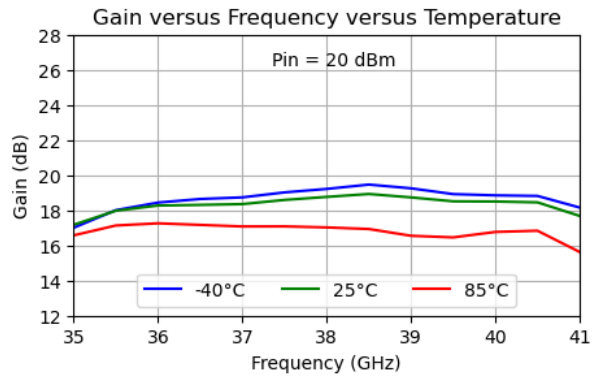
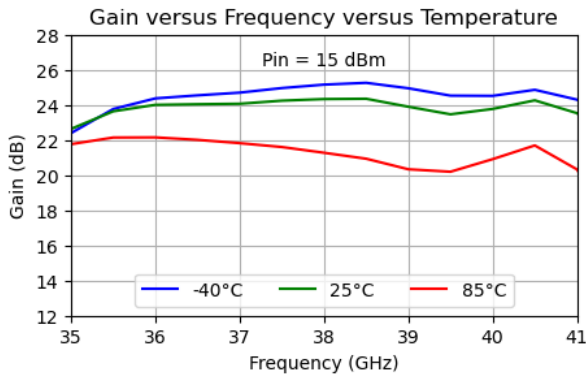
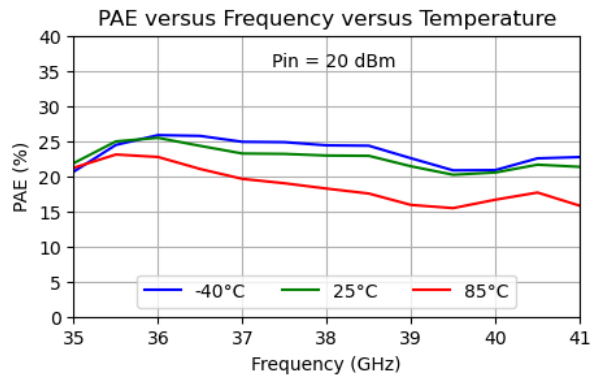
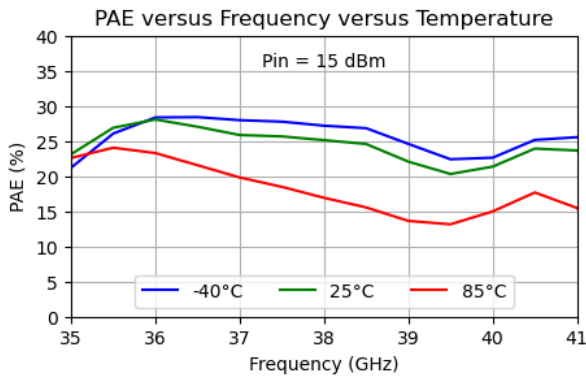
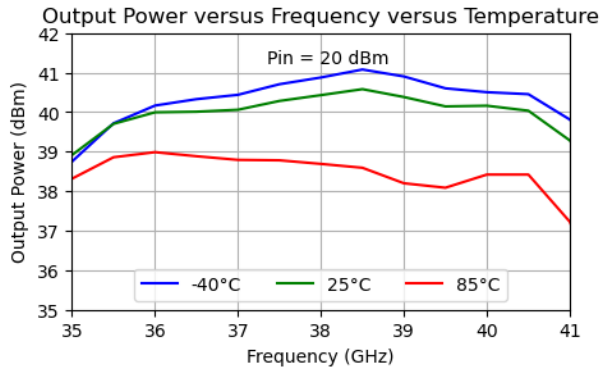
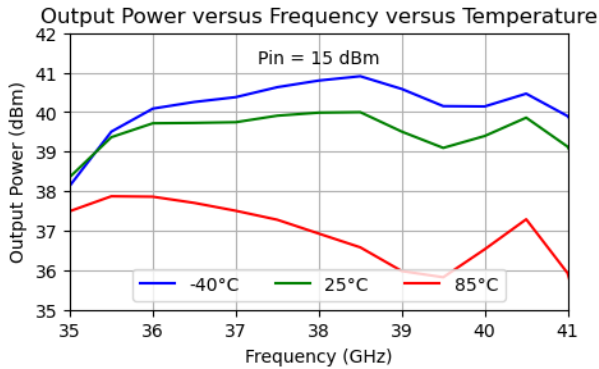


## Typical Board Measurements : Large Signal Performances

Measurements reference plane is de-embedded at the wire-bondings plane on the RF feed line.

### Performance versus frequency and temperature

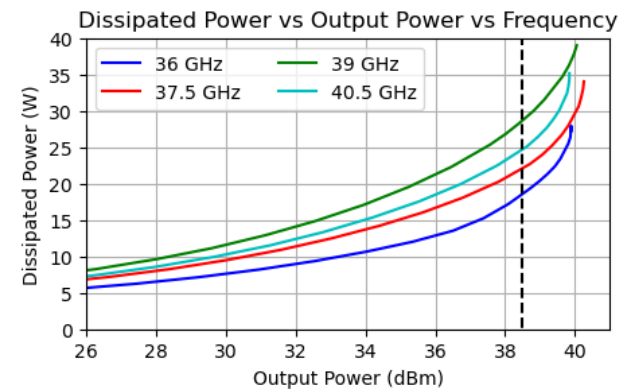
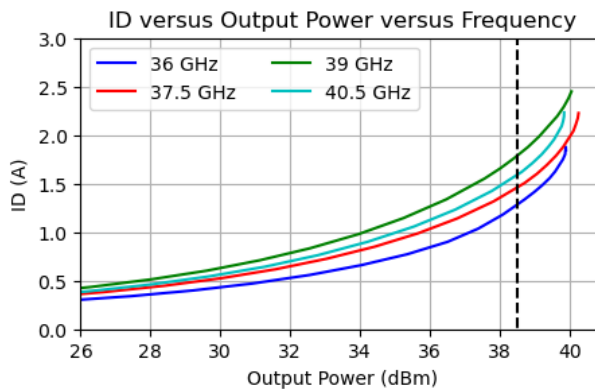
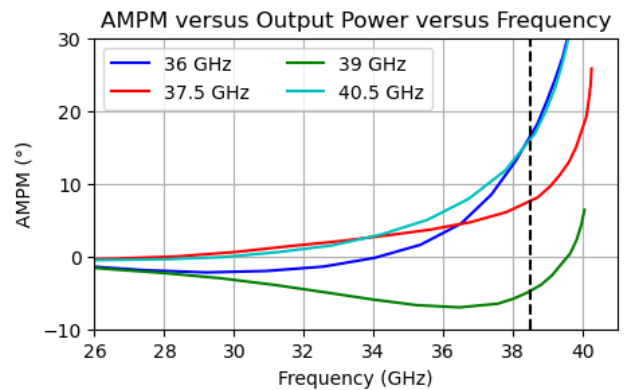
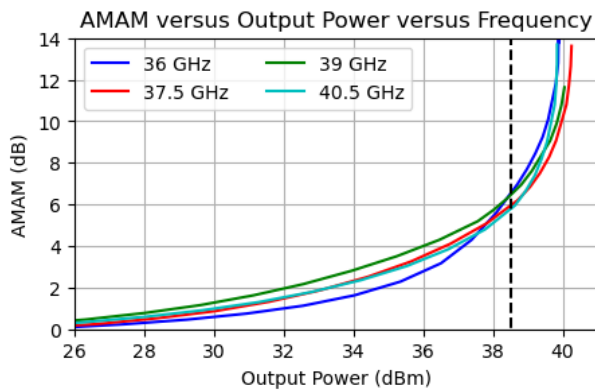
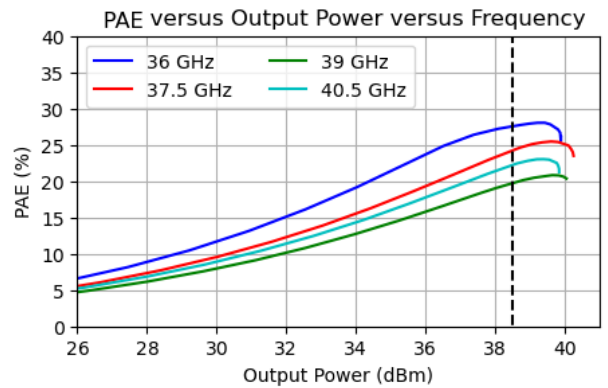
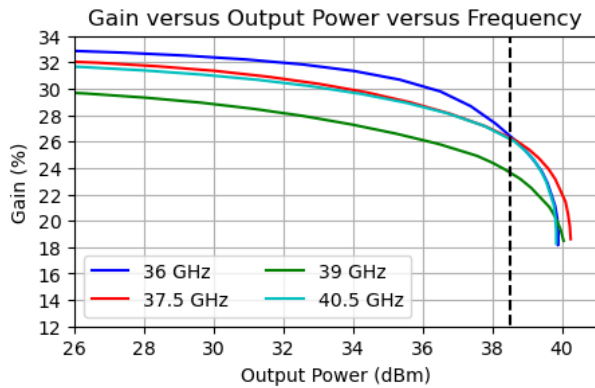
Test conditions :  $V_D = 20V$ ,  $I_{dq} = 290mA$ ,  $T_{case} = -40^\circ C / 25^\circ C / 85^\circ C$





**Performance versus output power and frequency**

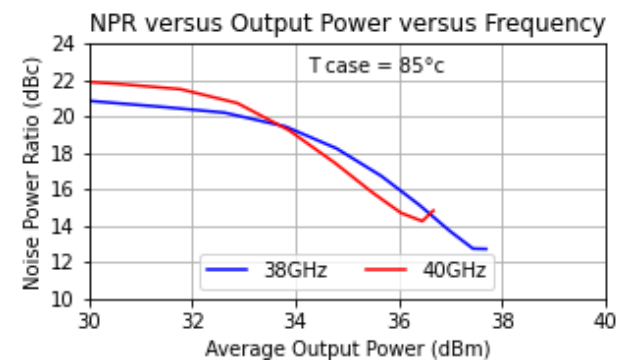
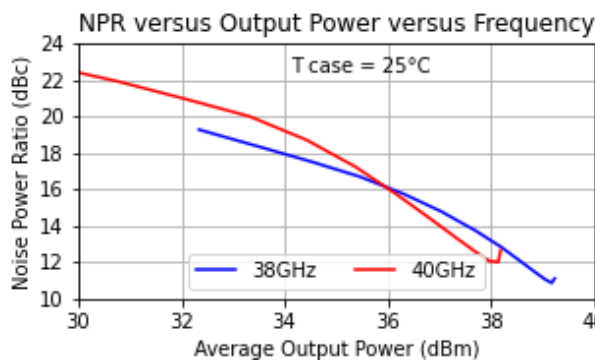
**Test conditions :**  $V_D = 20V$ ,  $I_{dq} = 290mA$ , Frequency = 36 / 37.5 / 39 / 40.5 GHz,  $T_{case} = 25^\circ C$



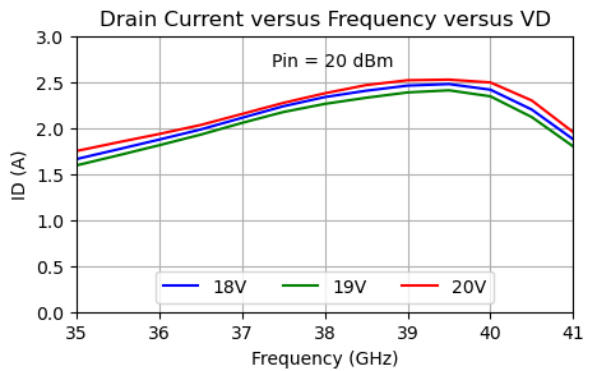
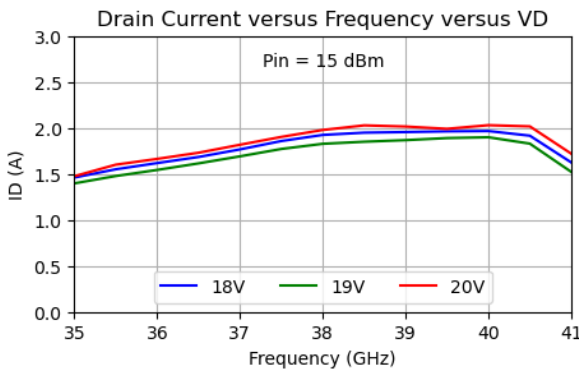
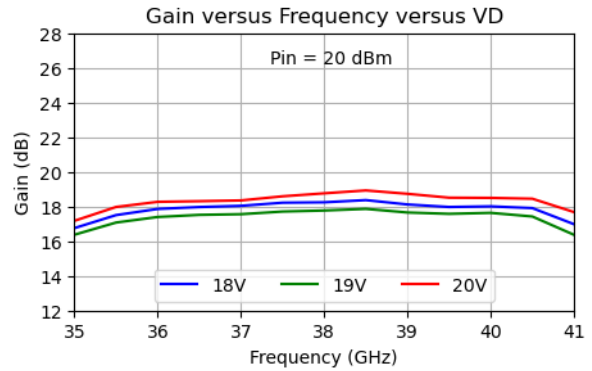
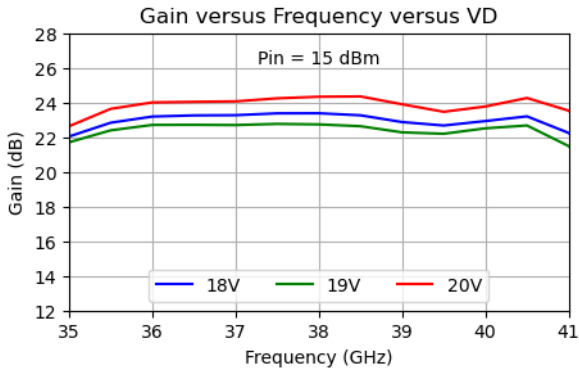
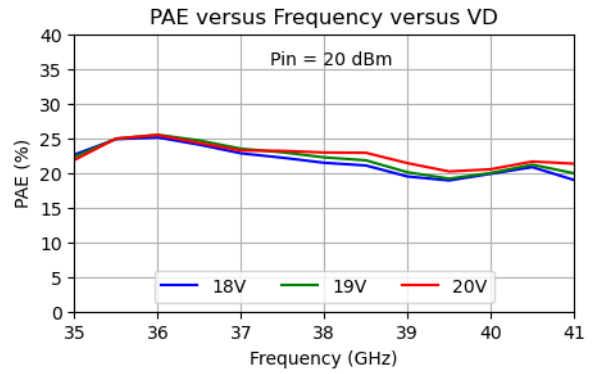
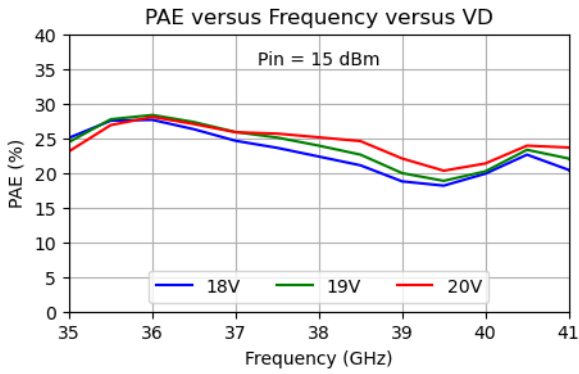
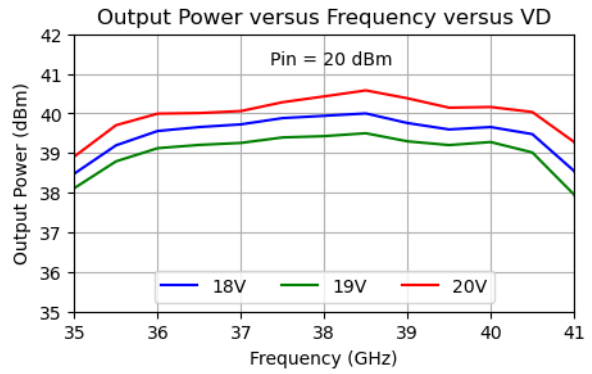
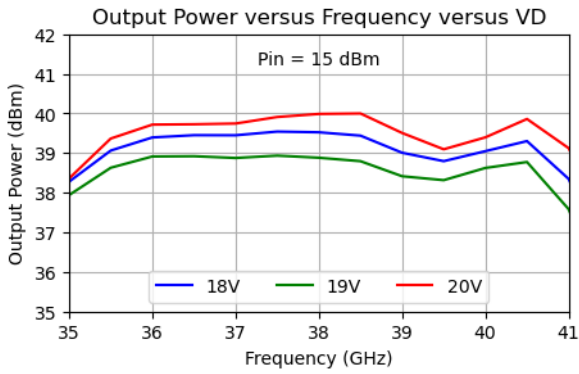
<sup>1</sup>Dotted line represents approximately 6 dB compression

**Noise Power Ratio versus Output Power and Frequency**

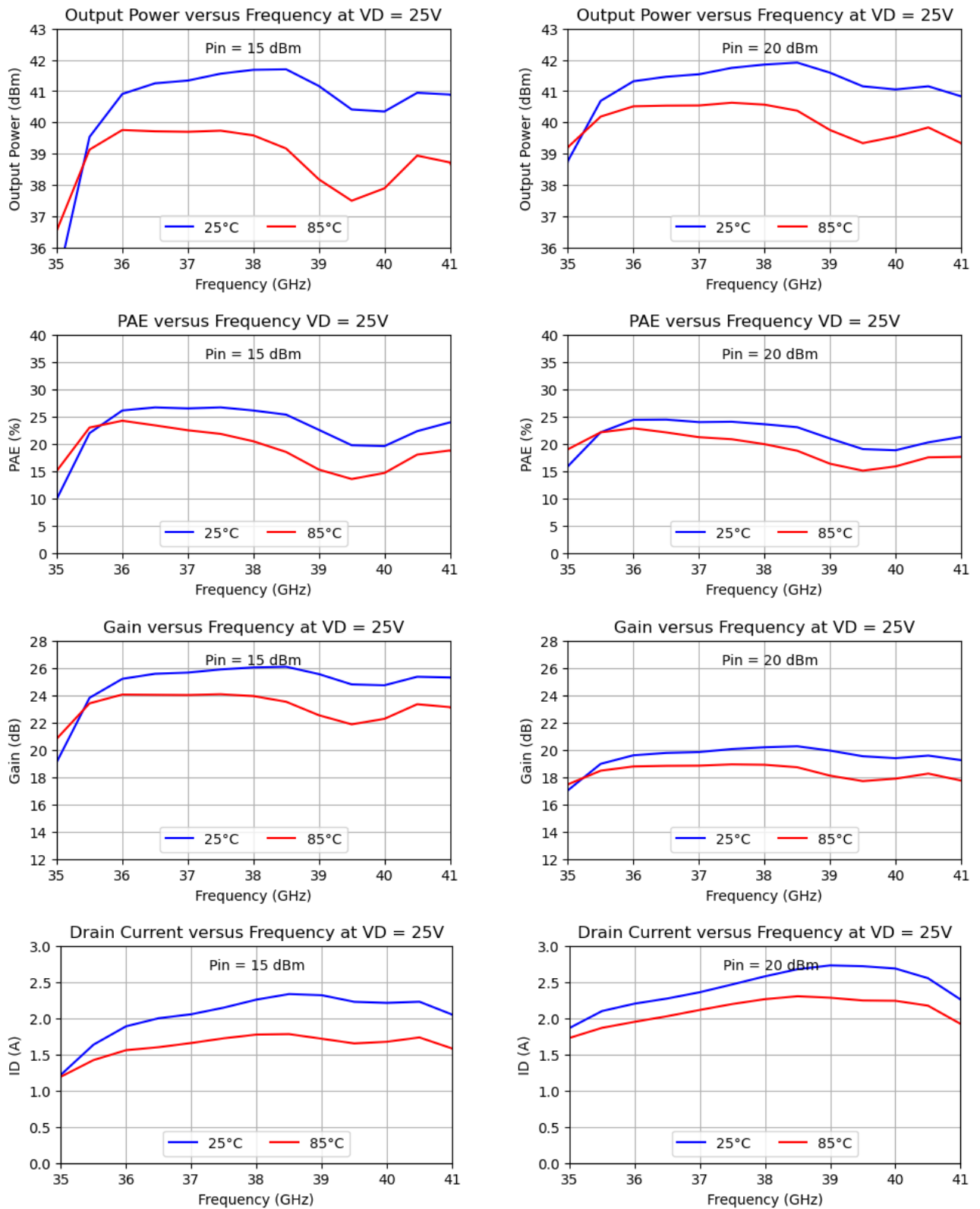
**Test conditions :**  $V_D = 20V$ ,  $I_{dq} = 290mA$ ,  $T_{case} = 25^\circ C / 85^\circ C$



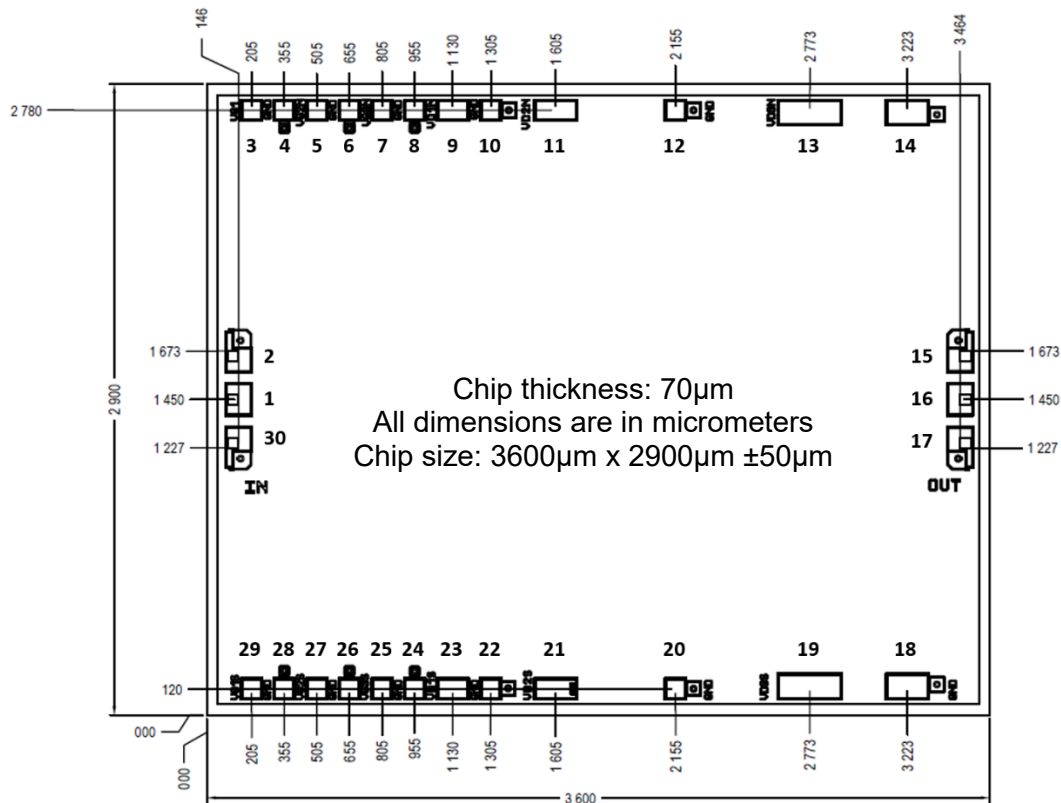
**Performance versus frequency and DC drain voltage**  
**Test conditions :**  $V_D = 18V / 19V / 20V$ ,  $I_{dq} = 290mA$ ,  $T_{case} = 25^\circ C$



**Performance versus frequency and temperature**  
**Test conditions :**  $V_D = 25V$ ,  $I_{dq} = 290mA$ ,  $T_{case} = 25^\circ C / 85^\circ C$

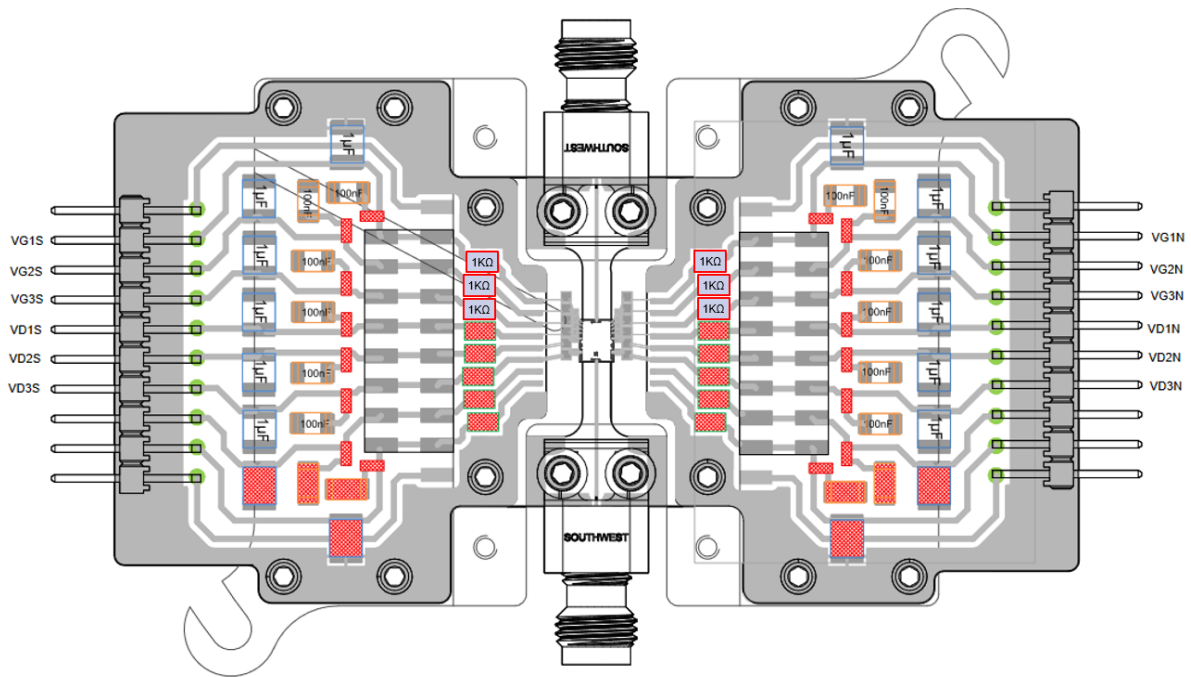


## Mechanical Data

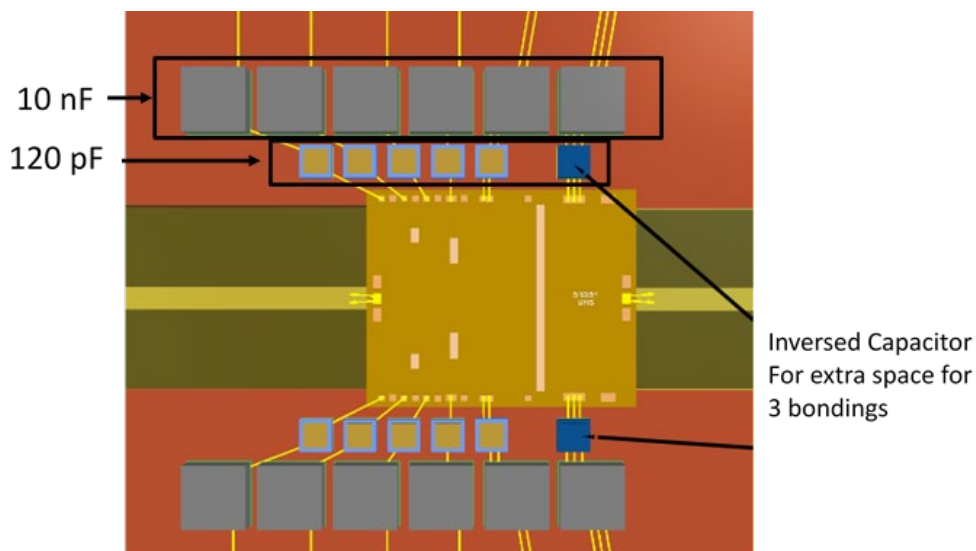


PAD Number	Name	Description	Pad size
1	RF IN	Input RF port	186µm x 105µm
3	G12	DC Gate voltage, 1 <sup>st</sup> & 2 <sup>st</sup> stage, North	96µm x 96µm
5	G3	DC Gate voltage 3 <sup>d</sup> stage, North	96µm x 96µm
7	G4	DC Gate voltage 4 <sup>th</sup> stage, North	96µm x 96µm
9	D12	DC Drain voltage, 1 <sup>st</sup> & 2 <sup>st</sup> stage, North	146µm x 96µm
11	D3	DC Drain voltage 3 <sup>d</sup> stage, North	196µm x 96µm
13	D4	DC Drain voltage 4 <sup>th</sup> stage, North	296µm x 116µm
16	RF OUT	Output RF port	118 µm x146 µm
19	D4	DC Drain voltage 4 <sup>th</sup> stage, South	296µm x 116µm
21	D3	DC Drain voltage 3 <sup>d</sup> stage, South	196µm x 96µm
23	D12	DC Drain voltage, 1 <sup>st</sup> & 2 <sup>st</sup> stage, South	146µm x 96µm
25	G4	DC Gate voltage 4 <sup>th</sup> stage, South	96µm x 96µm
27	G3	DC Gate voltage 3 <sup>d</sup> stage, South	96µm x 96µm
29	G12	DC Gait voltage, 1 <sup>st</sup> & 2 <sup>st</sup> stage, South	96µm x 96µm
2,4,6,8,10,12,14, 15,17,18,20,22, 24,26,28,30	GND	NC (Ground)	96µm x 96µm

**Recommended Evaluation Board**



**Recommended Assembly Plan**



4 levels of decoupling capacitor have been used, 2 on the tab and 2 on the board. The first level is composed of 120 pF chip capacitors, the second level is composed of 10nF chip capacitors, the third level is composed of 100nF SMD 1210 capacitors and the fourth stage is composed of 1µF SMD 1206 capacitors. The first two levels should be as close as possible to the die. A 1KΩ resistor was added in series on each gate supply.

## Recommended reflow process assembly

Refer to the application note AN0001 available at <https://www.ums-rf.com> for die attach.

## Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <https://www.ums-rf.com>.

## Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations for the UMS package products.

## Ordering Information

Chip form : CHA7452-99F/00

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