CHA2110-98F

7-12GHz LNA

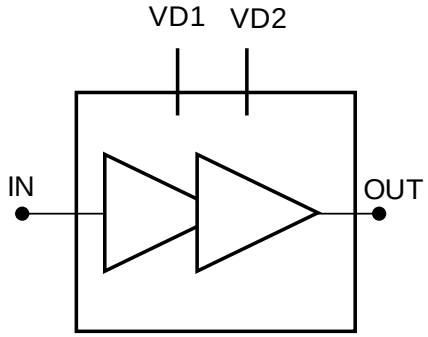
GaAs Monolithic Microwave IC

Description

The CHA2110-98F is a monolithic two-stage wide band low noise amplifier circuit. It is self-biased.
It is designed for military, space and telecommunication systems.

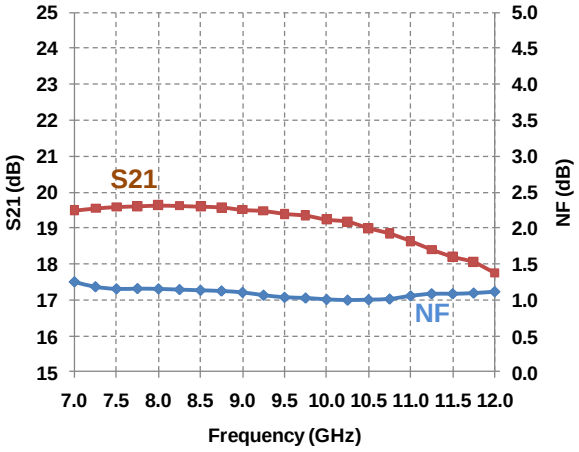
The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate and air bridges.

It is available in chip form.



Main Features

- Broadband performances: 7-12GHz
- Linear gain: 19dB
- Return Losses: 12dB
- Noise Figure: 1.2dB
- Output power @ 1dBcomp: 11dBm
- DC bias: Vd=4 Volt@Id=45mA
- Chip size 1.93x1.3x0.1mm



Gain and NF versus frequency

Main Electrical Characteristics

Tamb.= +25°C; pads 1A, 1B, 2A and 2B are non-connected

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	7		12	GHz
Gain	Linear Gain		19		dB
NF	Noise Figure		1.2		dB
Pout	Output Power @1dB comp (f=10GHz)		11		dBm

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Electrical Characteristics

Tamb.= +25°C; pads 1A, 1B, 2A and 2B are non-connected

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	7		12	GHz
Gain	Linear Gain	18 (7-10.5GHz) 16.5 (10.5-12GHz)	19	21	dB
NF	Noise Figure		1.2	1.5	dB
RL_in	Input return losses		-12	-5	dB
RL_out	Output return losses		-12	-9	dB
P1dB	Output power at 1dB comp (f=10GHz)	9.5	11	12.5	dBm
IP3	3rd order interception point (f=10GHz)		21		dB
Vd	Drain supply voltage (self biased)		4		V
Id	Drain supply current		45	55	mA

These values are representative of measurements on test fixture.

Absolute Maximum Ratings (1)

Tamb.= +25°C; pads 1A, 1B, 2A and 2B are non-connected

Symbol	Parameter	Values	Unit
Max Pin ON	No damage maximum input power	15	dBm
Max Pin OFF	No damage maximum input power (Vd=0V)	18	dBm
Vd	Drain bias voltage	5V	V
Id	Drain bias current	70	mA
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Typical Bias Conditions

Tamb.= +25°C; pads 1A, 1B, 2A and 2B are non-connected

Symbol	Pad N°	Parameter	Values	Unit
Vd	VD1, VD2	Drain supply voltage	4	V

The circuit is self-biased.

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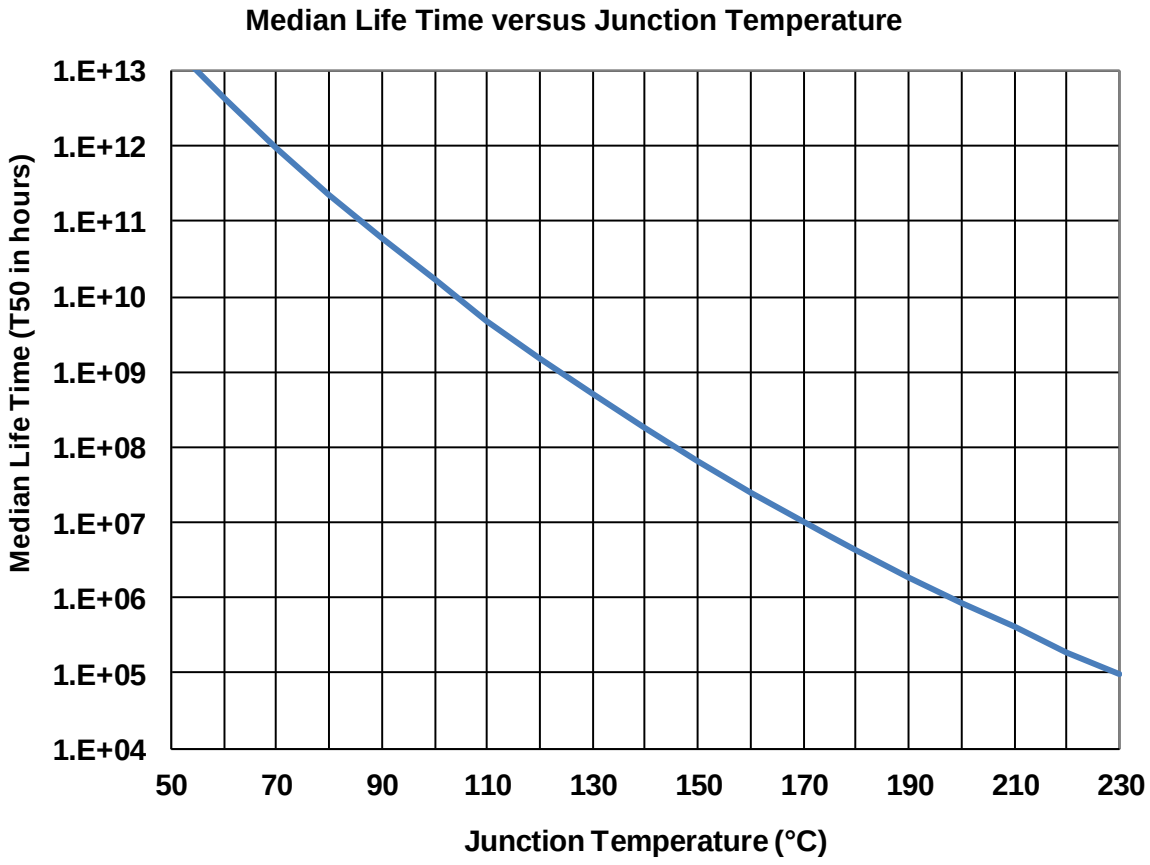
Device thermal information

The thermal performances of the device given below are based on UMS rules to evaluate the junction temperature.
This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHA2110-98F is fabricated (AsGa Power PHEMT 0.25µm).
The temperature Tb is defined as the chip back side temperature
The thermal resistance (Rth_eq) is given for the full circuit and assumes CW operation mode as given in the table.

Parameters	Symbol	Conditions	Value	Unit
Thermal Resistance	Rth_eq	**Tb=85°C**, Vd=4V, Id_drive=0.041A Pin=-20dBm Pout=-2dBm Pdiss=0,164W **CW mode**	105	°C/W
Junction Temperature	Tj		104	°C
Median Life	T50		$1x10^{10}$	Hrs



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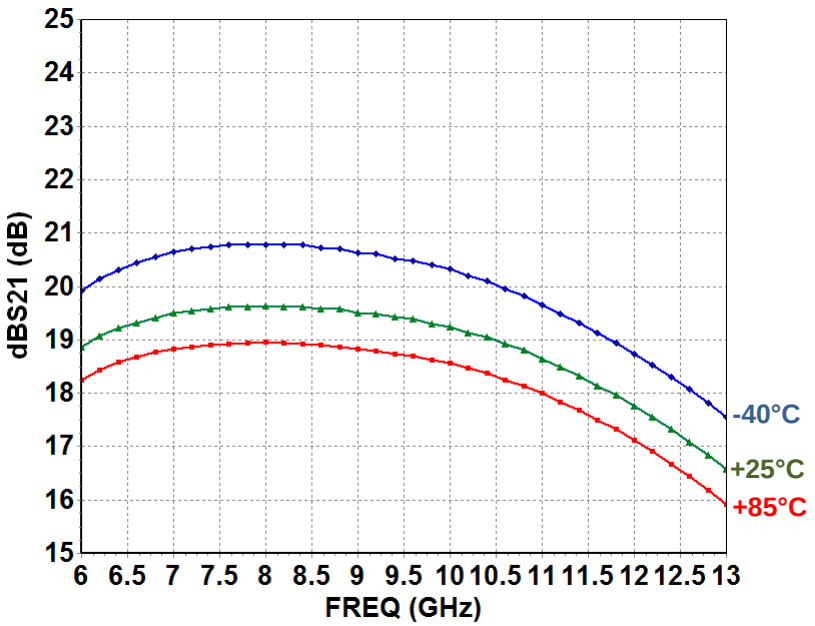
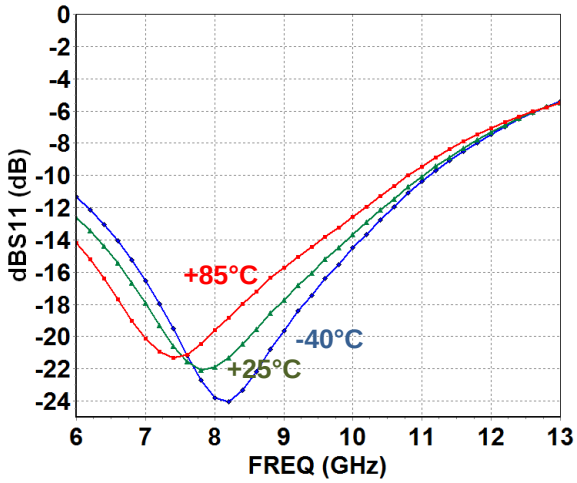
Test fixture Measurements

T = [-40°C ; +25°C ; +85°C],
Vd = +4V, Id = 45mA; pads 1A, 1B, 2A and 2B are non-connected

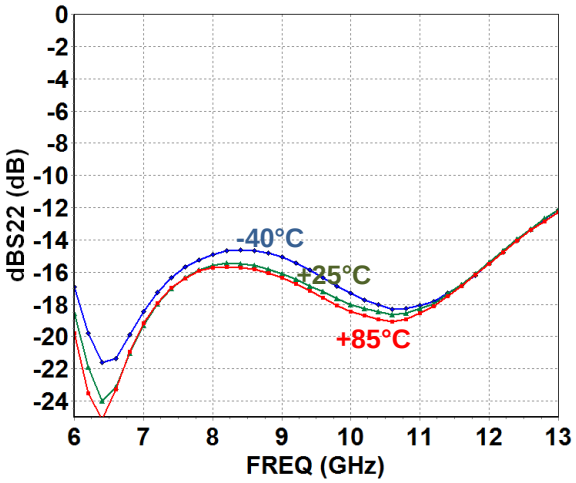
S21 versus frequency



Input return loss



Output Return loss



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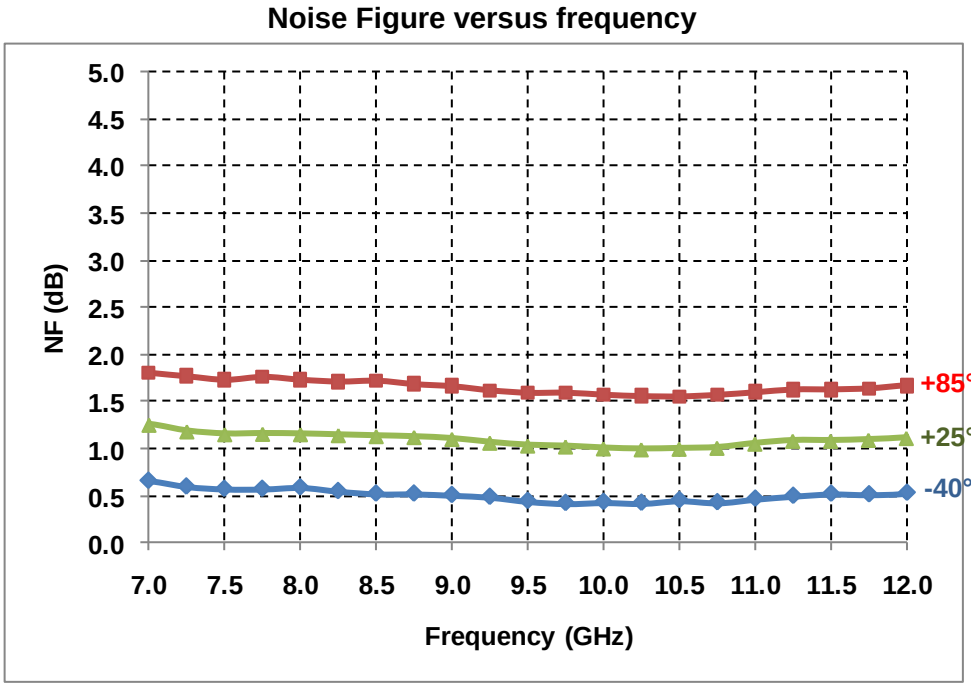

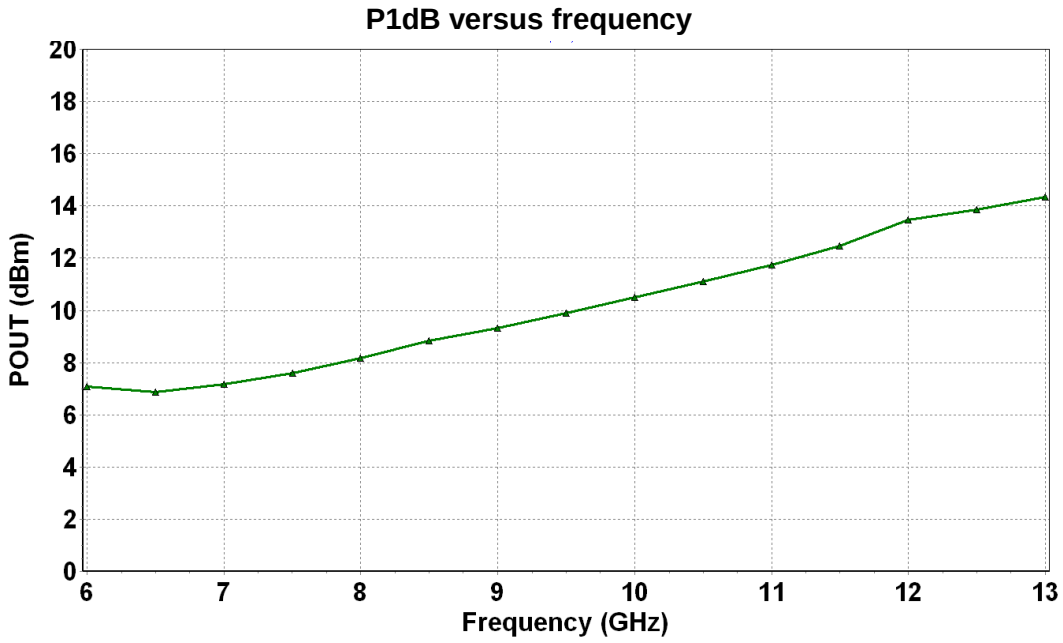

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Test fixture Measurements

Tamb=+25°C,
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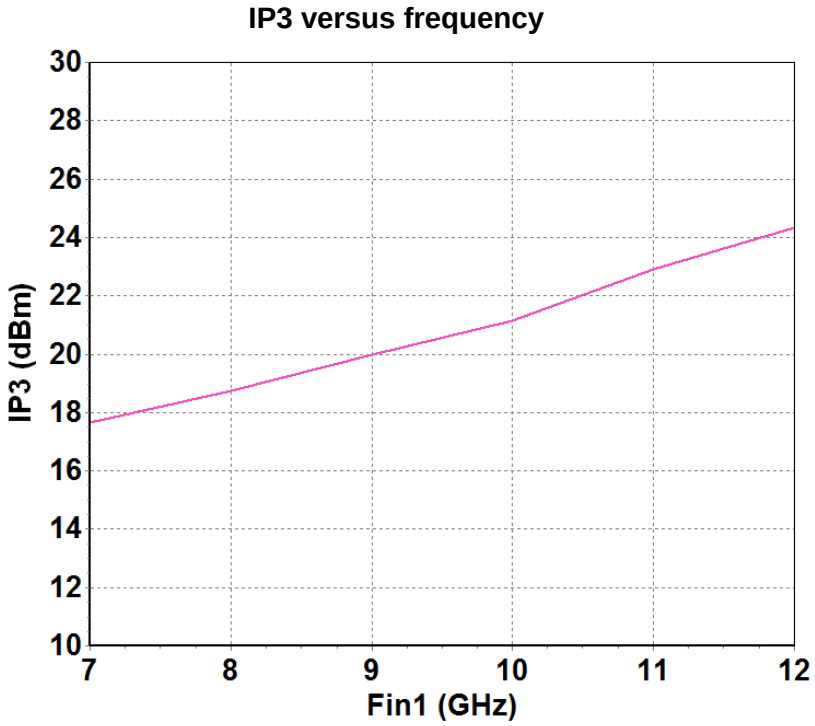

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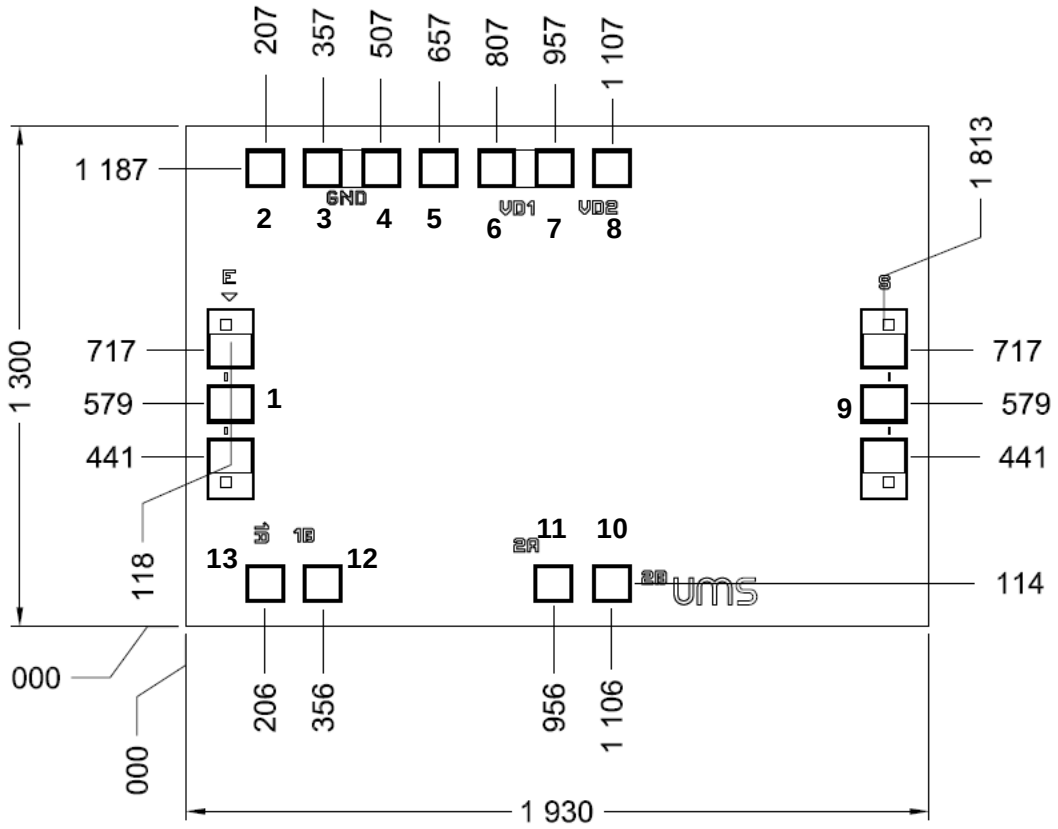
Mechanical data



Chip thickness: 100µm.
Chip size: 1300x1930 ±35µm
All dimensions are in micrometers

RF pads (1, 9) = 82x105µm² (BCB passivation opening)
DC pads (2,3,4,5,6,7,8,10,11,12,13) = 82x86µm² (BCB passivation opening)

Pin number	Pin name	Description
1	E	Input RF
2	none	NC
3, 4	GND	NC
5	none	NC
6, 7	VD1	Vd
8	VD2	Vd
9	S	Output RF
10	2B	NC
11	2A	NC
12	1B	NC
13	1A	NC

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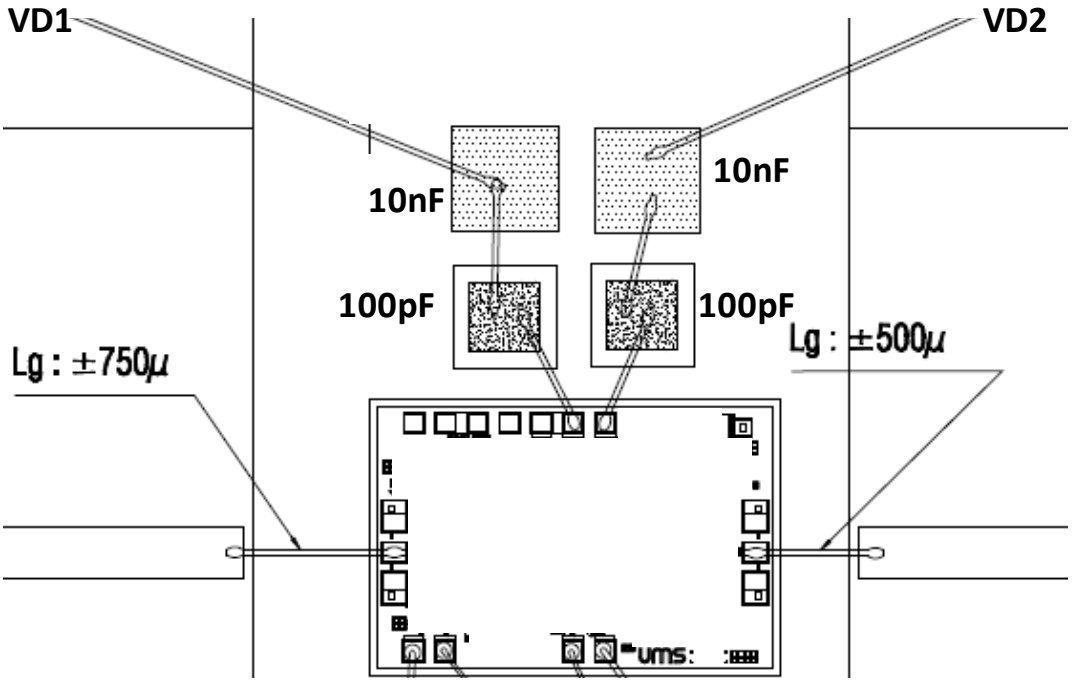
Recommended assembly plan



Note: Supply feed should be bypassed. 25µm diameter gold wire is to be preferred.

Recommended circuit bonding table

Label	Type	Decoupling	Comment
E	Input RF	N/A	Inductance (Lbonding≈750µm) = 0.6nH, 1 gold wire with diameter of 25µm
Vd1, Vd2	Vd	100pF & 10nF	Drain Supply Inductance ≤ 1nH
S	Output RF	N/A	Inductance (Lbonding≈500µm) = 0.4nH, 1 gold wire with diameter of 25µm

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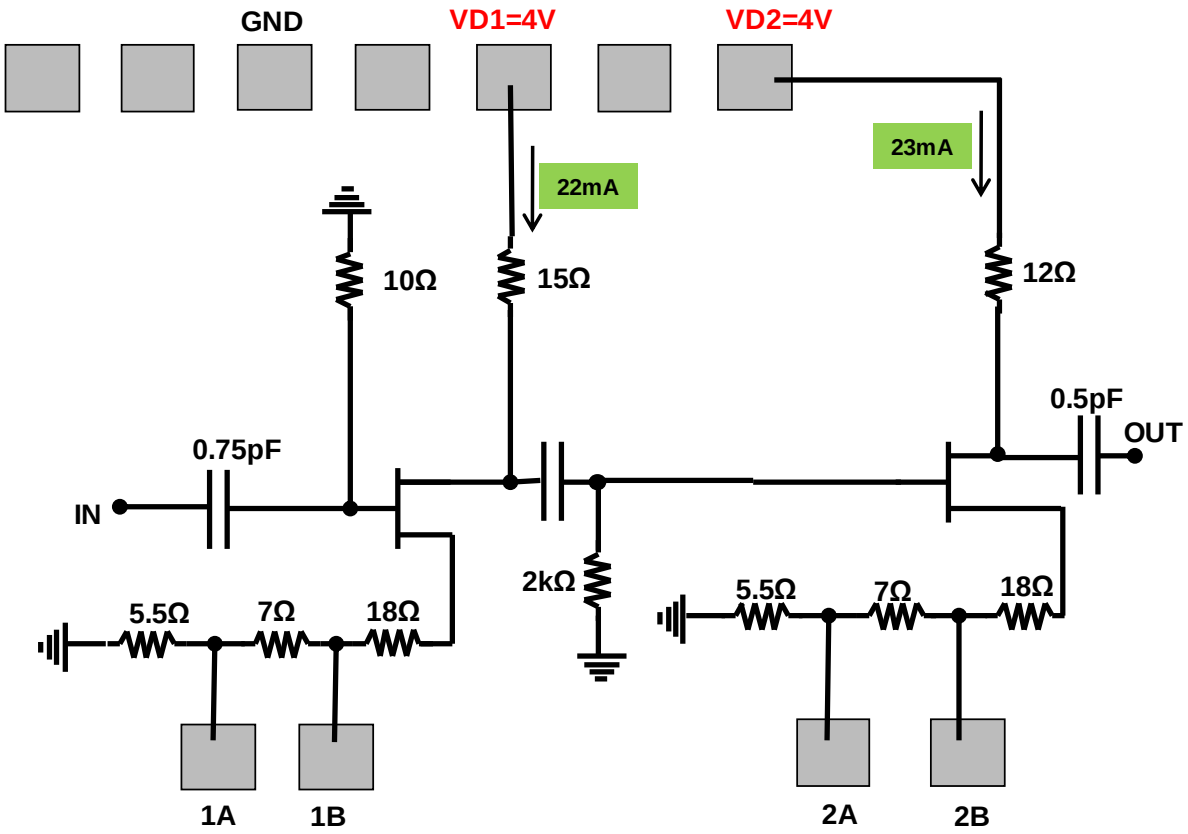
Chip biasing options

This chip is self-biased, and flexibility is provided by the access to number of pads. The internal DC electrical schematic is given in order to use these pads in a safe way.



The requirement is :
Not to exceed Vds = 3.5Volt (internal Drain to Source voltage).

We propose three standard biasing :

Low Noise and low consumption:	Vd = 4V. The pads 1A, 1B, 2A and 2B are non-connected (NC). Idd = 45mA & Pout-1dB = +11dBm Typical (f=10GHz).
Low Noise and higher gain:	Vd = 4V and 1A or 1B grounded. All the other pads non connected (NC). Idd = 55mA & Pout-1dB = +11dBm Typical (f=10GHz)
Low Noise and higher output power:	Vd = 4V and 2A or 2B grounded. All the other pads non connected (NC). Idd = 55mA & Pout-1dB = +13dBm Typical (f=10GHz)

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Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Ordering Information

Chip form:	CHA2110-98F/00

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