

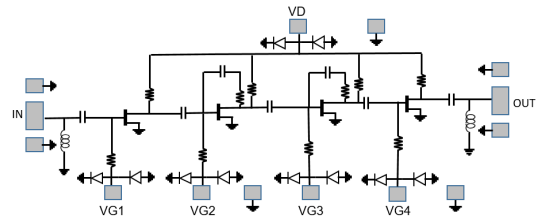
## 50-71GHz Low Noise Amplifier GaAs Monolithic Microwave IC

### Description

The CHA2368-98F is a four stage monolithic Low Noise Amplifier, which exhibits 21dB linear gain and 3.5dB Noise Figure in the frequency band 50-71GHz. It includes ESD protections on each RF access and DC pads.

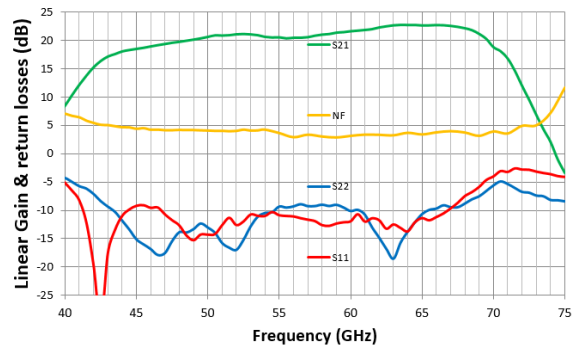
This amplifier is designed for a wide range of applications, from Commercial to Space communication systems.

It is manufactured with a pHEMT process, 0.1µm gate length, via holes through the substrate, air bridges and electron beam gate lithography and is available in bare die with BCB layer protection.



### Main Features

- Frequency Range: 50-71GHz
- Noise Figure: 3.5dB
- P1dB : 12dBm
- Gain: 21dB
- Gain control: 30dB
- BCB layer protection
- Typical DC bias: Vd=3.3V @Id=75mA
- Chip size 2.57mmx1.17mmx0.07mm



Typical S parameters and Noise Figure

### Main Electrical Characteristics

Tcase= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	50		71	GHz
Gain	Linear Gain		21		dB
NF	Noise Figure		3.5		dB
P <sub>1dB</sub>	Output Power @1dB compression		12		dBm

## Electrical Characteristics

T<sub>case</sub> = +25°C, V<sub>d</sub>(D) = 3.3V, V<sub>G</sub>(G1=G2=G3~0V) set in order to get I<sub>dq</sub> = 75mA

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	50		71	GHz
Gain	Linear Gain		21		dB
NF	Noise Figure		3.5		dB
IRL	Input return loss		10		dB
ORL	Output return loss		10		dB
G <sub>CTRL</sub>	Gain control range		30		dB
IP-1dB	Input power at 1dB gain compression		-8		dBm
OP-1dB	Output power at 1dB gain compression		12		dBm
V <sub>d</sub>	Drain bias voltage		3.3		V
I <sub>d</sub>	Drain bias current		75		mA

These values are representative of on-board measurements as defined on the drawing in paragraph "Evaluation board".

**Absolute Maximum Ratings** <sup>(1)</sup>T<sub>case</sub>= +25°C

Symbol	Parameter	Values	Unit
V <sub>d</sub>	Drain bias voltage	4V	V
V <sub>g</sub>	Gate bias voltage	-1.5 to +0.4	V
P <sub>in</sub>	Maximum peak input power overdrive	2	dBm
T <sub>j</sub>	Junction temperature	175	°C

<sup>(1)</sup> Operation of this device above anyone of these parameters may cause permanent damage.

**Recommended Operating Range** <sup>3, 4</sup>

Symbol	Parameter	Values	Unit
V <sub>d</sub>	Drain bias voltage	3.0 to 3.5	V
I <sub>d</sub>	Drain bias current	74 to 90	mA
V <sub>g</sub>	Gate bias voltage	-0.5 to +0.1	V
P <sub>in</sub>	Input power range	-20 to 0	dBm

<sup>(3)</sup> Electrical performances are defined for specified test conditions

<sup>(4)</sup> Electrical performances are not guaranteed over all recommended operating conditions

## Temperature Range

Tcase	Operating temperature range	-40 to +95	°C
Tstg	Storage temperature range	-55 to +150	°C

## Typical Bias Conditions

Tcase= +25°C

Symbol	Pad N°	Parameter	Values	Unit
VG1	9	Gate voltage tuned for Idq ~75mA	+0	V
VG2	7			
VG3	5			
VD	2	Drain Voltage	3.3	V

## “Power ON” sequence

1. Ground the device
2. Bias LNA gate voltage at Vgs close to Vpinch-off (G1=G2=G3=0.5V -1.5V)
3. Apply Vds quiescent bias voltage (Vd = 3.3V)
4. Increase slowly Vg1 up to 0V and 2<sup>nd</sup> & 3<sup>rd</sup> stage Vgs up to quiescent bias drain current Idq (100mA for total Idq current)
5. Apply RF input power

## “Power OFF” sequence

1. Remove RF input power
2. Bias LNA gate voltage at Vgs close to Vpinch-off (G1=G2=G3=0.5V -1.5V)
3. Set drain voltage to 0V
4. Set gate voltage to 0V

**Device thermal performances**

The device thermal performances below are based on UMS rules to evaluate the junction temperature.

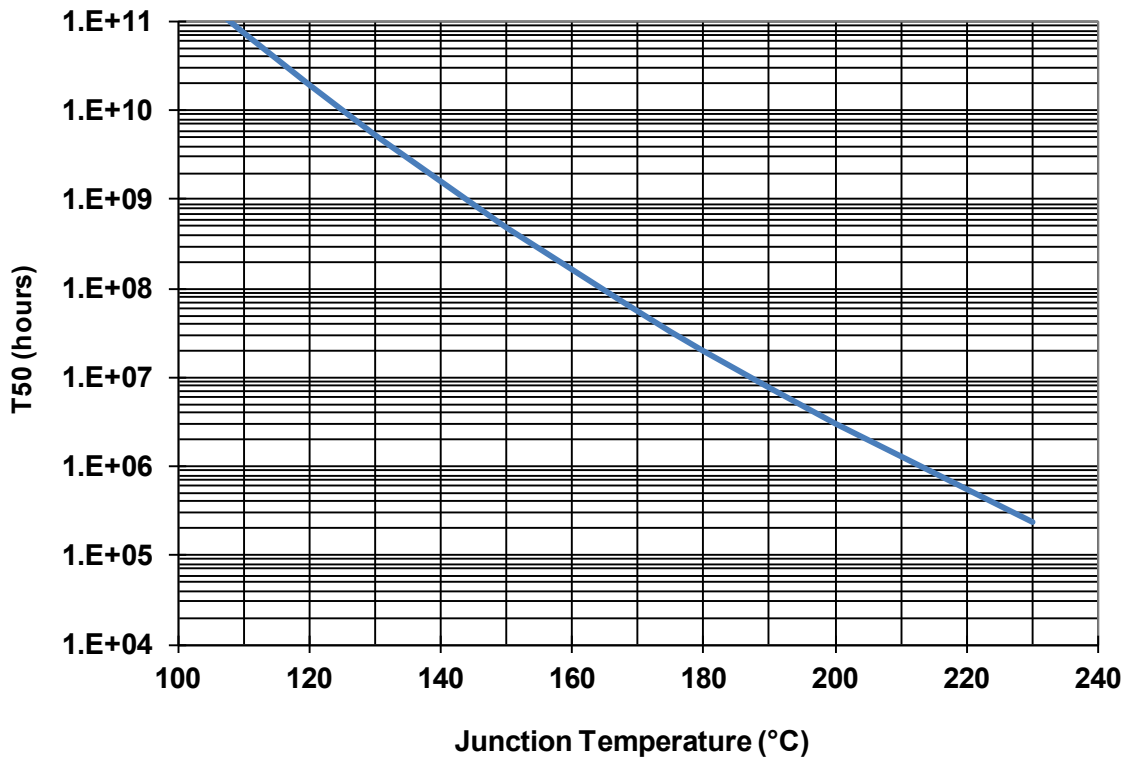
The temperature  $T_c$  ( $T_{b\text{ chip}}$ ) is defined as the chip backside temperature.

The system maximum temperature must be adjusted in order to guarantee that  $T_{\text{junction}}$  remains below the maximum value specified in the Absolute Maximum Ratings table.

Therefore, the PCB system must be designed to comply with this requirement.

Parameter	Biasing conditions	$T_{\text{junction}}$ (°C)	$R_{\text{TH}}$ (°C/W)	T50 (hours)
$R_{\text{TH}}^{(1)}$ Thermal Resistance ( Junction to Case)	$V_d = 3.3V$ $I_d = 75mA$ $P_{\text{diss}} = 0.24W$	150	270	$5 \times 10^8$

<sup>(1)</sup> Assuming 85° Tcase



## Typical on-board Sij parameters

Tcase= +25°C, Vd = +3.3V, Id = 75mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
40	-5,25	131,06	-51,62	17,91	9,22	94,76	-4,32	164,49
40.5	-6,70	102,97	-56,84	3,76	11,09	54,82	-5,03	137,15
41	-8,51	70,09	-51,96	-13,32	12,82	12,61	-5,76	112,07
41.5	-12,43	31,08	-49,95	77,36	14,32	-31,34	-6,19	84,42
42	-20,48	-8,46	-50,01	10,36	15,61	-77,18	-7,13	53,08
42.5	-30,30	-77,84	-52,73	96,24	16,6	-123,6	-8,39	24,58
43	-17,16	129,54	-50,13	66,33	17,29	-169,97	-9,35	-5,77
43.5	-13,12	87,74	-47,70	-13,92	17,75	144,18	-10,27	-37,76
44	-10,70	55,92	-50,62	16,06	18,27	99,4	-11,80	-71,42
44.5	-9,77	24,44	-51,82	-22,49	18,6		-13,36	-106,85
45	-9,42	-6,02	-51,96	-54,81	18,8	55,03	-15,08	-141,85
45.5	-9,05	-35,42	-52,41	7,62	19,12	11,85	-15,96	-0,08
46	-9,44	-61,80	-51,59	0,07	19,35	-30,22	-16,78	132,48
46.5	-9,61	-92,91	-48,84	-2,98	19,53	-72,35	-17,83	80,60
47	-10,94	-122,29	-48,45	-46,61	19,71	-114,35	-17,47	41,63
47.5	-11,76	-63,70	-53,92	-9,50	19,86	-156,11	-15,38	7,58
48	-12,51	-8,76	-52,90	-21,62	19,97	162,53	-13,83	-33,58
48.5	-14,09	129,19	-51,39	10,70	20,1	121,04	-13,88	-65,46
49	-15,61	95,56	-49,30	8,24	20,26	79,66	-13,28	-88,55
49.5	-14,63	53,94	-49,79	61,53	20,44	38,5	-12,30	-120,76
50	-14,77	12,89	-48,25	4,01	20,67	-2,15	-13,01	-158,47
50.5	-14,30	-16,81	-51,73	-35,00	20,88	-43,92	-13,93	165,46
51	-12,83	-42,82	-47,21	-26,85	20,74	-86,01	-15,73	125,21
51.5	-11,52	-72,13	-50,13	-79,47	20,88	-129,05	-16,55	81,38
52	-12,35	-102,61	-50,20	-10,90	20,98	-169,13	-16,92	27,39
52.5	-12,02	-120,74	-50,04	-45,88	21,02	148,76	-15,15	-16,48
53	-10,68	-53,54	-49,58	5,35	20,91	106,98	-12,80	-57,47
53.5	-10,86	-83,34	-50,50	-7,26	20,78	64,58	-11,10	-97,97
54	-10,73	-17,69	-48,21	5,89	20,53	22,72	-10,46	-133,78
54.5	-9,97	138,72	-49,27	8,20	20,6	-18,38	-10,32	-163,34
55	-10,26	114,92	-47,02	43,14	20,55	-56,58	-9,32	168,65
55.5	-10,89	92,62	-51,49	-14,54	20,45	-98,01	-9,51	138,48
56	-11,03	70,18	-49,56	-28,33	20,57	-137,68	-9,29	113,17
56.5	-11,42	46,97	-52,08	38,12	20,6	-177,1	-8,92	85,64
57	-11,61	24,60	-45,16	0,13	20,72	142,64	-9,26	60,31
57.5	-11,83	6,15	-44,62	-23,47	20,94	103,3	-9,24	37,42
58	-12,19	-11,93	-43,86	-65,93	21,04	63,17	-9,01	11,41
58.5	-12,10	-28,50	-48,06	-69,45	21,22	21,85	-9,23	-11,54
59	-11,56	-41,19	-47,02	-87,69	21,42	-19,14	-9,02	-34,27
59.5	-11,88	-64,36	-45,22	-60,68	21,52	-60,64	-9,50	-59,36
60	-12,25	-77,81	-47,70	48,78	21,69	-102,4	-10,12	-81,84
60.5	-11,27	-102,44	-47,86	42,37	21,82	-144,22	-9,91	-104,29
61	-12,09	-35,60	-48,26	18,99	21,96	173,79	-10,76	-128,00

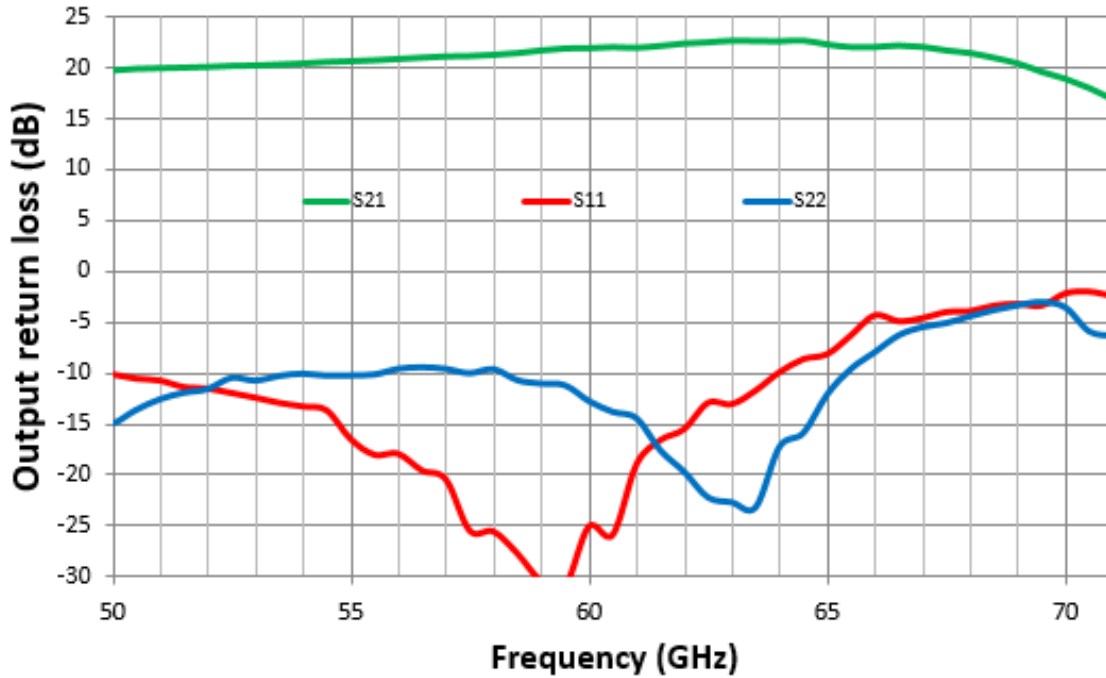
61.5	-11,51	-49,89	-48,83	28,61	22,15	131,8	-12,98	-151,49
62	-11,54	-66,08	-49,93	64,79	22,43	-54.03	-14,78	-163,19
62.5	-12,78	-78,90	-49,67	40,04	22,61	-72.11	-16,76	-179,01
63	-12,32	-88,70	-46,80	-17,71	22,79	-90.32	-18,48	-163,82
63.5	-12,84	-14,89	-47,54	17,86	22,89	-108.79	-15,64	-161,71
64	-13,34	147,86	-50,96	14,93	22,88	-128.32	-13,72	-0,07
64.5	-11,91	128,96	-46,89	-58,35	22,91	-148.17	-12,10	164,41
65	-11,40	105,22	-45,50	-66,14	22,83	-168.55	-10,66	142,62
65.5	-11,16	79,82	-46,06	-4,26	22,82	173.30	-9,92	112,45
66	-10,68	54,51	-45,85	-18,62	22,84	154.58	-9,69	84,26
66.5	-9,98	17,68	-45,54	30,56	22,67	133.14	-9,10	52,29
67	-9,69	-14,70	-46,74	45,73	22,53	110.29	-9,43	11,68
67.5	-9,03	-52,15	-51,13	42,94	22,3	87.74	-9,45	-22,59
68	-7,34	-86,19	-47,25	67,12	22,02	64.55	-8,81	-59,45
68.5	-6,45	-114,21	-46,39	5,35	21,63	40.27	-8,05	-97,64
69	-5,55	-53,05	-48,39	24,33	20,95	14.06	-7,53	-133,97
69.5	-4,63	-85,04	-49,76	-2,94	20,02	-13.39	-6,60	-163,02
70	-3,92	150,56	-51,85	1,08	18,56	-41.26	-5,63	164,72
70.5	-3.06	-145.00	-49.12	-11.99	18.03	-53.55	-4.92	144.16
71	-3.2	-146.84	-48.64	46.68	16.93	-71.90	-5.37	139.92

## Typical on board Measurements

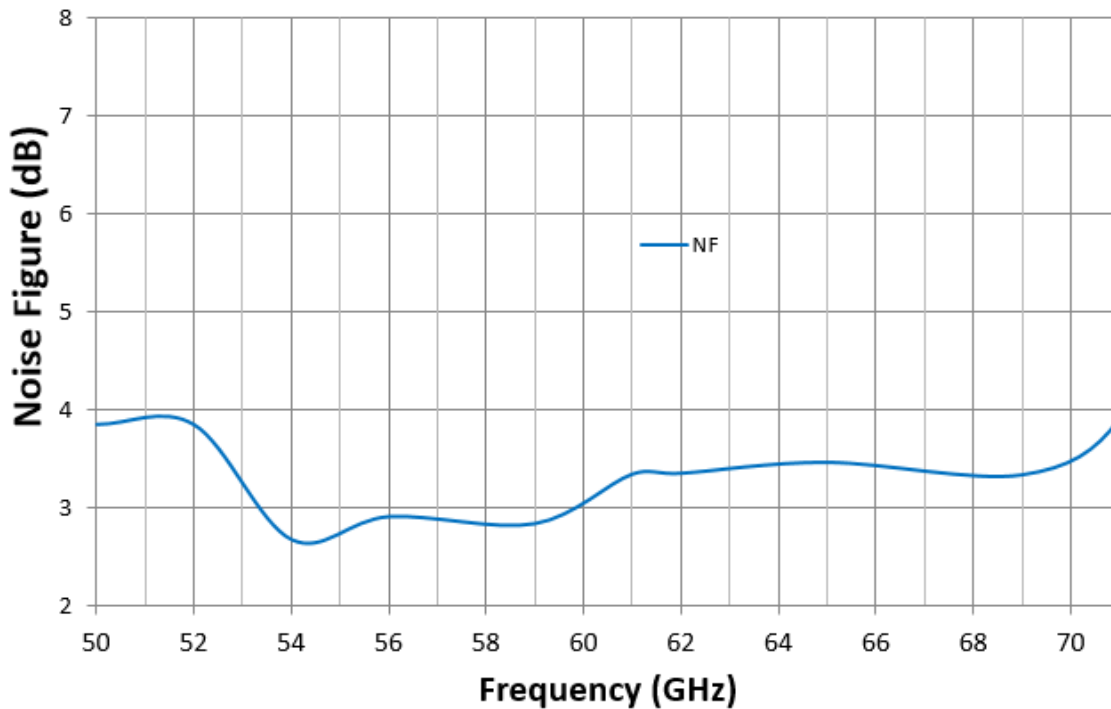
T<sub>case</sub> = +25°C, V<sub>d</sub> = +3.3V, I<sub>d</sub> = 75mA, Typical

Losses due to board are de-embedded. Measurements are given in the die access plan.

### Linear Gain & return losses versus Frequency



### Noise Figure versus VD & Frequency

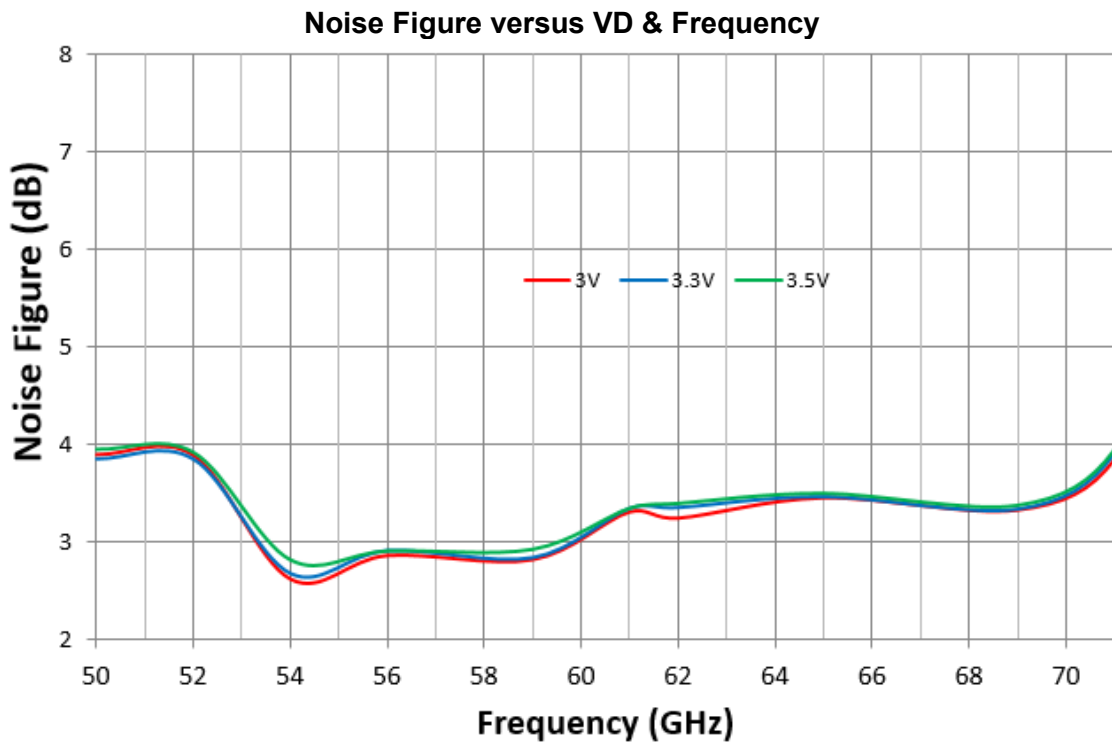
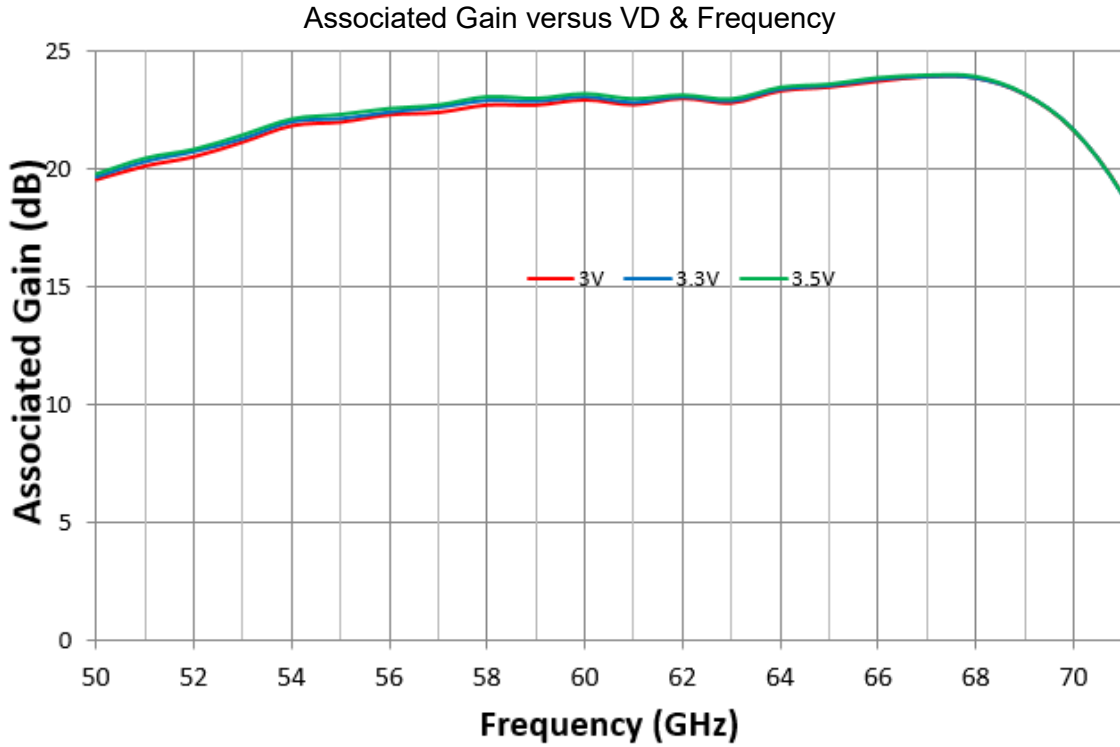




**Typical on board Measurements**

Tcase= +25°C, Vd = +3.3V, Id = 75mA, Typical

Losses due to board are de-embedded. Measurements are given in the die access plan.

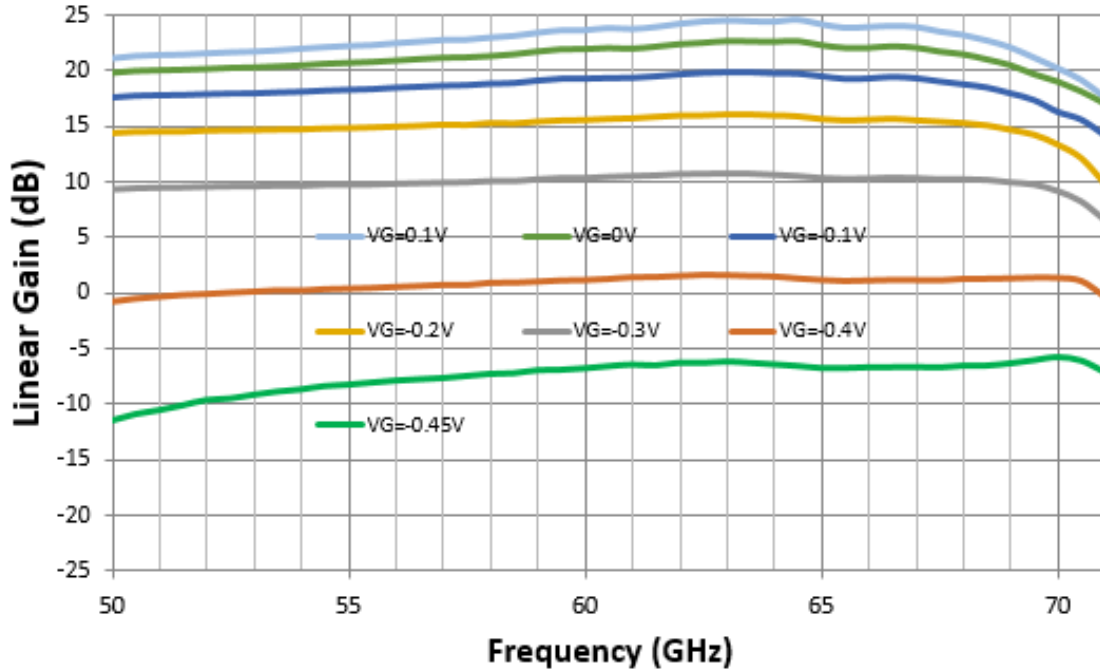


## Typical on board Measurements

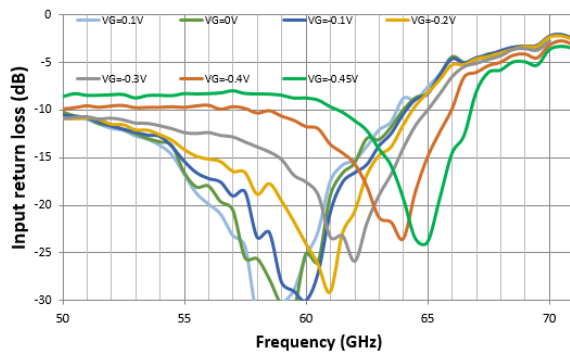
Tcase= +25°C, Vd = +3.3V, Id = 75mA, Typical

Losses due to board are de-embedded. Measurements are given in the die access plan.

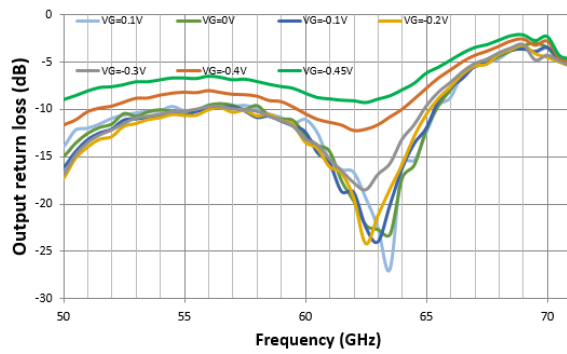
### Linear Gain versus VG & Frequency



### Input return loss versus VG & Frequency



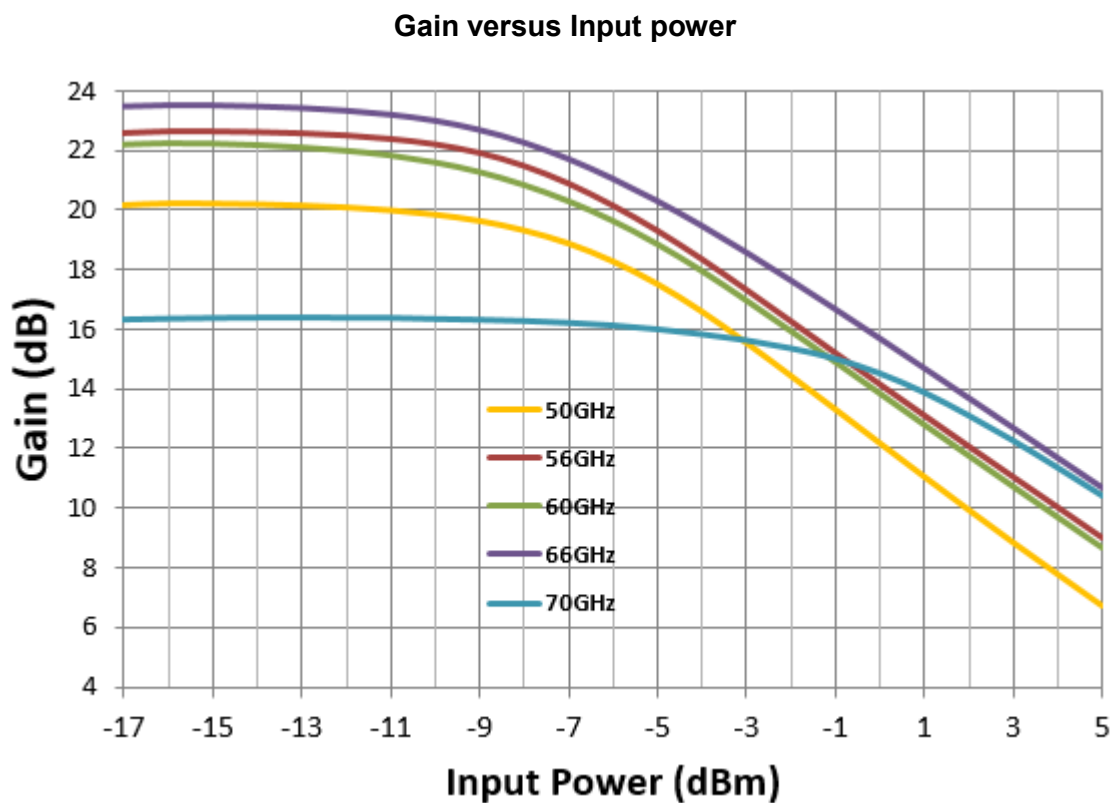
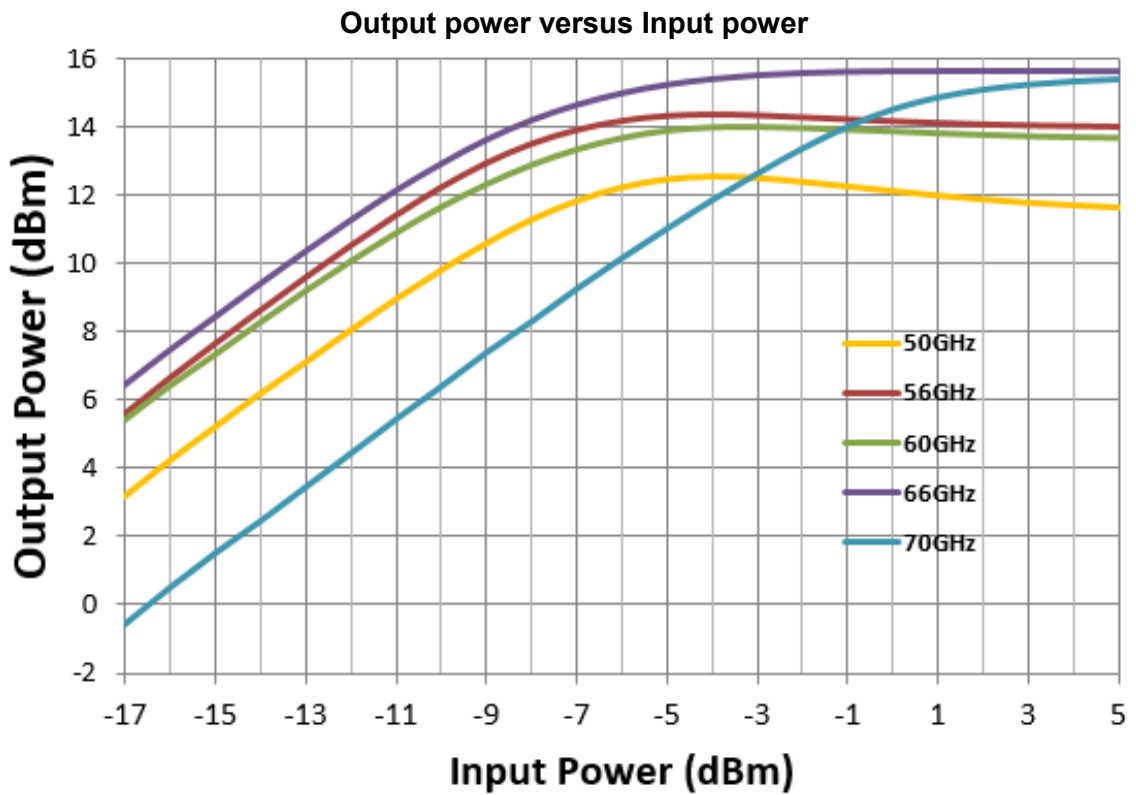
### Output return loss versus VG & Frequency



**Typical on board Measurements**

Tcase= +25°C, Vd = +3.3V, Id = 75mA, Typical

Losses due to board are de-embedded. Measurements are given in the die access plan.

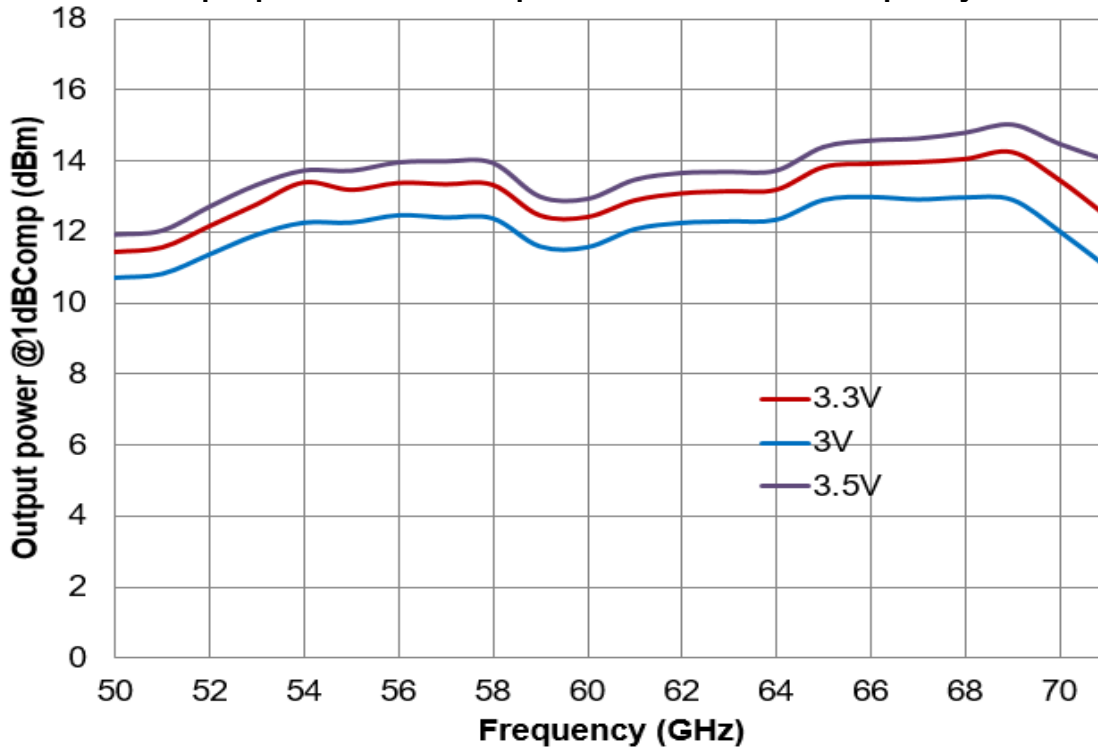


## Typical on board Measurements

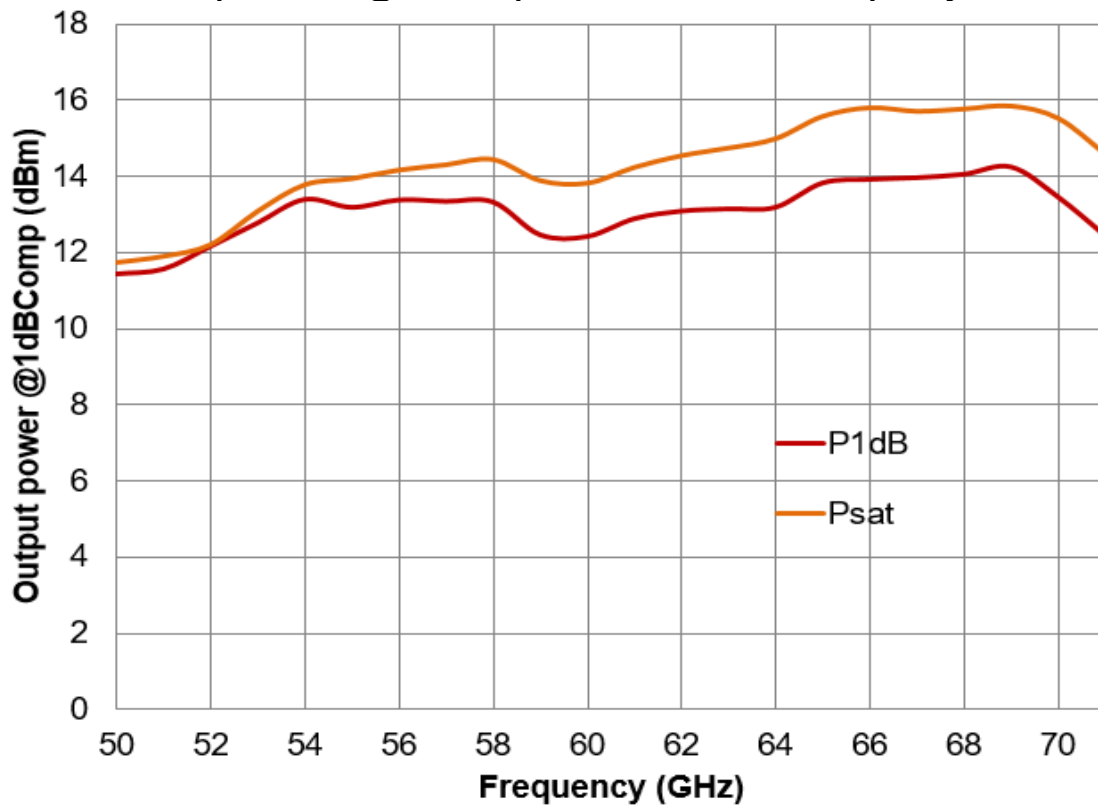
T<sub>case</sub> = +25°C, V<sub>d</sub> = +3.3V, I<sub>d</sub> = 75mA, Typical

Losses due to board are de-embedded. Measurements are given in the die access plan.

Output power at 1 dB compression versus VD & Frequency



Output Power @1dBComp & saturated versus Frequency



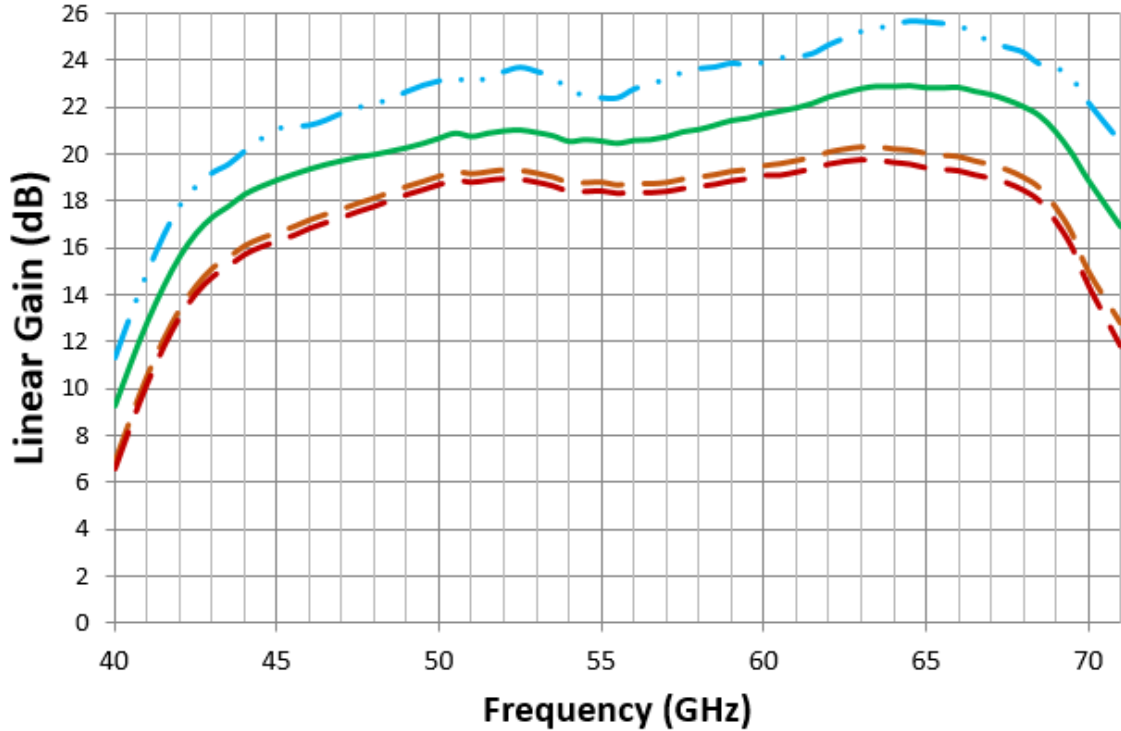
**Typical on board Measurements**

Tcase= +25°C, Vd = +3.3V, Id = 75mA, Typical

Losses due to board are de-embedded. Measurements are given in the die access plan.

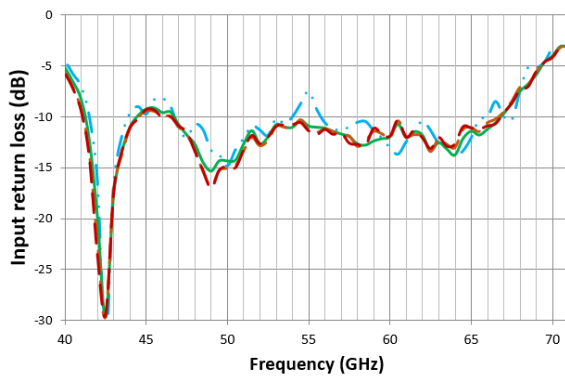
**Linear Gain versus Frequency & Temperature**

Tcase: -40°C 25°C 85°C 95°C



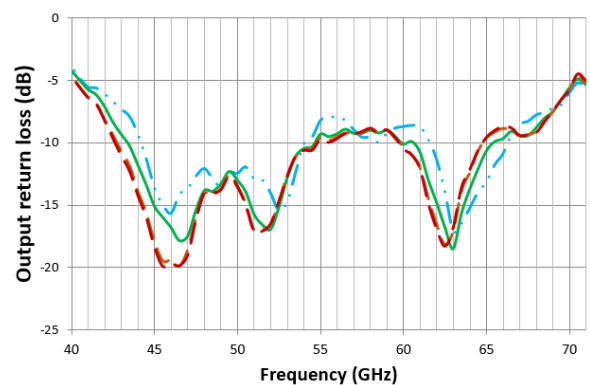
**Input return loss versus Frequency & Temperature**

Tcase: -40°C 25°C 85°C 95°C



**Output return loss versus Frequency & Temperature**

Tcase: -40°C 25°C 85°C 95°C



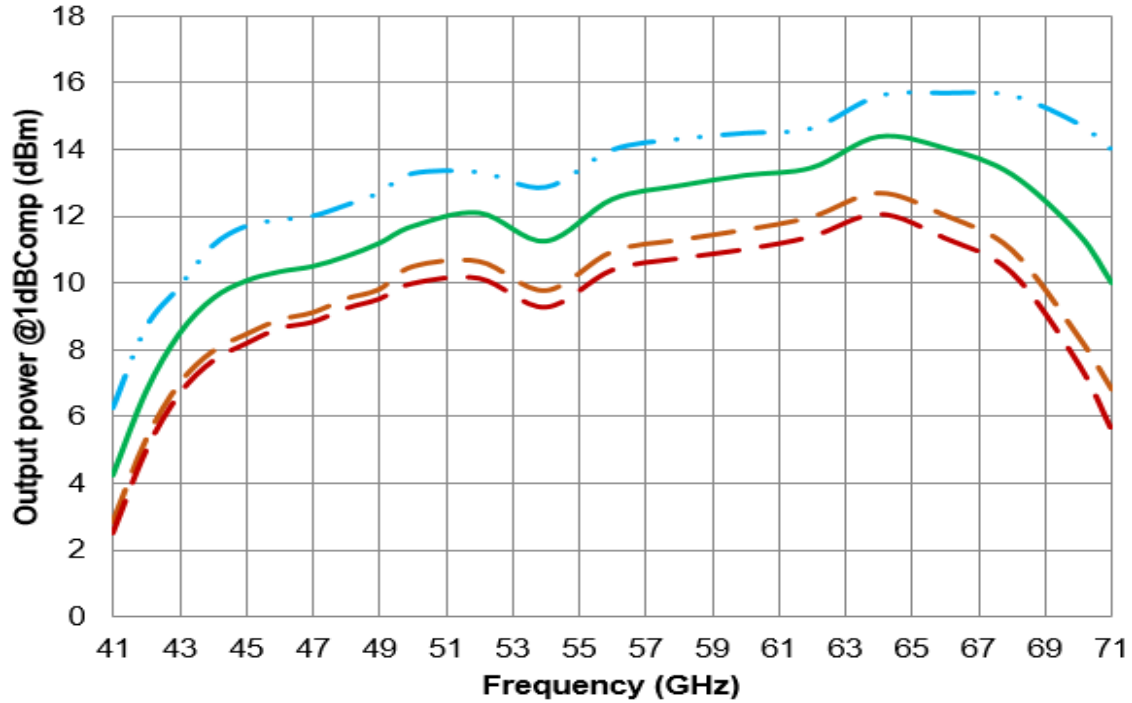
## Typical on board Measurements

Tcase= +25°C, Vd = +3.3V, Id = 75mA, Typical

Losses due to board are de-embedded. Measurements are given in the die access plan.

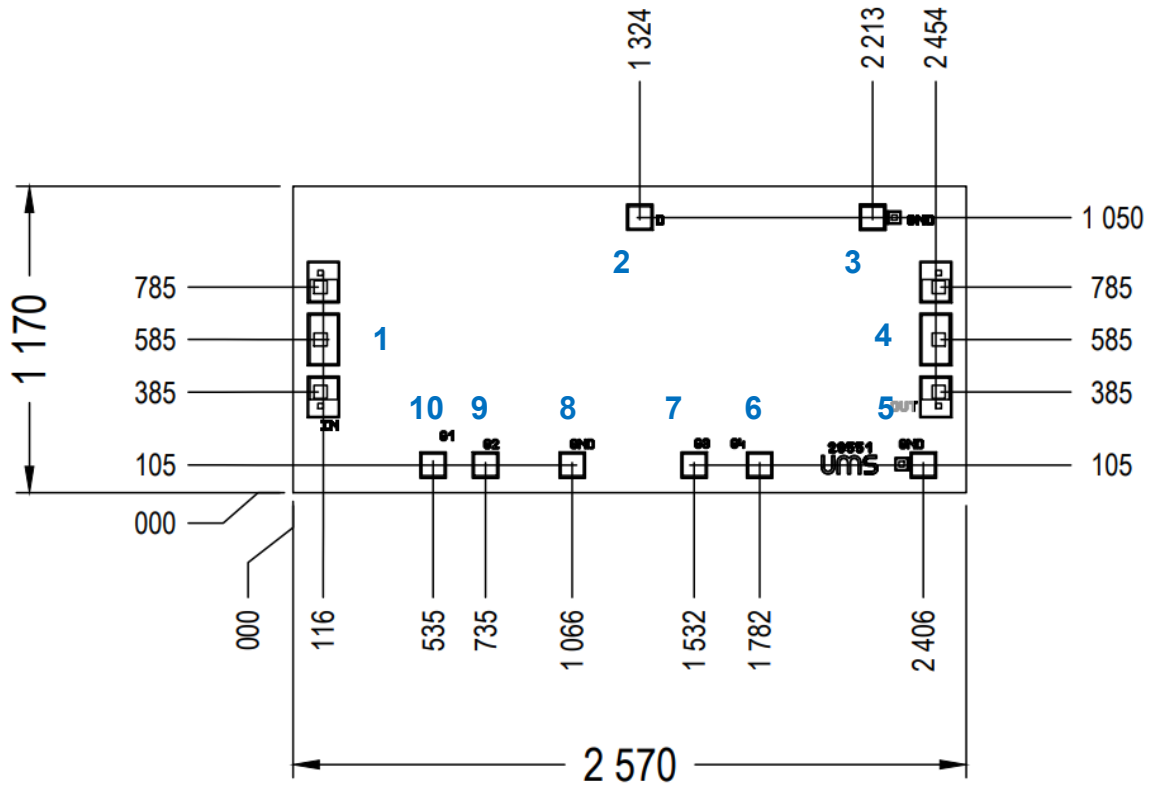
### Output power at 1 dB compression versus Frequency & Temperature

Tcase: -40°C 25°C 85°C 95°C



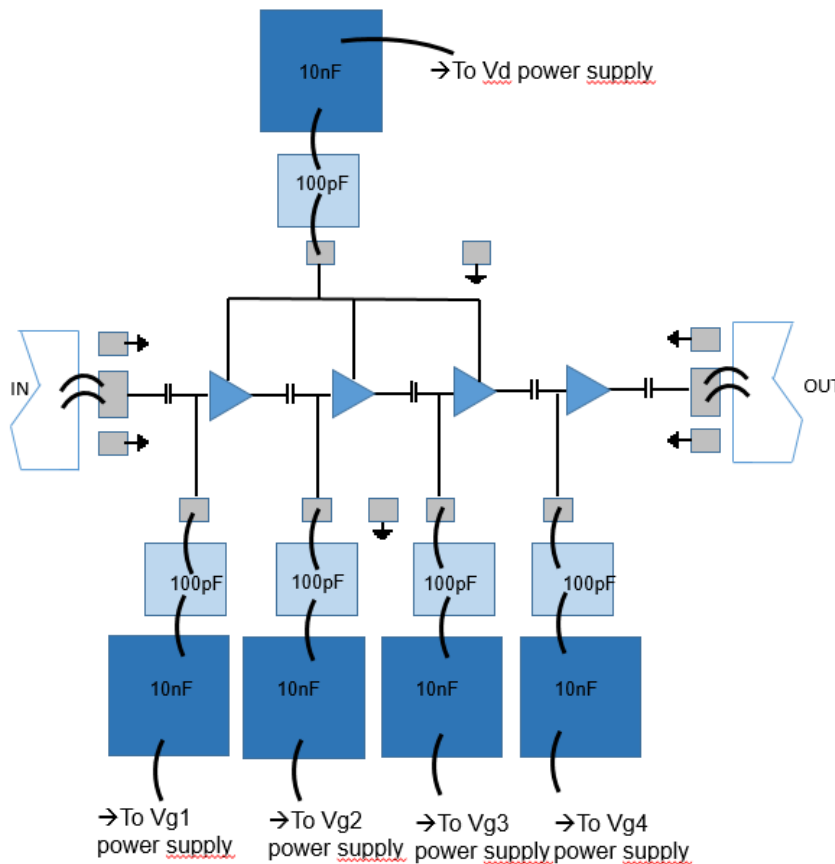
**Mechanical data**

Chip thickness: 70µm.  
 Chip size: 2570µm/1170µm ±35µm  
 All dimensions are in micrometers



PAD Number	Name	Description	Pad size (BCB Opening)
1	RF IN	Input RF port	186µm x 105µm
2	D	DC Drain voltage all stages	86µm x 83µm
10	G1	DC Gate voltage 1 <sup>st</sup> stage	86µm x 83µm
9	G2	DC Gate voltage 2 <sup>nd</sup> stage	86µm x 83µm
7	G3	DC Gate voltage 3 <sup>rd</sup> stage	86µm x 83µm
6	G4	DC Gate voltage 4 <sup>th</sup> stage	86µm x 83µm
3,5,8	GND	Ground not connected	86µm x 83µm
4	RF OUT	Output RF port	186µm x 105µm

## Recommended assembly plan



Note: Supply feed should be bypassed. 25µm diameter gold wire is to be preferred.

Connection RF accesses: Circuits having to be as close as possible to each other, the ribbon length (75µm wide) must be reduced to the achievable minimum (160µm gap between two chips is considered) and the loop height must be the smallest realizable (80µm).

A second solution is the use of double wires (Ø 25µm), wedge bonded. In this case, a minimum of two wires and the same chip-to-chip distance than ribbon solution are necessary to reduce the inductance effect. Nevertheless, simulations have demonstrated an improvement of RF performance for Q-band frequency range with the use of ribbon connection instead of wire.

2 levels of decoupling capacitor have been used:

First level of capacitor is 100pF, second level is 10nF. First level of capacitors decoupling must be close to the chip.

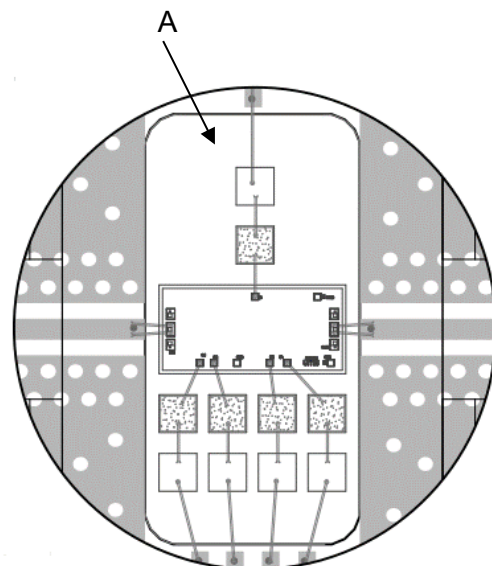
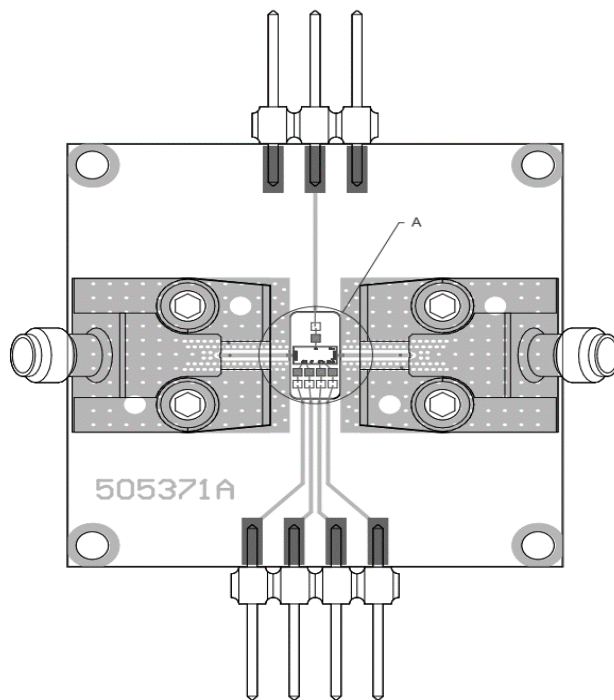
## Recommended circuit bonding table

Label	Type	Decoupling	Comment
IN / OUT	RF access	Not required	as close as possible to the circuit
D	Vd	100pF/ 10nF	Drain Supply: 100pF as close as possible to the circuit
G1/G2/G3	Vg	100pF/ 10nF	Gate Supply: 100pF as close as possible to the circuit



### Evaluation mother board

- Based on typically RO4003™ / 8mils or equivalent.
- Decoupling capacitors of 100pF and 10nF ±10% are recommended for all DC accesses.
- Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.



### Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.

ESD protections are also implemented on gate and control accesses.

The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling on the PC board, as close as possible to the package.

**Notes**

## Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations for the UMS products.

## Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <https://www.ums-rf.com>.

## Recommended reflow process assembly

Refer to the application note AN0001 available at <https://www.ums-rf.com> for die attach.

## Ordering Information

Chip form:

CHA2368-98F/00

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