United Monolithic Semiconductors

CHA4220-98F

0.5-20GHz Driver

GaAs Monolithic Microwave IC

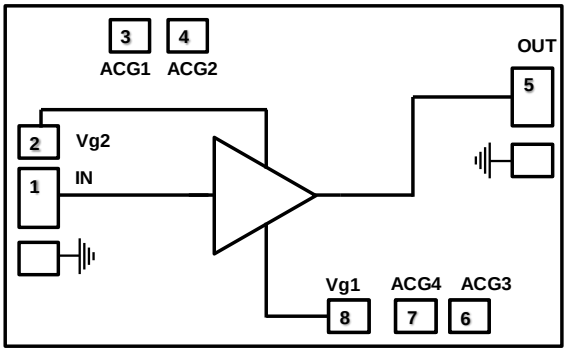
Description

The CHA4220-98F is a distributed driver amplifier which operates between 0.5 and 20GHz.

It is designed for a wide range of applications, such as military, telecom, test instrumentation.

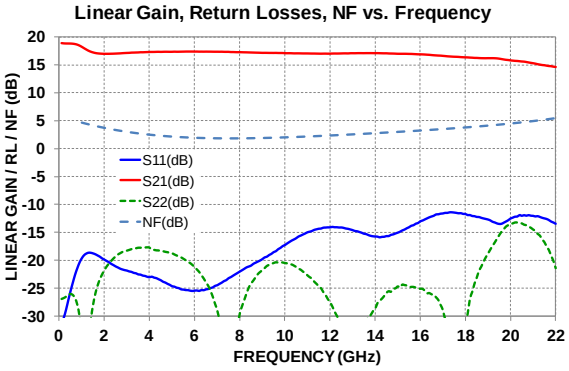
The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is supplied as bare die part with RF accesses matched on 50 ohms.



Main Features

- Broadband performances: 0.5-20GHz
- Typical Linear Gain: 17dB
- OP1dB: 20dBm
- Psat: 23dBm
- OIP3: 28dBm
- Typical Noise Figure: 3.5dB
- DC bias: Vd=7V@Id=120mA, Vg1#-0.2V and Vg2=1.5V.
- Bare die
- Die size: 3.04 x 1.56 x 0.1mm



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	0.5		20	GHz
Gain	Linear Gain		17		dB
NF	Noise Figure		3.5		dB
Pout	Output Power @1dB comp.		20		dBm

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Electrical Characteristics

Tamb.= +25°C,Vg1 to be set in order to have Idq=120mA, Vg2=1.5V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	0.5		20	GHz
Gain	Linear Gain		17		dB
NF	Noise Figure		3.5		dB
IRL	Input Return Loss		15		dB
ORL	Output Return Loss		18		dB
P1dB	Output power for 1dB Compression For Freq=2-20 GHz		 20		 dBm
Psat	Saturated output power For Freq=2-20 GHz		 23		 dBm
OIP3	Output Third Order Intercept For Freq=2-20 GHz		 28		 dBm
Idq	Quiescent current on Vd		120		mA
Vd	Supply voltage on Vd	6	6.5	7	V
Id	Drain current @3dB gain compression		140		mA
Pin_max	Maximum input power For Vd=6V For Vd=7V		 17 15		 dBm dBm

The values are representative of typical “test fixture” measurements as defined on the drawing in paragraph “Evaluation test fixture”.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad N°	Parameter	Values	Unit
Vg1	8	Gate control1 for the amplifier	-0.2/-0.4	V
Vg2	2	Gate control2 for the amplifier	1.5	V
Vd	5	Drain Voltage	7	V

The associated drain current with no RF input power is Idq=120mA

This typical bias is recommended in order to get the best compromise between output power, linearity and Noise Figure performance vs. Temperature.

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	8V	V
Idq	Drain bias current	170	mA
Vg1	Gate bias voltage Vg1	-2 to 0	V
Vg2	Gate bias voltage Vg2	1 to 2	V
Pin	Maximum peak input power overdrive	17	dBm
Ta	Operating temperature range (chip backside)	-40 to 85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage: these maximum ratings parameters could not be cumulated.
These are stress ratings only, and functional operation of the device at these conditions is not implied.

Maximum Junction temperature=175°C with Ta=+85°C.

Rth_equivalent =72°C/W ➔ chip's equivalent thermal resistance from channel to die bottom with Ta. = +85°C and 7V & Idq=120mA.

The Rth_equivalent is extrapolated, taking into account the full DC power and the channel temperature increase on the worst transistor.

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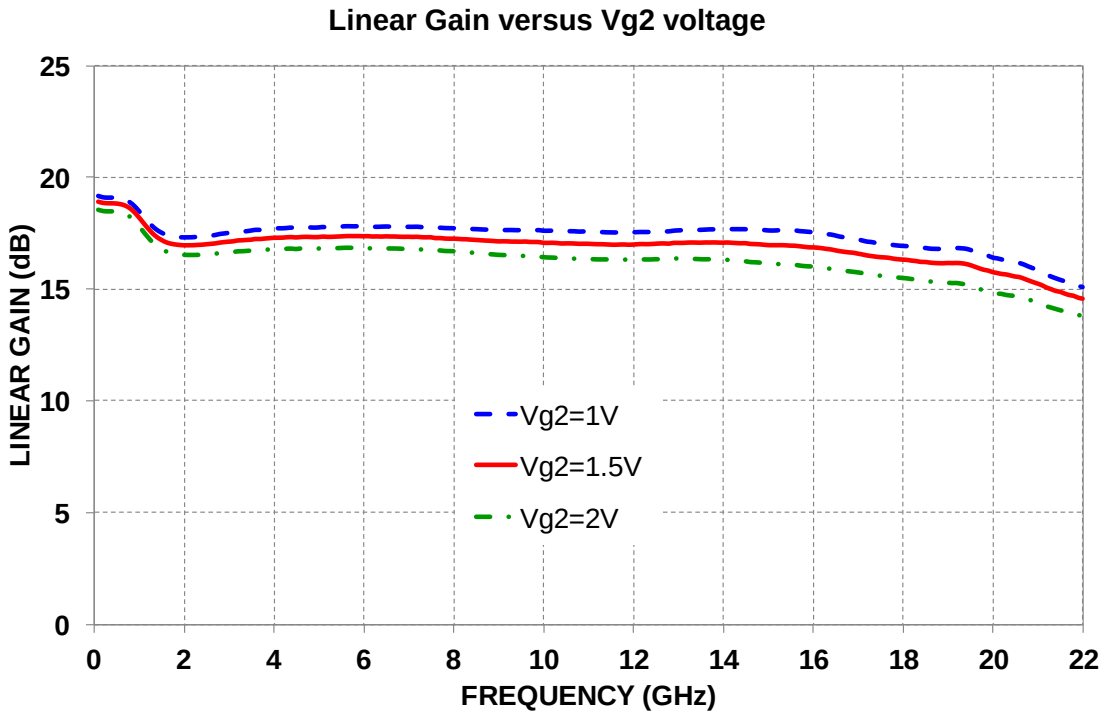
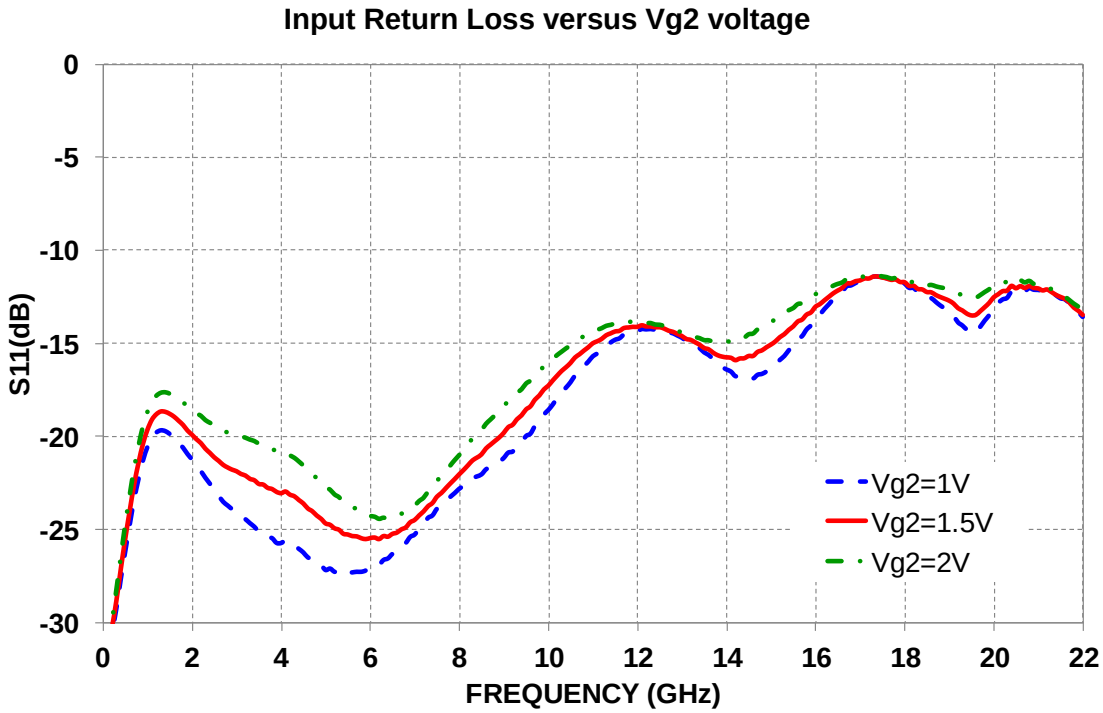
Typical Jig Measurements

Tamb.= +25°C, Vd=7V, Vg1 set in order to get Idq =120mA





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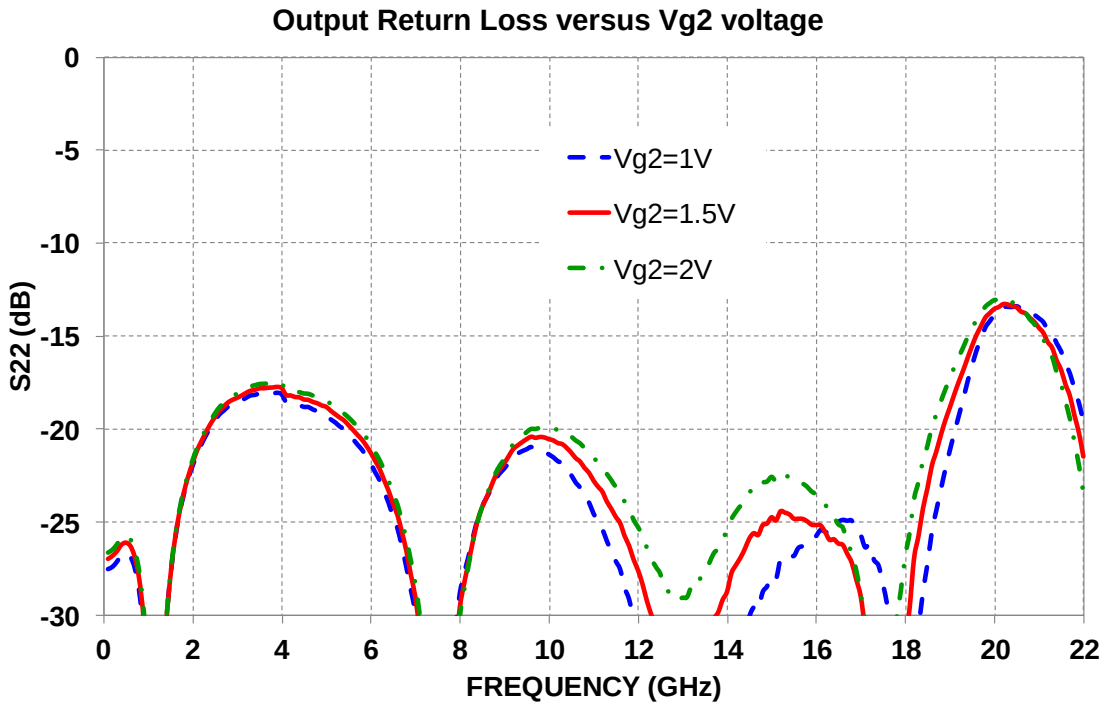
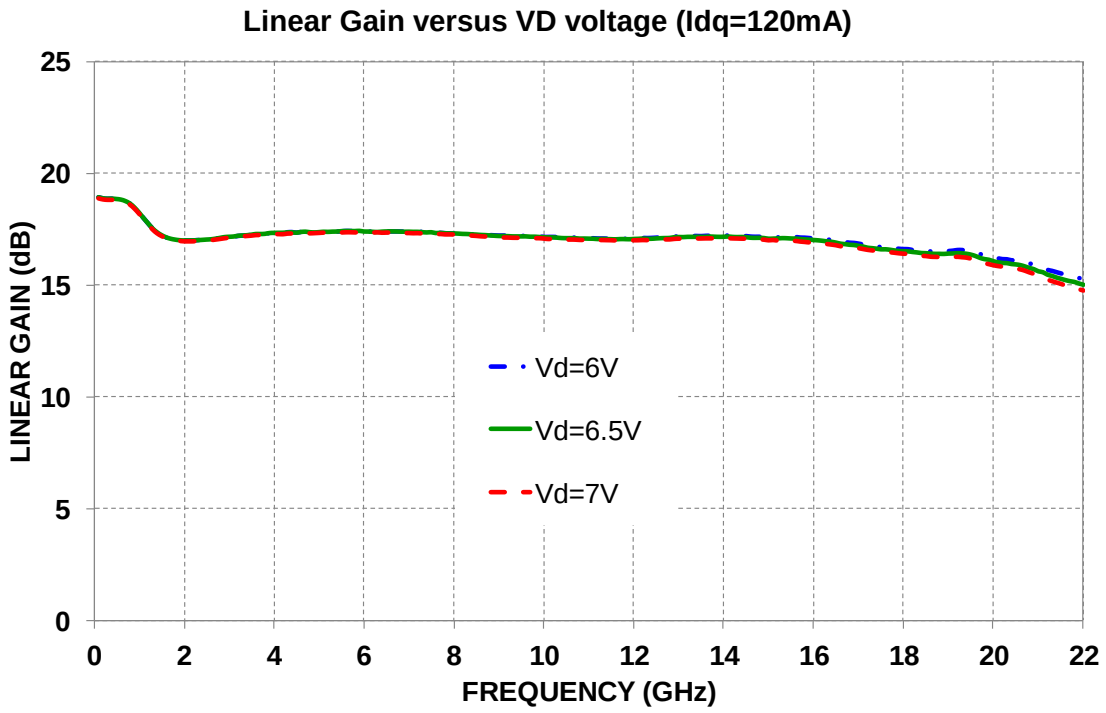
Tamb.= +25°C, Vd =7V, Vg1 set in order to get Idq =120mA





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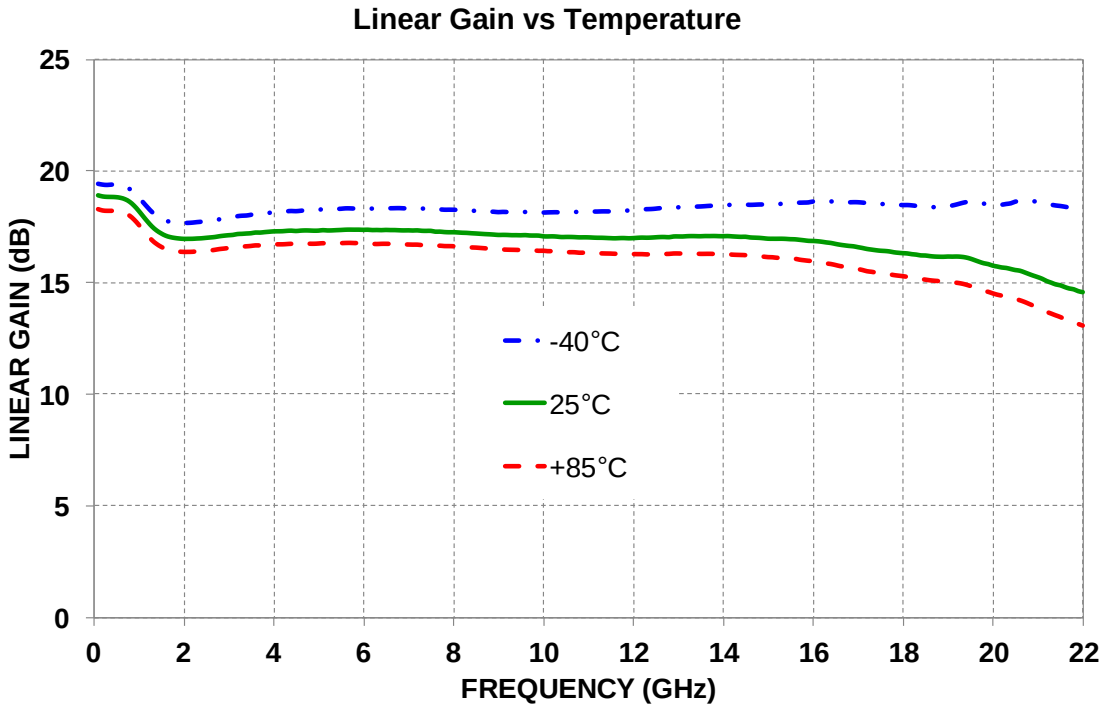
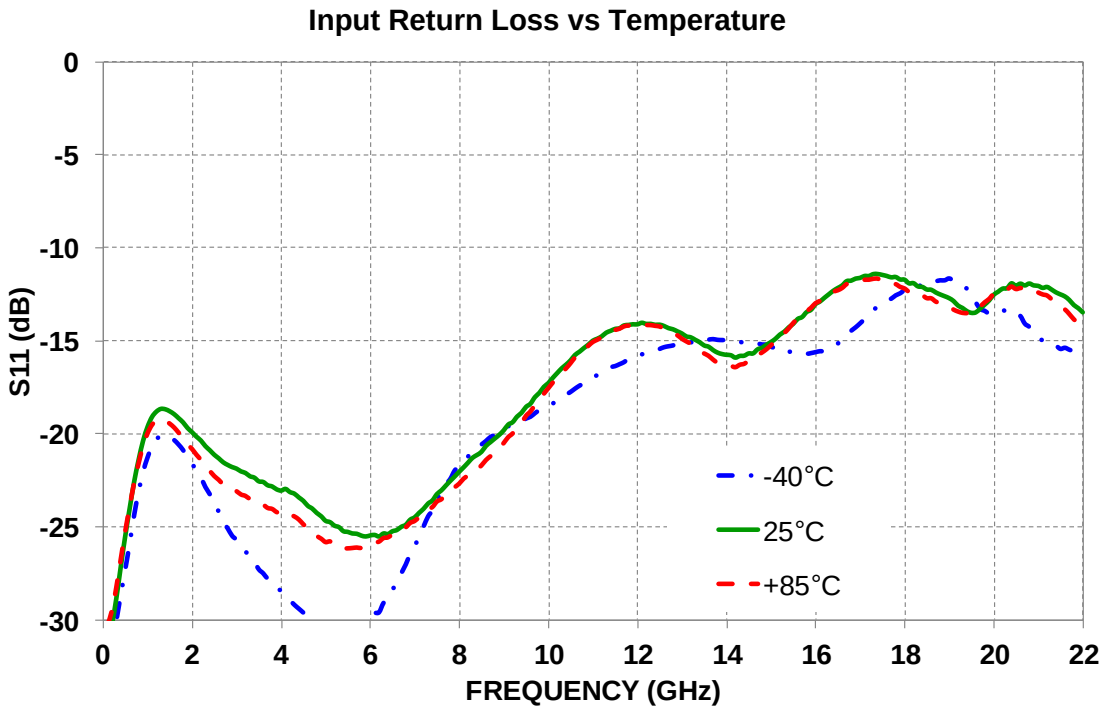
Typical Jig Measurements

Tamb.= +25°C, +85°C,-40°C, Vd =7V, Vg1 set in order to get Idq =120mA, Vg2=1.5V
Vg1 and Vg2 remain constant versus temperature.





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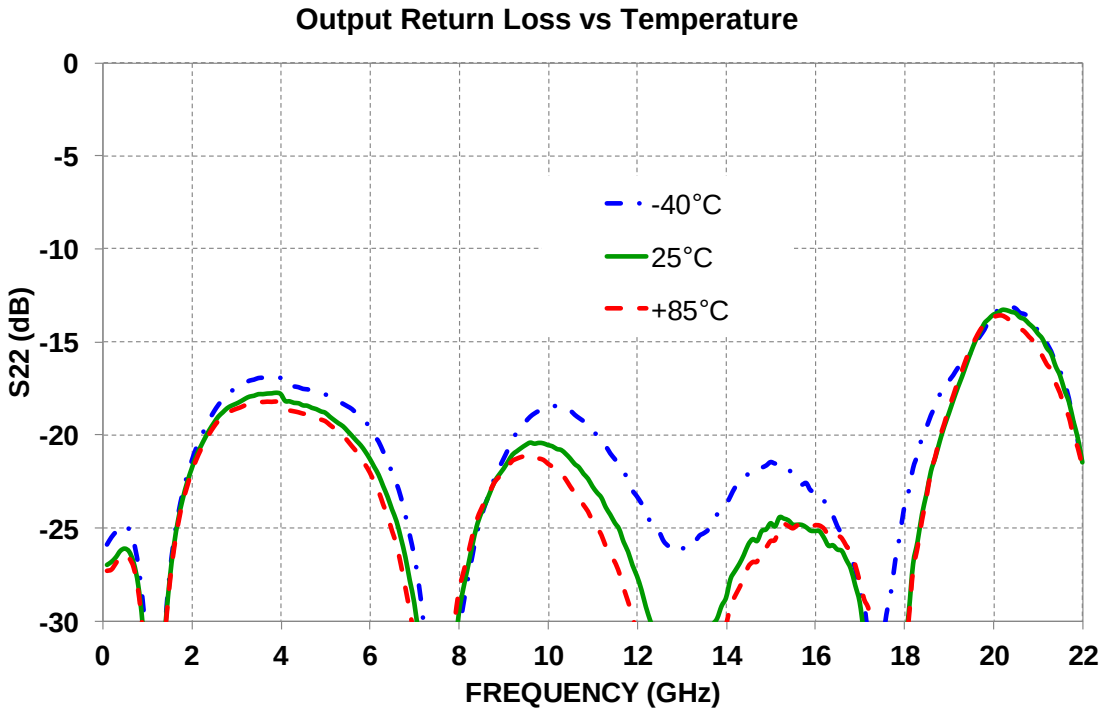
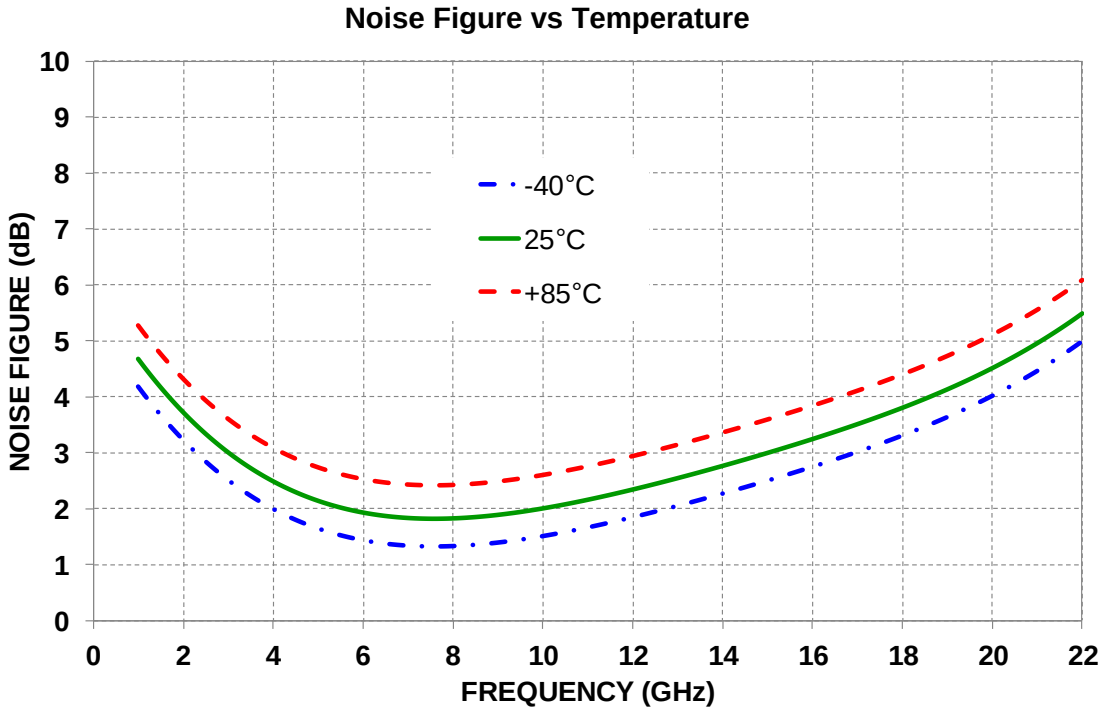
Typical Jig Measurements

Temperature.= +25°C,+85°C,-40°C, Vd =7V, Vg1 set in order to get Idq =120mA, Vg2=1.5V
Vg1 and Vg2 remain constant versus temperature.





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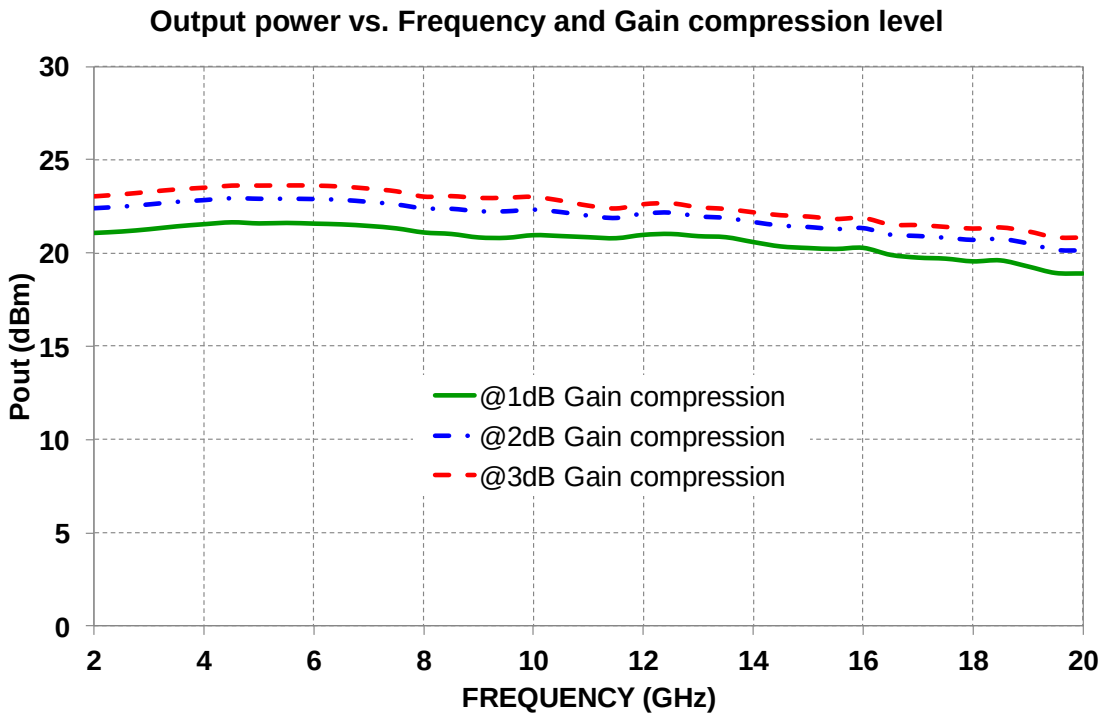

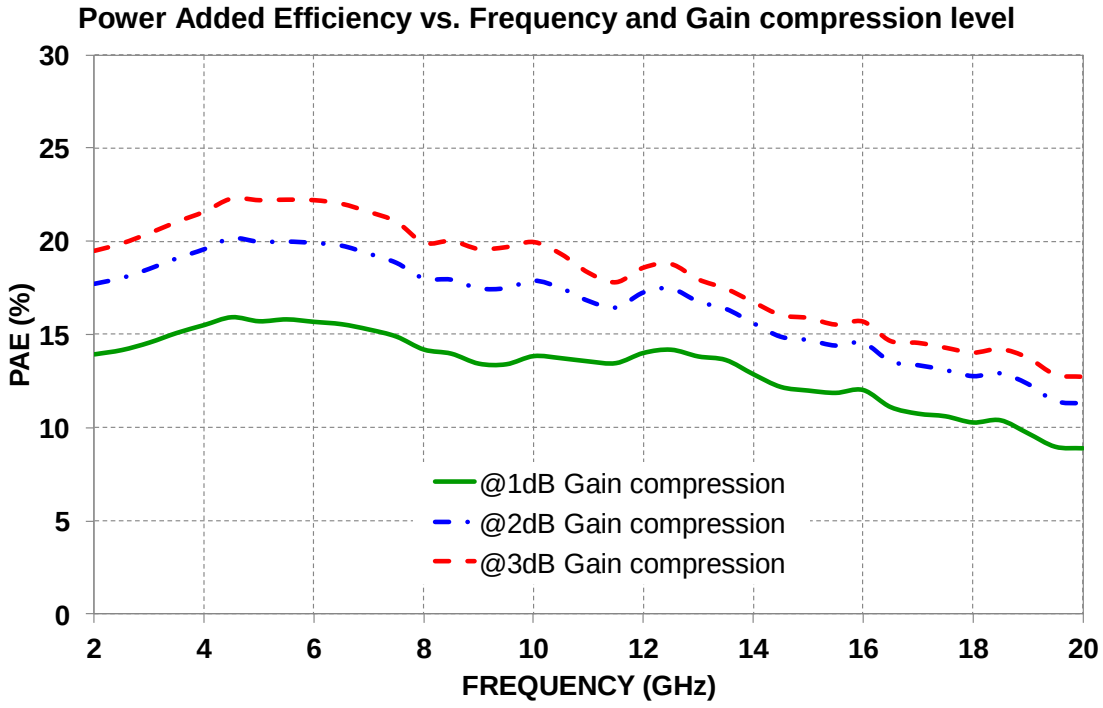

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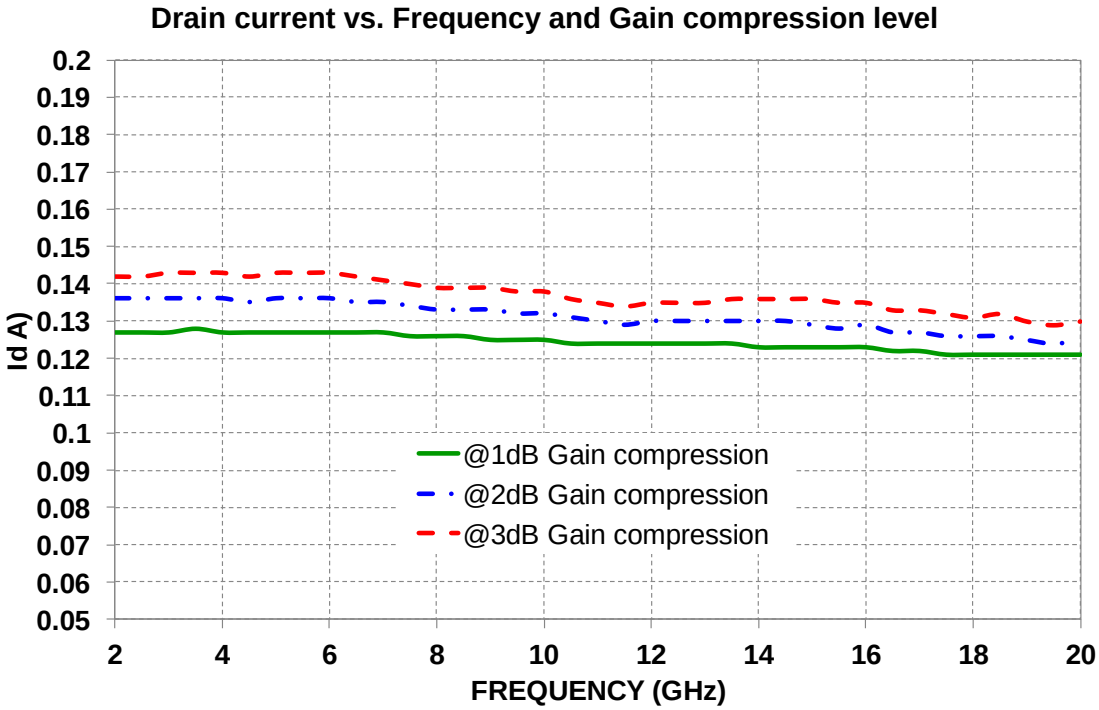

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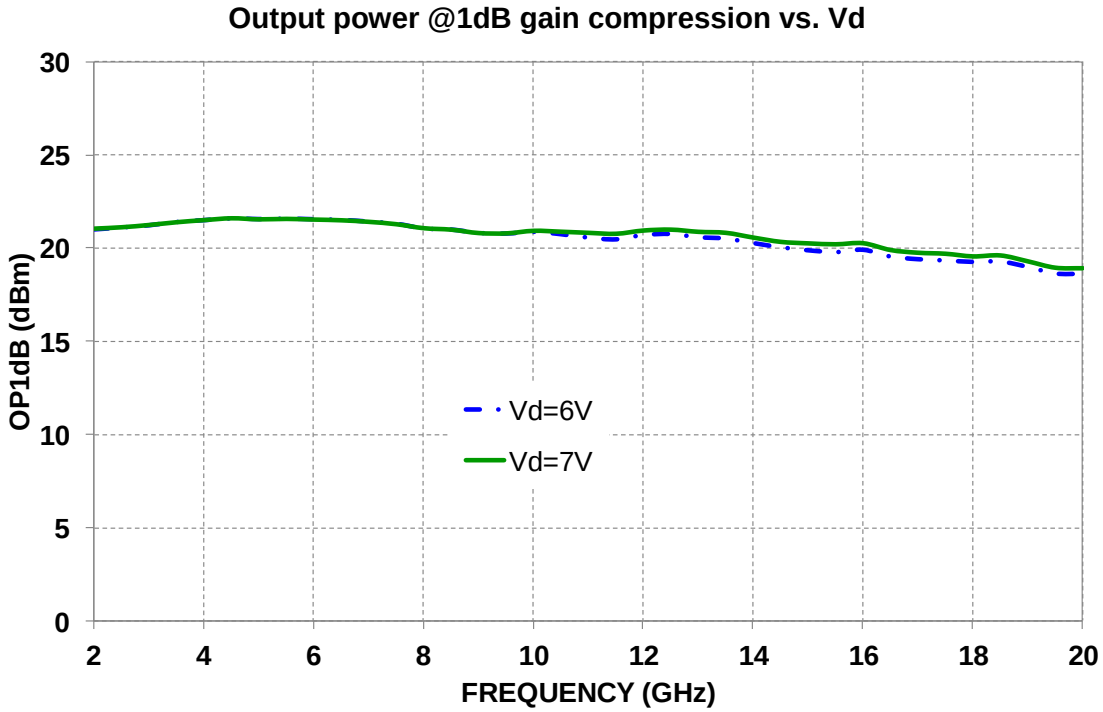
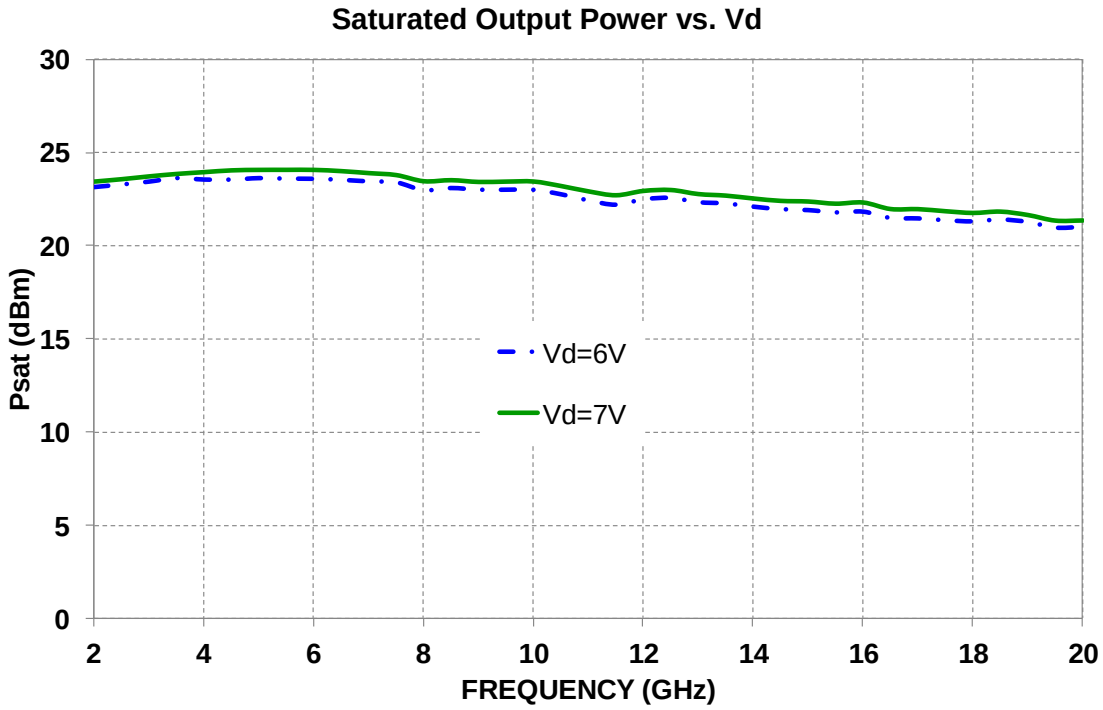
Tamb.= +25°C, Vg1 set in order to get Idq =120mA, Vg2=1.5V





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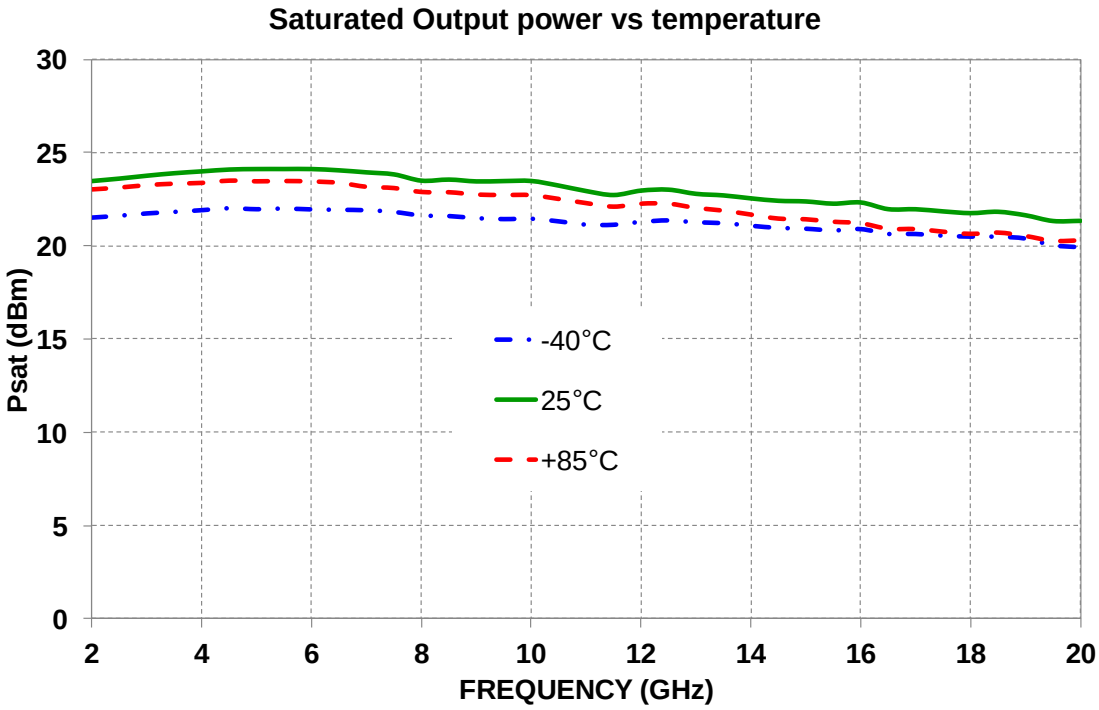
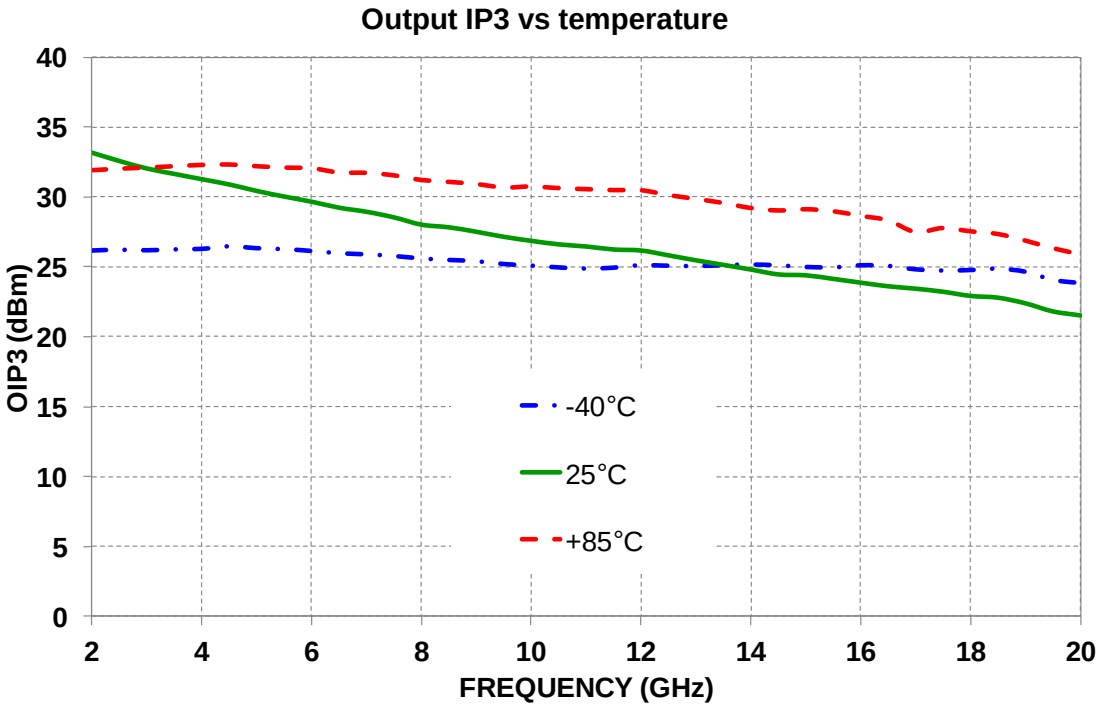
Typical Jig Measurements

Temperature.= +25°C,+85°C,-40°C, Vd =7V, Vg1 set in order to get Idq =120mA, Vg2=1.5V
Vg1 and Vg2 remain constant versus temperature.





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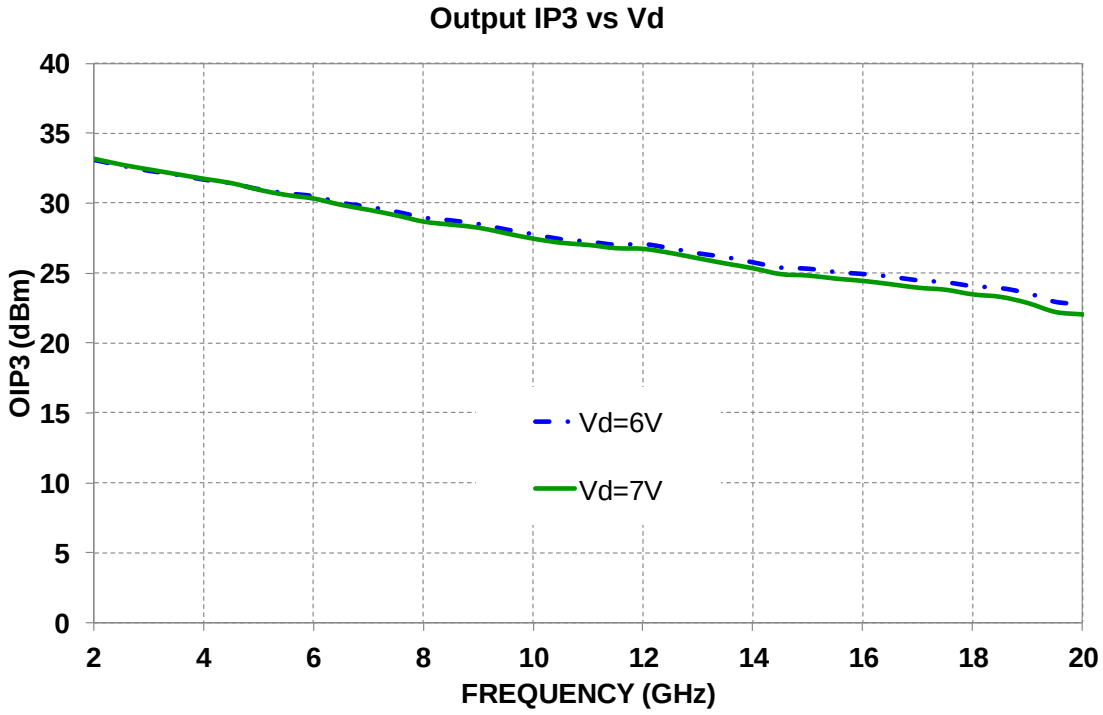
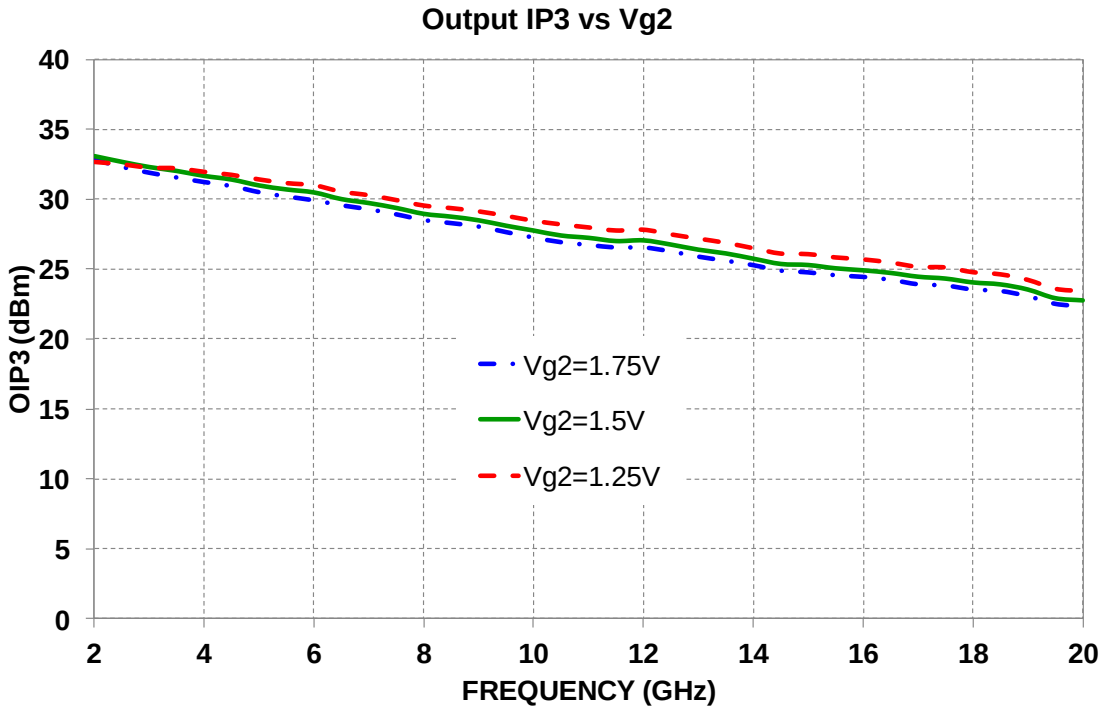


Tamb.= +25°C, Vg1 set in order to get Idq =120 mA, Vd=6V



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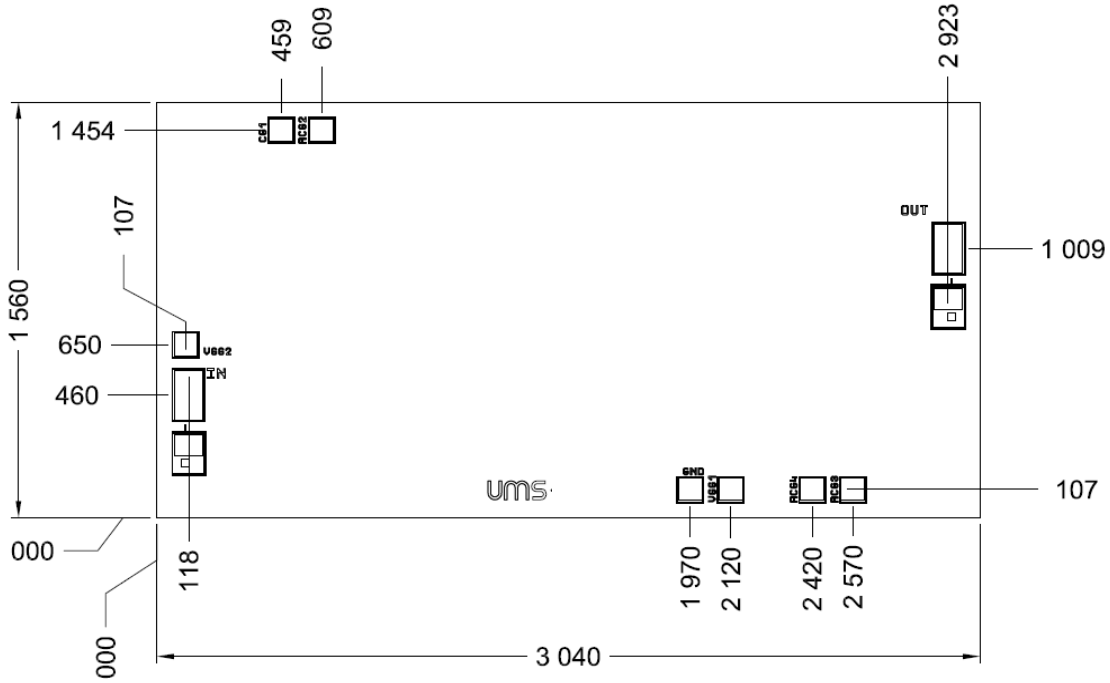
Mechanical Data: outline drawing



Chip width and length are given with a tolerance of +/- 35µm.
Chip thickness is 100µm.
All pads are 100 µm x 100 µm, except IN and OUT pads that are 200 x 120 µm.

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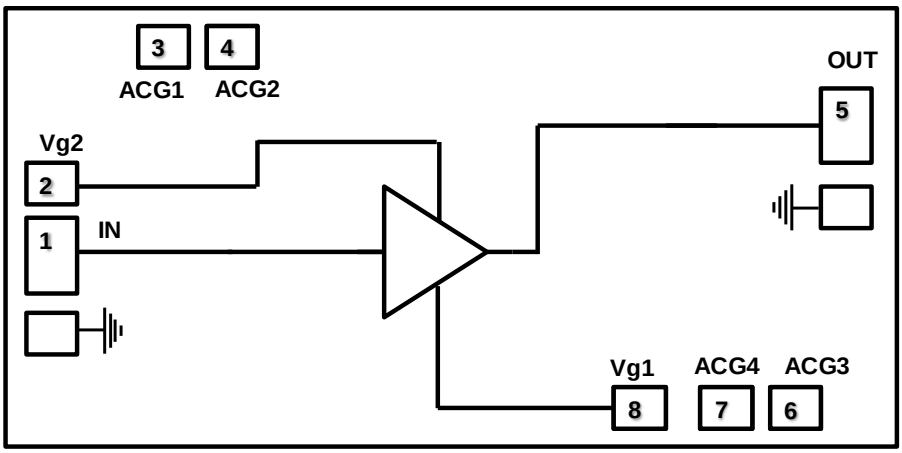
PAD Reference



PAD Number	Name	Description
1	IN	RFIN is DC coupled and matched to 50 ohms
2	Vg2	Gate control 2 for amplifier: +1.5V should be applied for nominal operation.
3	ACG1	Low frequency termination (bypass capacitor see value next page).
4	ACG2	Low frequency termination (bypass capacitor see value next page).
5	OUT & VD	RFOUT for amplifier (matched on 50 ohms). Vd voltage should be applied on this pad through a bias Tee
6	ACG3	Low frequency termination (bypass capacitor see value next page).
7	ACG4	Low frequency termination (bypass capacitor see value next page).
8	Vg1	Gate control 2 for amplifier: about -0.2V
Die bottom	GND	Die bottom must be connected to RF/DC ground

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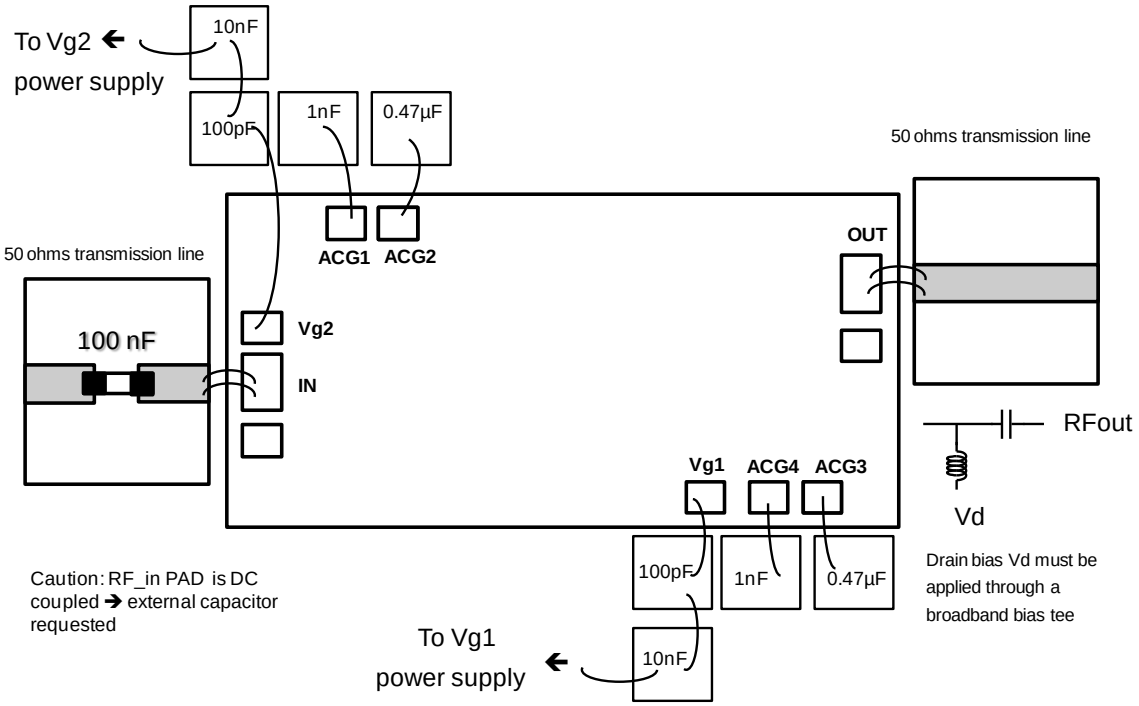
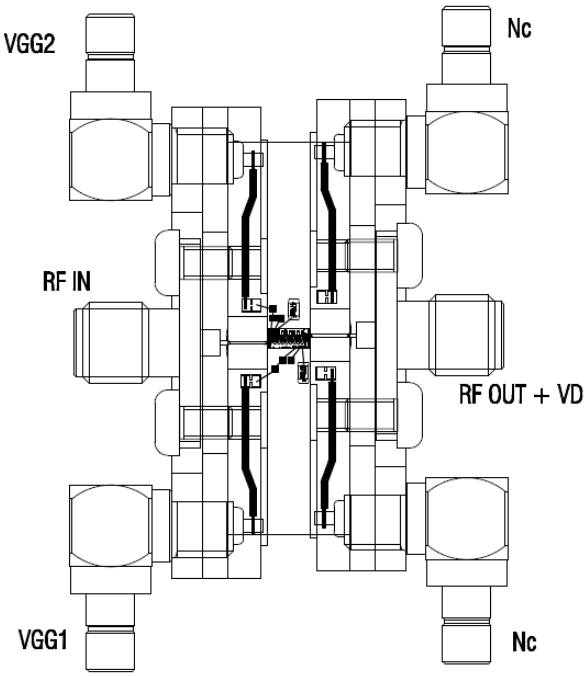
Assembly Recommendations



Evaluation test fixture



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Device Operation

Device Power Up instructions:

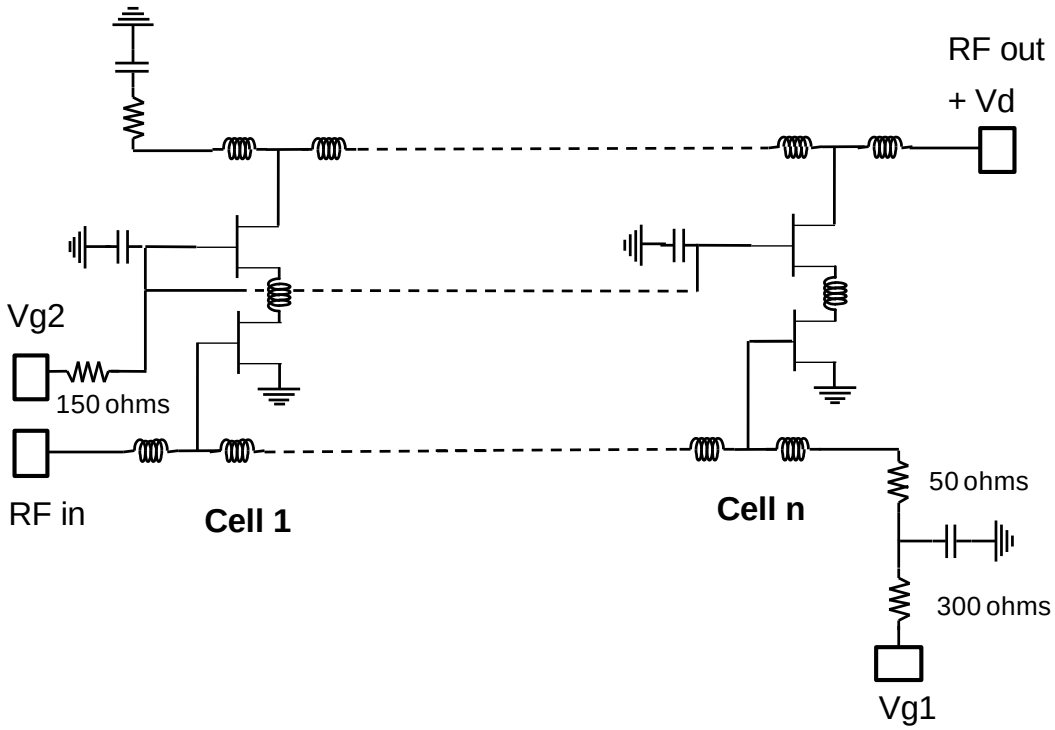
1) Ground the device
2) Set Vg1 to -2V
3) Set Vg2 to 1.5V (nominal value for Vg2)
4) Set Vd to 7V (nominal value for Vd)
5) Set Vg1 in the range of -0.2V for having Idq=120mA
6) Apply RF input power

Device Power Down instructions:

1) Remove RF input power
2) Remove Vd
3) Remove Vg2
4) Remove Vg1

DC Schematic

Vd=7V, Vg1=-0.2V, Vg2=1.5V, Idq=120mA



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Notes

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Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

Chip form:	CHA4220-98F/00

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