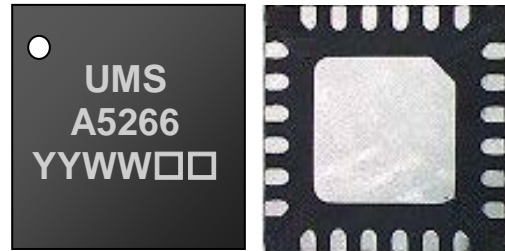


10-16GHz Medium Power Amplifier

GaAs Monolithic Microwave IC in SMD leadless package

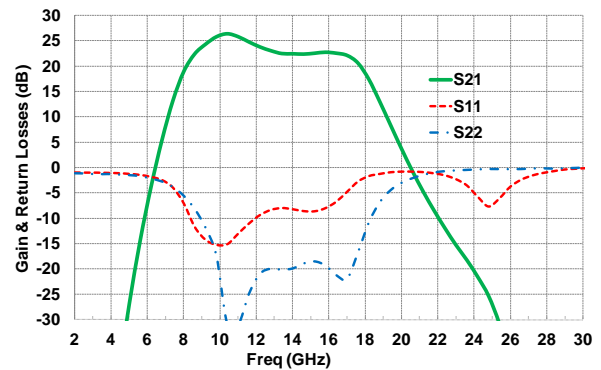
Description

The CHA5266-QDG is a three stage monolithic GaAs medium power amplifier. It is designed for a wide range of applications, from professional to commercial communication systems. The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography. It is supplied in RoHS compliant SMD package.



Main Features

- Broadband performances: 10-16GHz
- 23dB Linear Gain
- 25.5dBm output power @ 1dB comp.
- 35dBm output IP3
- DC bias: Vd=5.0Volt@Id=320mA
- 24L-QFN4x4
- MSL1



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	10		16	GHz
Gain	Linear Gain 10-12 GHz		25		dB
	Linear Gain 12.5-16 GHz		22		dB
OIP3	Output TOI		35		dBm
Pout	Output Power @1dB comp.		25.5		dBm

Specifications

Tamb.= +25°C, Vd = +5.0V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	10		16	GHz
Gain	Linear Gain 10-12 GHz		25		dB
	Linear Gain 12.5-16 GHz		22		dB
RL_in	Input Return Loss		9		dB
RL_out	Output Return Loss		20		dB
P1dB	Output power @ 1dB compression		25.5		dBm
Psat	Saturated output power		27		dBm
OIP3	Output IP3		35		dBm
NF	Noise Figure		6		dB
Idq	Quiescent Drain current		320		mA
Vg	Gate Voltage		-0.35		V

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

“Power ON” sequence

1. Ground the device
2. Bias MPA gate voltage at Vg low enough (Typically: Vg ≈ -2V)
3. Apply Vds bias voltage (Typically: Vd = 5V)
4. Increase slowly Vgs up to quiescent bias drain current Idq
5. Apply RF signal

“Power OFF” sequence

1. Turn off RF signal
2. Bias MPA gate voltage at Vg low enough (Typically: Vg ≈ -2V)
3. Turn Vds bias voltage to 0V
4. Turn Vgs bias voltage to 0V

Absolute Maximum Ratings ⁽¹⁾T_{amb.} = +25°C

Symbol	Parameter	Values	Unit
V _d	Drain bias voltage	7.0V	V
I _{dq}	Drain bias current	0.45	A
V _g	Gate bias voltage	-2 to 0	V
V _{dg}	External drain-gate excursion	8	V
P _{in}	Input continuous power	20	dBm
T _j	Maximum Junction temperature ⁽²⁾	175	°C

⁽¹⁾ Operation of this device above anyone of these parameters may cause permanent damage.

⁽²⁾ Thermal Resistance channel to ground paddle

Recommended Operating Range ^{(3), (4)}

Symbol	Parameter	Values	Unit
V _d	Drain bias voltage	4 to 6	V
I _d	Drain bias current	280 to 360	mA
V _g	Gate bias voltage	-2 to 0	V
P _{in}	Maximum peak input power overdrive	10	dBm

Temperature Range

T _a	Operating temperature range	-40 to +95	°C
T _{stg}	Storage temperature range	-55 to +150	°C

Typical Bias ConditionsT_{amb.} = +25°C

Symbol	Pad N°	Parameter	Values	Unit
VD1	22	DC Drain voltage 1 st stage	5	V
VD2	21	DC Drain voltage 2nd stage	5	V
VD3	20	DC Drain voltage 3rd stage	5	V
VG1	9	DC Gate voltage 1 st stage	-0.35	V
VG2	10	DC Gate voltage 2nd stage	-0.35	V
VG3	11	DC Gate voltage 3rd stage	-0.35	V

Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is only cooled down by conduction through the package thermal pad (no convection mode considered).

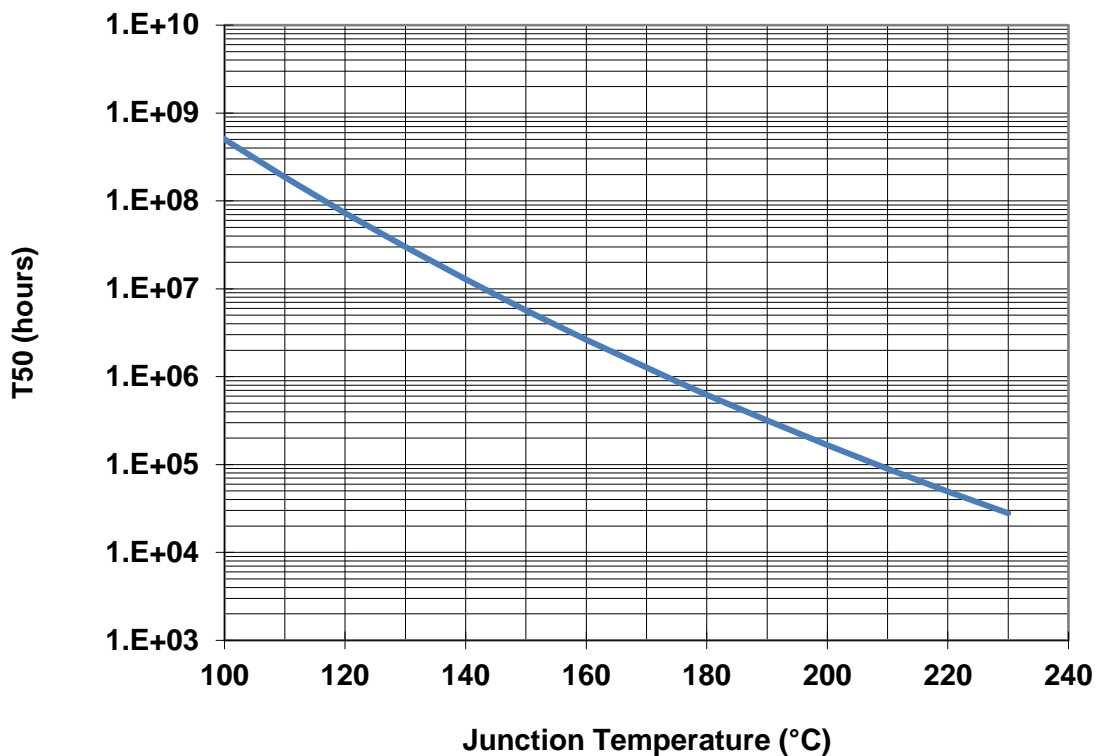
The temperature is monitored at the package back-side interface (Tcase).

The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Absolute Maximum Ratings table.

So, the system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	Tjunction (°C)	RTH (°C/W)	T50 (hours)
RTH ⁽¹⁾ Thermal Resistance (Junction to Case)	Vd= 5V Id= 320mA Pdiss= 1.6W	168	45.7	1.46E+06

¹ Assuming 95°C Tcase



Typical Package Sij parameters

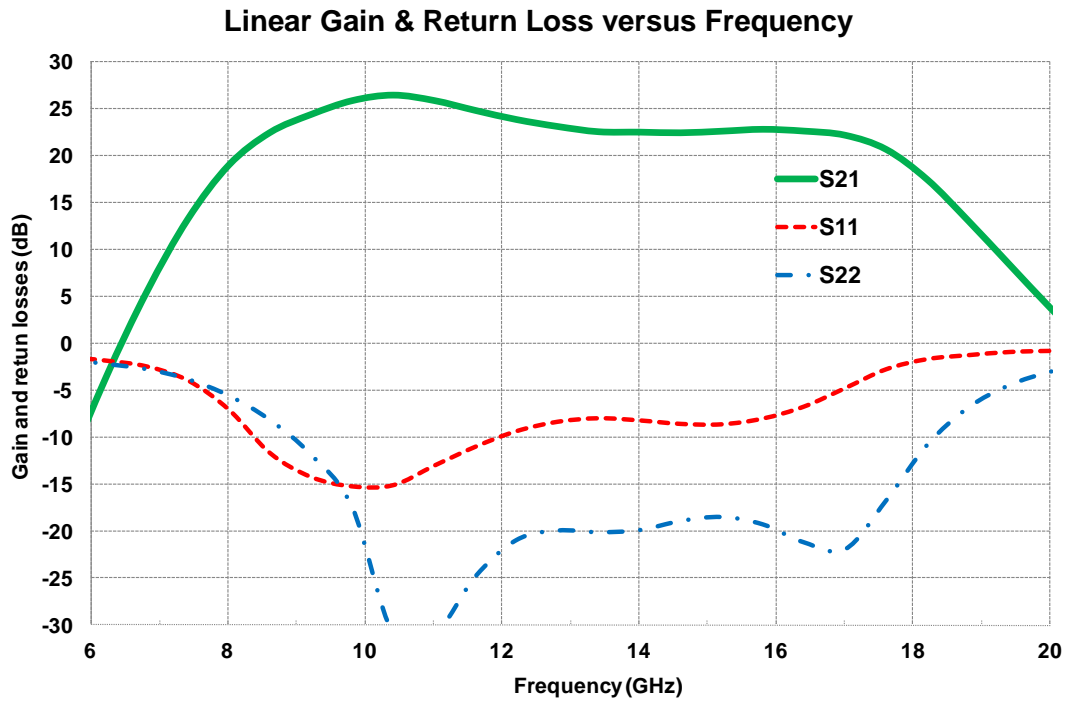
Tamb.= +25°C, Vd = +5.0V, Id = 320mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
2.0	-1.0	89.8	-70.1	-0.2	-47.8	-95.8	-1.2	101.2
3.0	-1.0	51.5	-74.3	-57.4	-53.4	-76.1	-1.3	61.5
4.0	-1.1	17.5	-87.0	158.2	-48.7	-2.8	-1.4	19.4
5.0	-1.3	-14.5	-71.8	59.1	-26.8	36.5	-1.5	-26.0
6.0	-1.7	-47.2	-70.0	34.9	-7.0	-17.1	-2.0	-76.0
7.0	-2.9	-84.8	-88.0	29.0	8.2	-104.4	-3.2	-130.4
8.0	-7.1	-127.2	-67.4	119.0	19.0	143.9	-5.6	170.8
9.0	-13.7	-137.8	-67.0	58.7	23.8	29.5	-10.5	111.2
10.0	-15.9	179.3	-59.0	64.1	26.3	-73.9	-20.2	63.1
11.0	-13.1	62.9	-54.7	15.1	25.8	-173.6	-31.0	83.3
12.0	-9.9	6.0	-53.8	-46.7	24.1	105.1	-22.0	45.2
13.0	-8.2	-29.4	-55.2	-95.7	22.8	33.9	-19.8	7.8
14.0	-8.2	-54.8	-54.7	-123.1	22.5	-33.8	-19.9	-8.1
15.0	-8.8	-61.5	-49.9	-172.8	22.5	-104.8	-18.6	-24.1
16.0	-7.8	-60.0	-49.2	142.0	22.7	175.7	-20.2	-58.8
17.0	-4.8	-62.1	-51.2	83.2	22.2	86.9	-22.0	-99.5
18.0	-2.0	-80.8	-57.9	90.2	18.7	-14.1	-12.7	164.0
19.0	-1.2	-100.0	-53.3	104.5	11.5	-101.4	-5.9	94.3
20.0	-0.8	-117.9	-51.5	84.6	3.7	-170.3	-3.1	48.4
21.0	-0.9	-135.5	-51.5	52.5	-3.4	132.3	-1.7	15.2
22.0	-1.3	-155.6	-50.0	62.1	-9.7	80.7	-0.9	-11.8
23.0	-2.3	177.2	-51.0	91.9	-15.2	30.8	-0.6	-35.1
24.0	-4.8	128.3	-47.4	77.0	-20.4	-24.8	-0.4	-55.0
25.0	-7.5	25.1	-49.4	32.8	-26.5	-90.3	-0.3	-73.3
26.0	-3.8	-60.1	-42.6	55.5	-38.3	-174.0	-0.4	-89.9
27.0	-1.7	-101.1	-41.9	43.2	-40.6	89.3	-0.3	-104.8
28.0	-0.9	-128.0	-41.8	23.3	-41.2	45.3	-0.2	-119.4
29.0	-0.4	-150.1	-38.7	5.8	-38.0	11.0	-0.2	-132.0
30.0	-0.2	-168.4	-39.4	-25.9	-38.8	-24.6	0.0	-143.3

Typical Board Measurements

Tamb.= +25°C, Vd = +5.0V, Id = 320mA

Measurement in the QFN planes as defined in paragraph "Definition of the Sij reference planes"

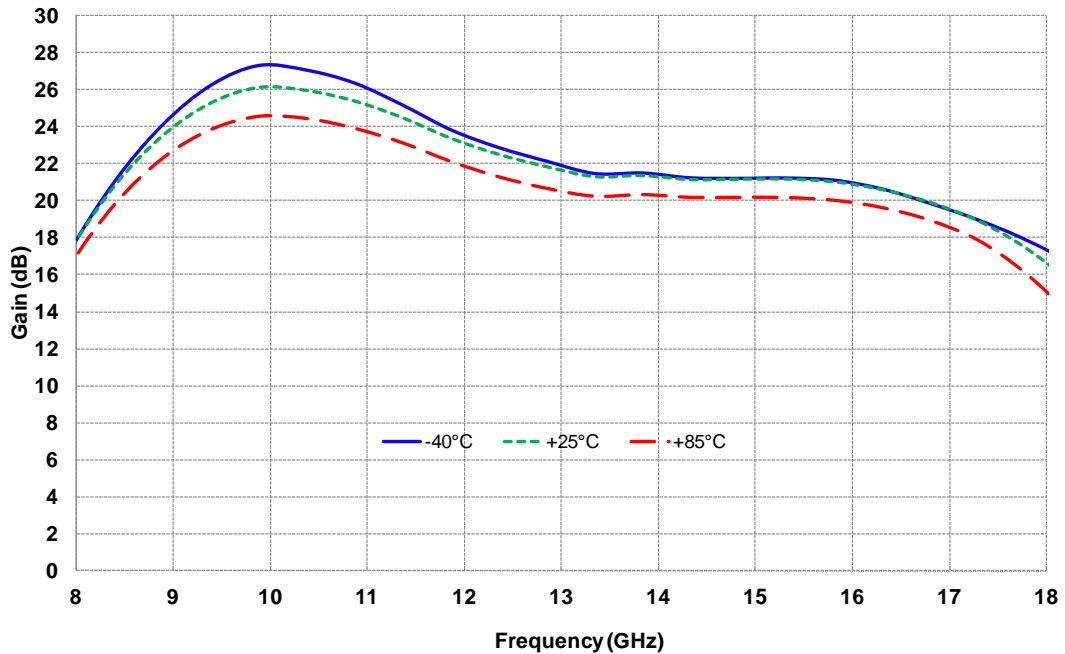


Typical Board Measurements

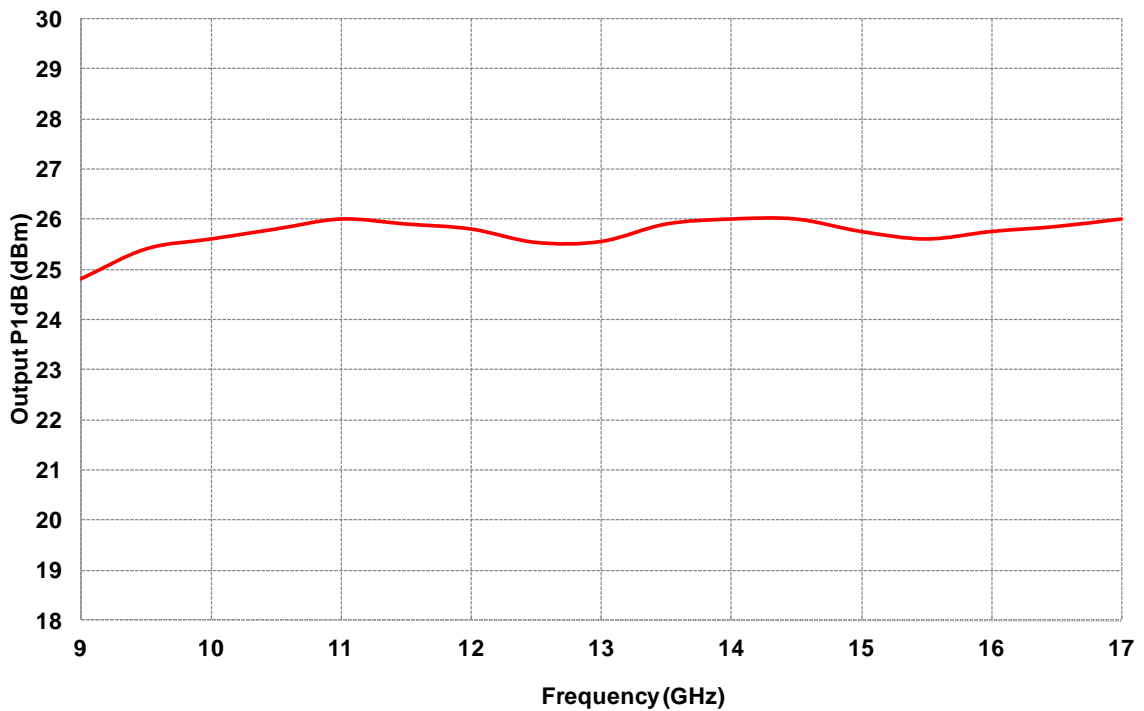
Vd = +5.0V, Id = 320mA

Measurement in the plan of the connectors, using the proposed land pattern & board, as defined in paragraph "Evaluation board"

Linear Gain versus Frequency & Temperature



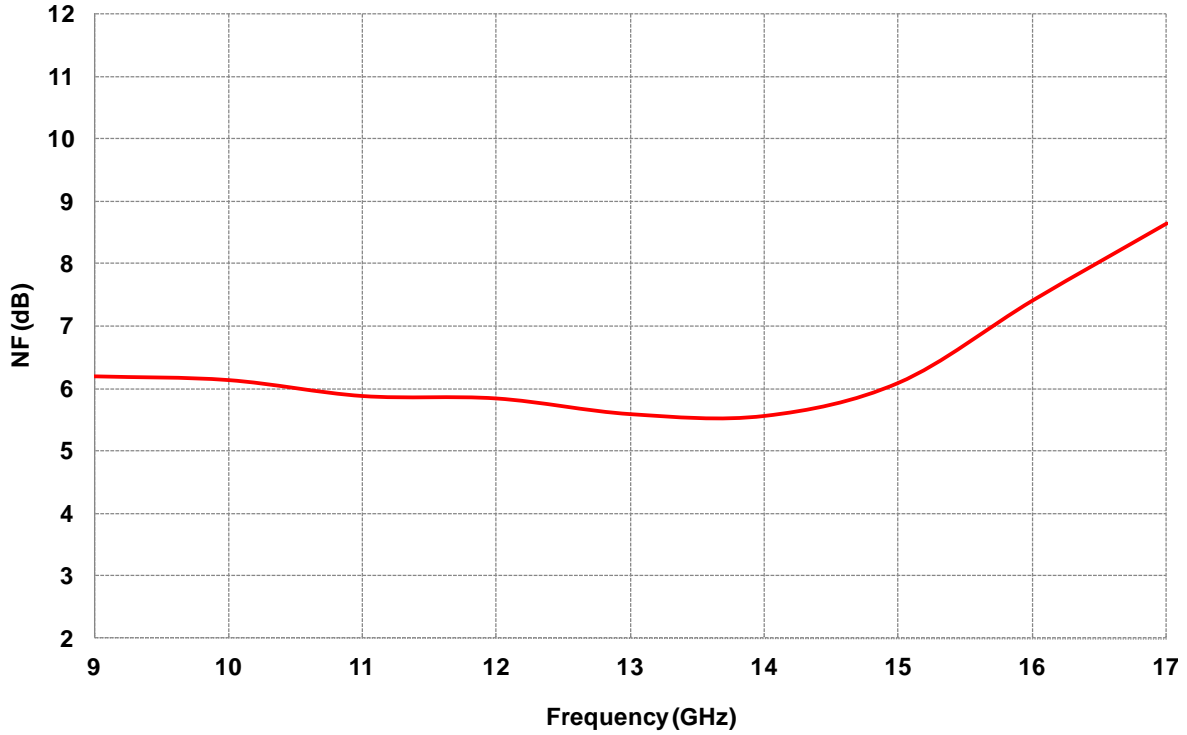
Output Power at 1dB compression versus Frequency



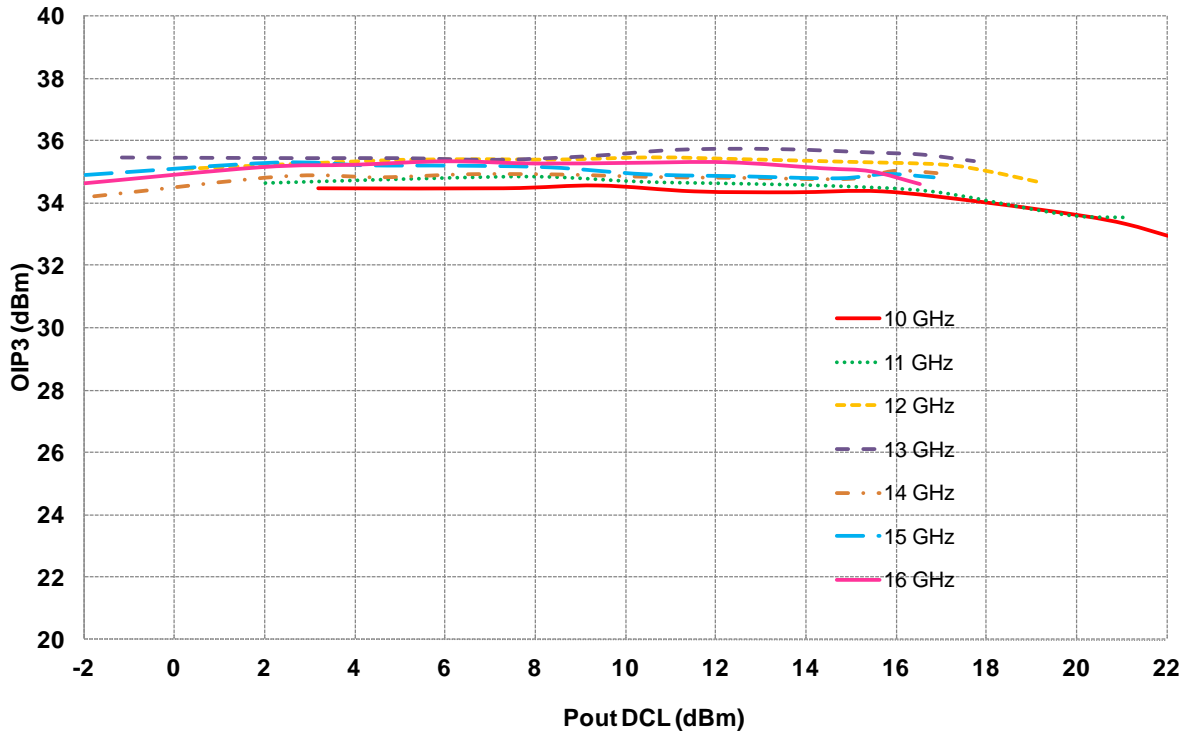
Typical Board Measurements

Tamb.= +25°C, Vd = +5.0V, Id = 320mA

Noise Figure versus Frequency



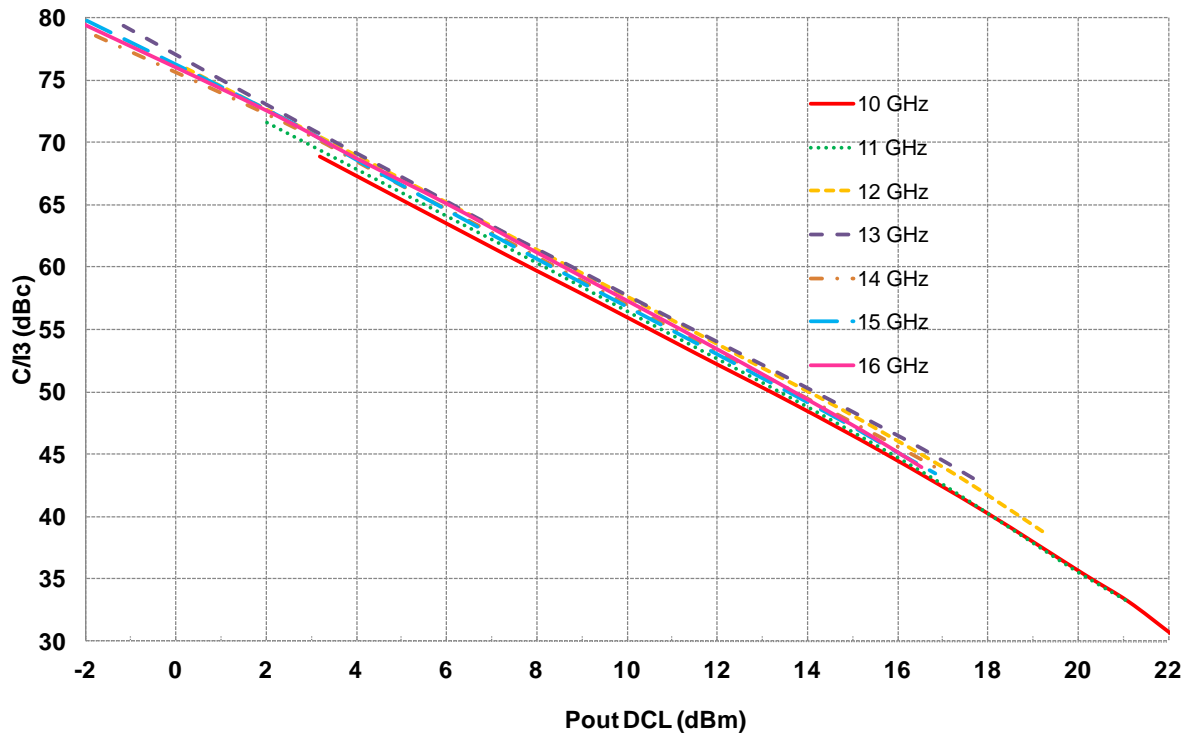
Output IP3 versus output power & Frequency



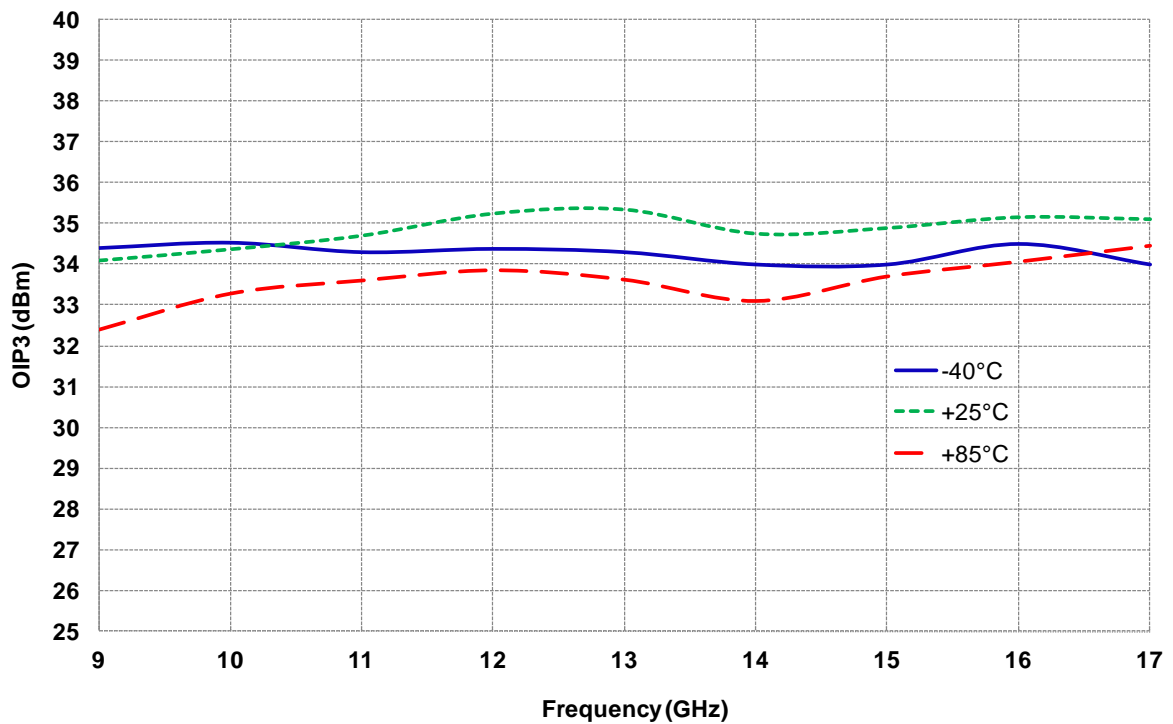
Typical Board Measurements

Tamb.= +25°C, Vd = +5.0V, Id = 320mA

C/I3 versus Pout DCL & frequency

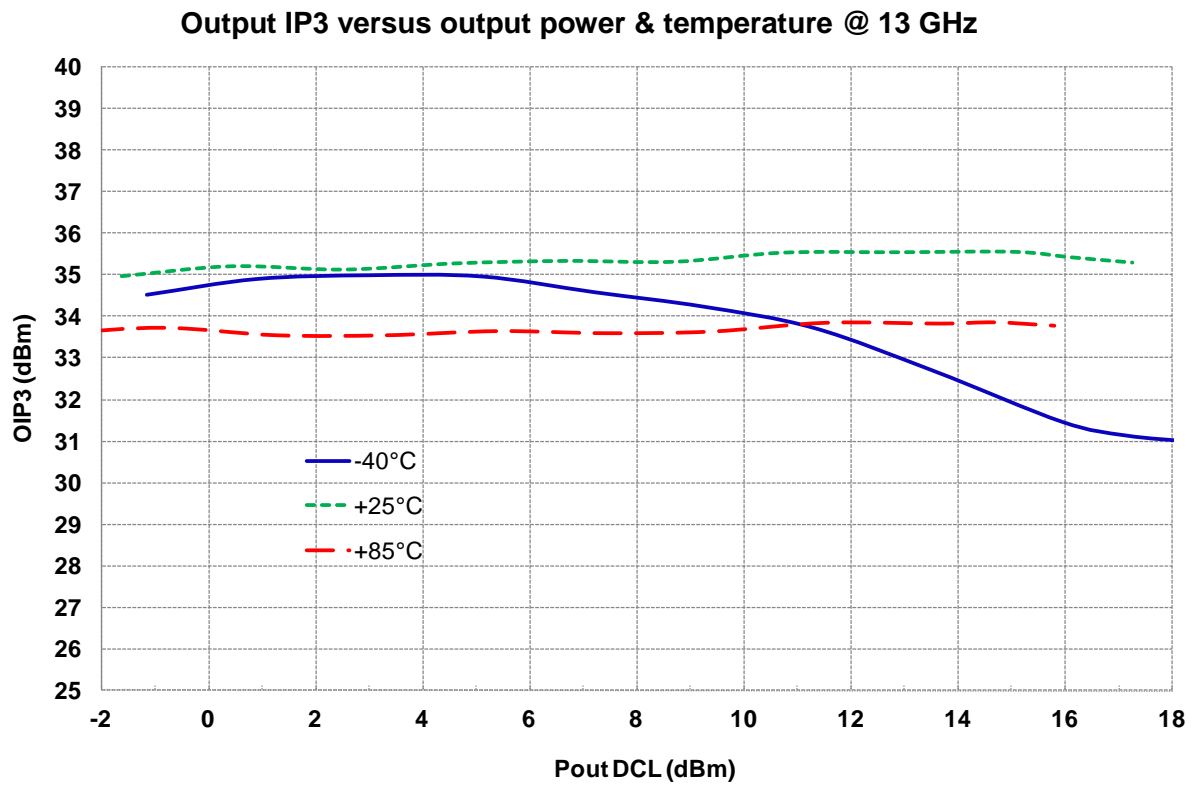


Output IP3 versus frequency & temperature @ Pout DCL = 9 dBm

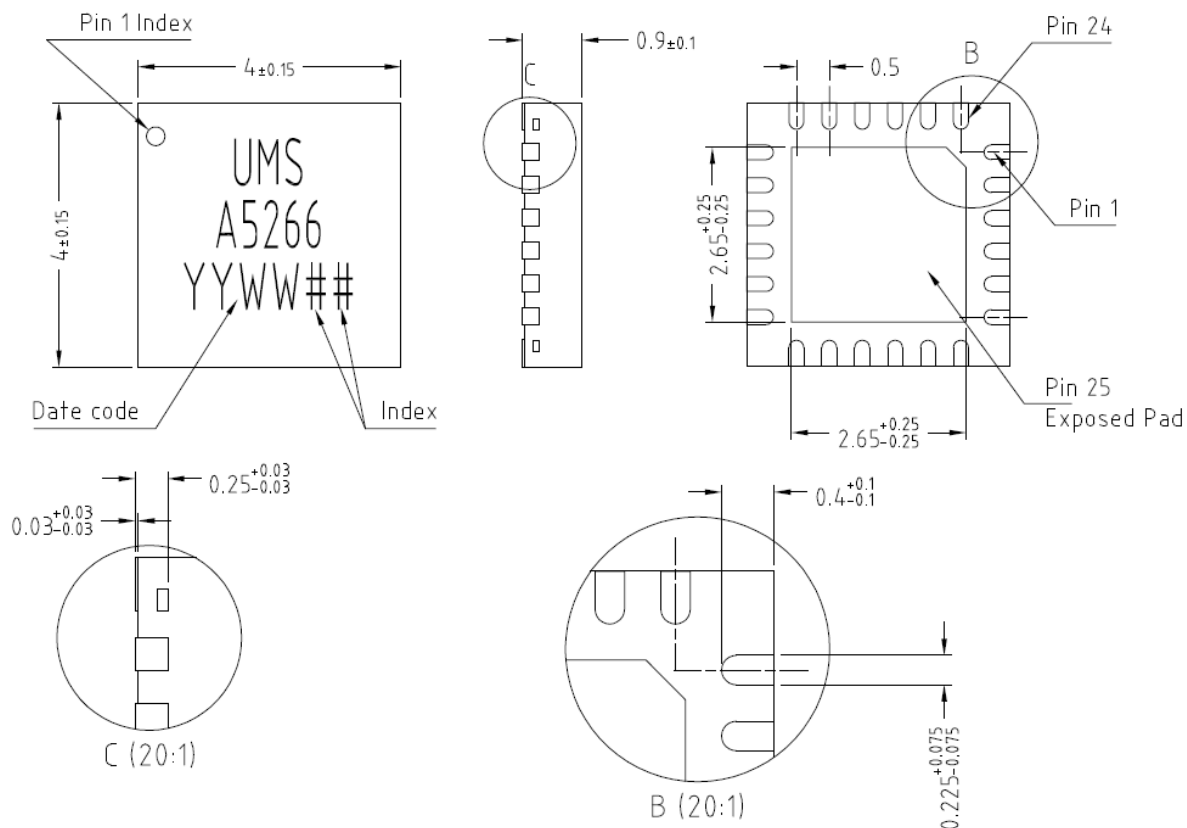


Typical Board Measurements

Vd = +5.0V, Id = 320mA



Package outline (1)



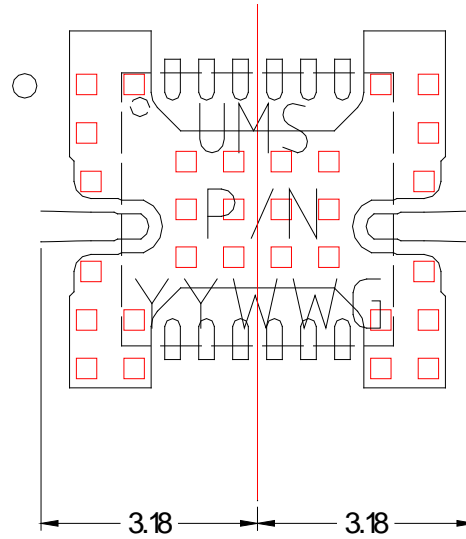
Matt tin, Lead Free	(Green)	1- Nc	9- VG1	17- Gnd ⁽²⁾
Units :	mm	2- Gnd ⁽²⁾	10- VG2	18- Gnd ⁽²⁾
From the standard :	JEDEC MO-220	3- Gnd ⁽²⁾	11- VG3	19- Nc
	(VGGD)	4- RF in	12- Nc	20- VD3
	25- GND	5- Gnd ⁽²⁾	13- Gnd ⁽²⁾	21- VD2
		6- Gnd ⁽²⁾	14- Gnd ⁽²⁾	22- VD1
		7- Gnd ⁽²⁾	15- RF out	23- Nc
		8- Nc	16- Gnd ⁽²⁾	24- Nc

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (<https://www.ums-rf.com>) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.18mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".

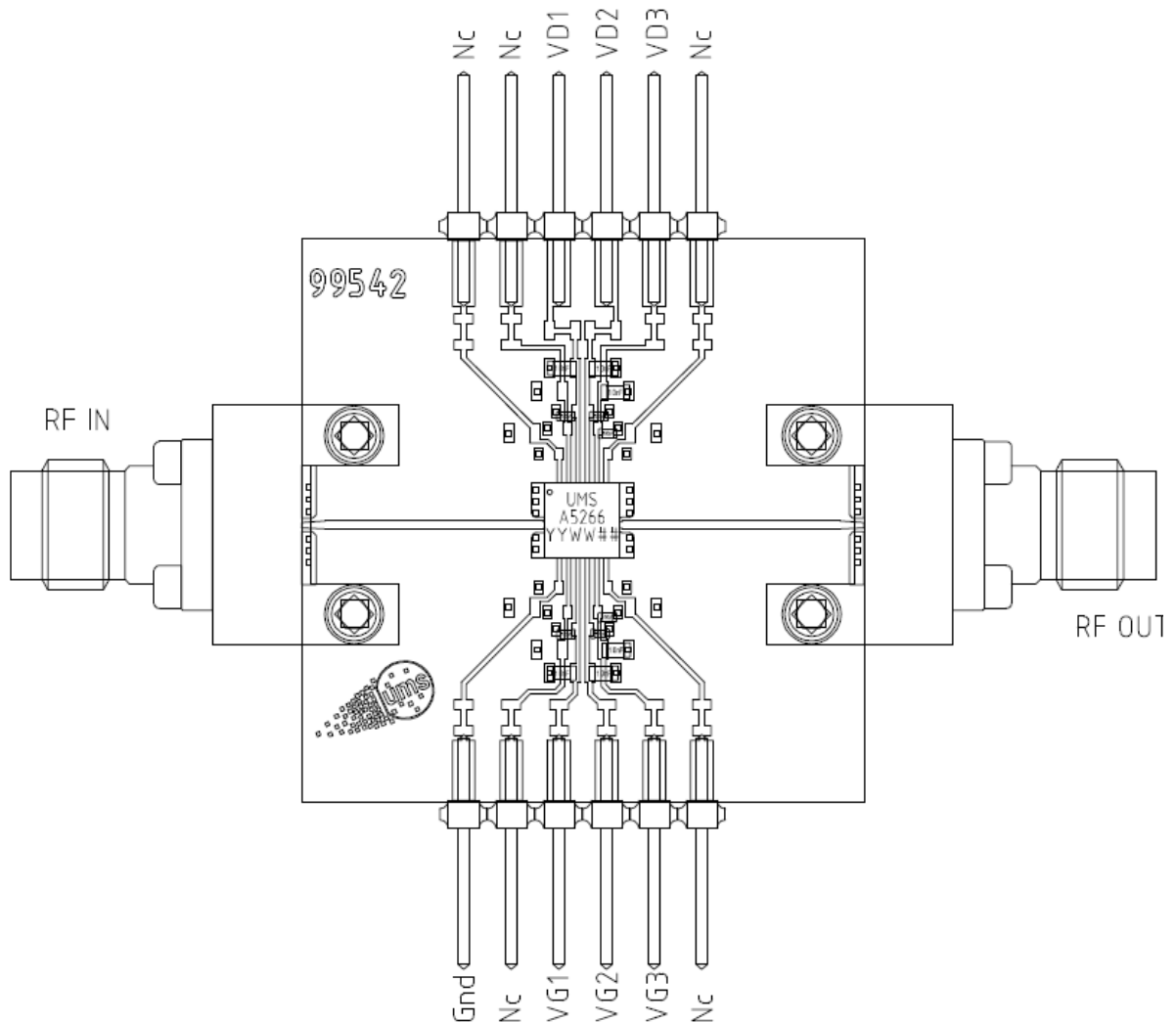


Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% matte tin (Sn)
MSL Rating	MSL1

Evaluation mother board

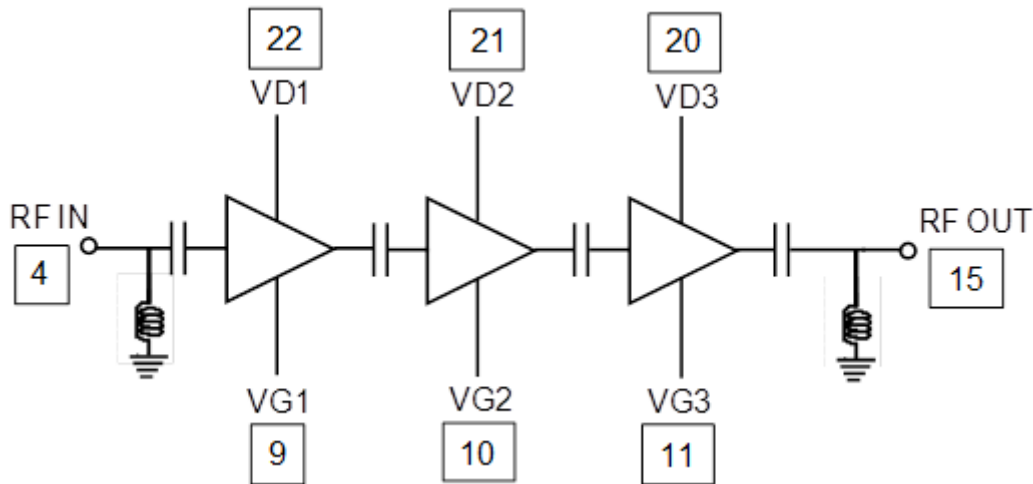
- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- First decoupling network is done with 100pF capacitors, second decoupling network is done with 10nF capacitors.
- See application note AN0017 for details.



Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.

Notes

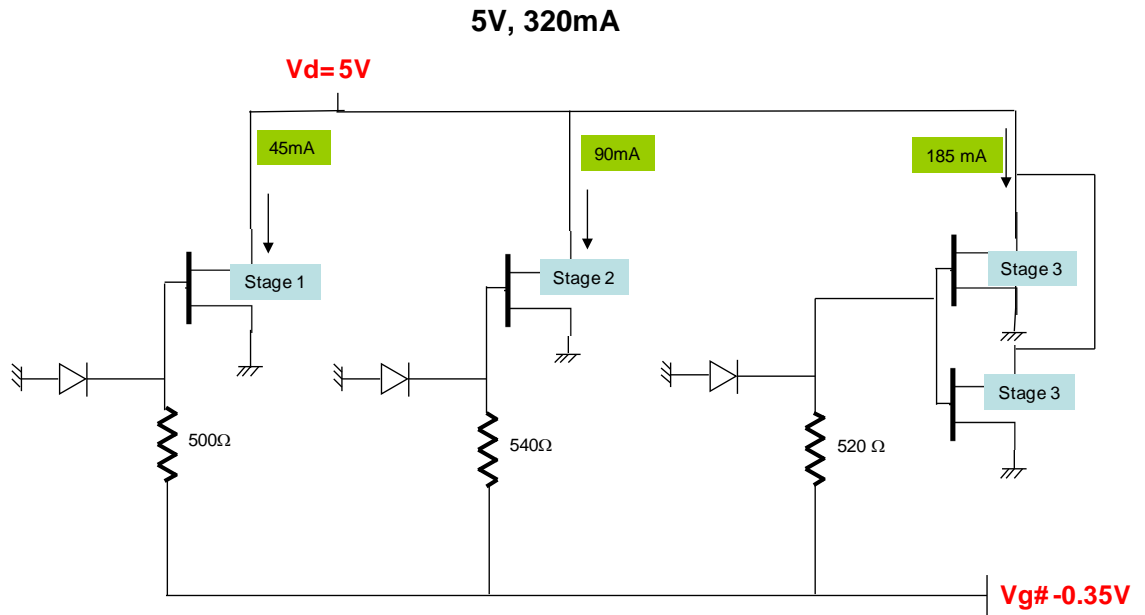
Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.



ESD protections are also implemented on gate and control accesses.

The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (100pF + 10nF) on the PC board, as close as possible to the package.

DC Schematic



Recommended package footprint

Refer to the application note AN0017 available at <https://www.ums-rf.com> for package footprint recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017 at <https://www.ums-rf.com>.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <https://www.ums-rf.com>.

Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x4 package:

CHA5266-QDG/XY

Stick: XY = 20

Tape & reel: XY = 21

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