United Monolithic Semiconductors

CHA3395-98F

21-30GHz Medium Power Amplifier

GaAs Monolithic Microwave IC

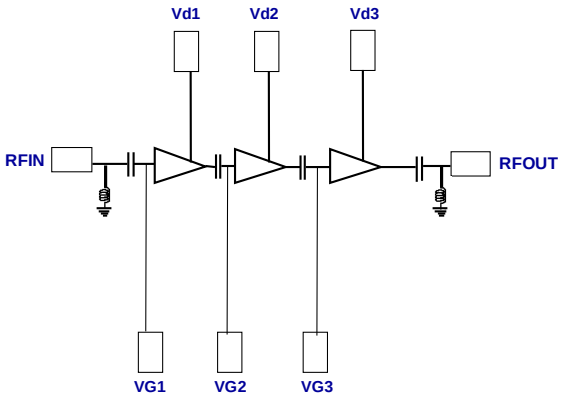
Description

The CHA3395-98F is a 3 stages monolithic Medium Power Amplifier, which produces 24dB gain for 20 dBm output power at 1dB compression.

It is designed for a wide range of applications, from space to commercial communication systems.

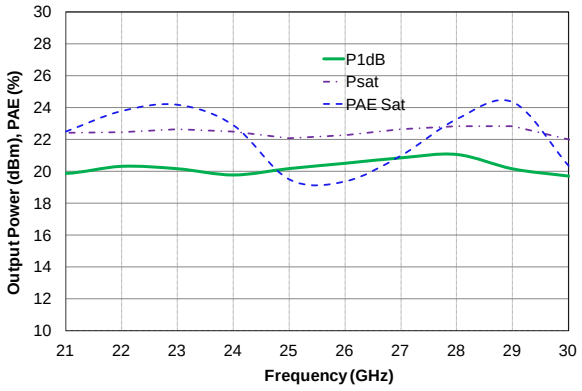
The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is available in chip form.



Main Features

- Broadband performances: 21-30GHz
- 20dBm Pout at 1dB compression
- 24dB gain
- 32dBm OTOI
- DC bias: Vd= 4.0V, Id= 180mA
- Chip size 1.5x2.5x0.1mm



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	21		30	GHz
Gain	Linear Gain		24		dB
P-1dB	Output Power @1dB comp.		20		dBm
OTOI	3rd order Intercept point		32		dBm

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Electrical Characteristics

Tamb.= +25°C, Vd = +4.0V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	21		30	GHz
Gain	Linear Gain		24.0		dB
ΔG	Gain variation in temperature		0.023		dB/°C
G_{CTRL}	Gain control range		15		dB
OTOI	3rd order Intercept point		32		dBm
P_{-1dB}	Output power @ 1dB compression		20		dBm
Psat	Saturated Output Power		22.5		dBm
RLin	Input Return Loss		12		dB
RLout	Output Return Loss		20		dB
NF	Noise figure		4.5		dB
Id	Quiescent Drain current		180		mA
Vg	Gate voltage		-0.4		V

These values are representative of test fixture measurements that are made in the chips access plan.
A bonding wire of typically 0.1 to 0.15nH will improve the matching at the accesses.

“Power ON” sequence

1. Ground the device
2. Bias MPA gate voltage at Vg low enough (Typically: Vg ≈ -1V)
3. Apply Vds bias voltage (Typically: Vd = 4V)
4. Increase slowly Vgs up to quiescent bias drain current Idq
5. Apply RF signal

“Power OFF” sequence

1. Turn off RF signal
2. Bias MPA gate voltage at Vg low enough (Typically: Vg ≈ -1V)
3. Turn Vds bias voltage to 0V
4. Turn Vgs bias voltage to 0V

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4.5V	V
Id	Drain bias quiescent current	260	mA
Vg	Gate bias voltage	-2 to +0.4	V
Vdg	External drain-gate excursion	5	V
Pin	Maximum input power	6	dBm
Tj	Maximum junction temperature (2)	175	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) Thermal Resistance channel to ground paddle

Recommended Operating Range 3, 4

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	3.3 to 4	V
Id	Drain bias current	100 to 180	mA
Vg	Gate bias voltage	-1 to 0	V
Pin	Maximum peak input power overdrive	5	dBm

(3) Electrical performances are defined for specified test conditions

(4) Electrical performances are not guaranteed over all recommended operating conditions

Temperature Range

Ta	Operating temperature range	-40 to +95	°C
Tstg	Storage temperature range	-55 to +150	°C

Typical Bias Conditions

Tamb.= +25°C

Symbol	Parameter	Values	Unit
VG1	DC Gate voltage 1st stage	-0.4	V
VG2	DC Gate voltage 2nd stage	-0.4	V
VG3	DC Gate voltage 3rd stage	-0.4	V
VD1	DC Drain voltage 1st stage	4.0	V
VD2	DC Drain voltage 2nd stage	4.0	V
VD3	DC Drain voltage 3rd stage	4.0	V

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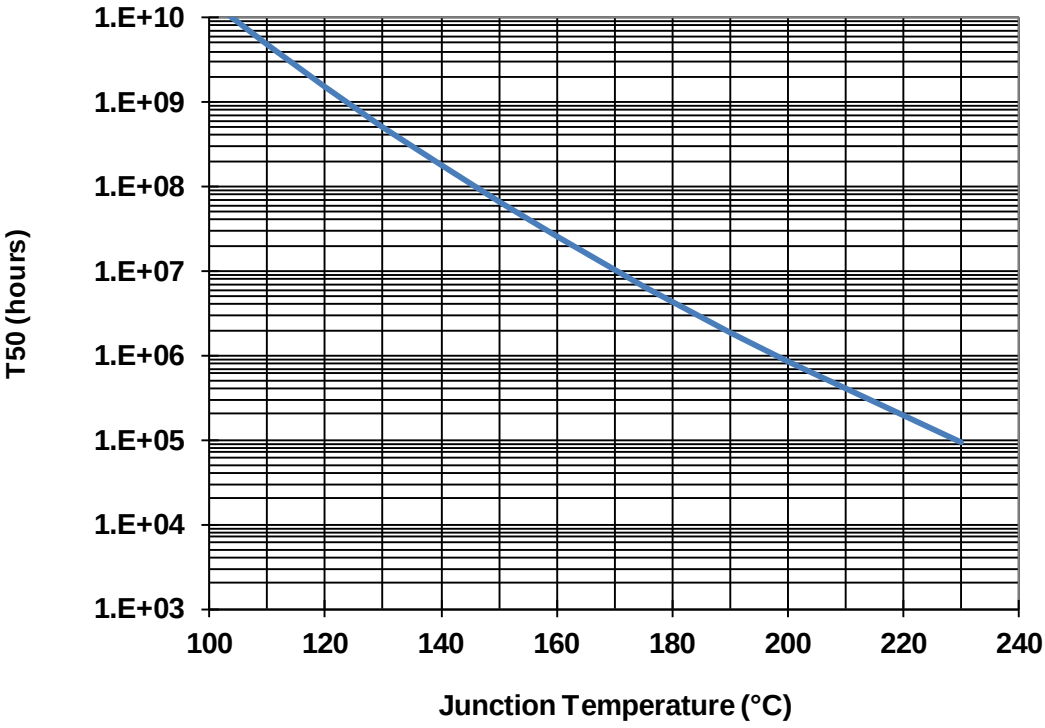
Device thermal information

The device thermal performances below are based on UMS rules to evaluate the junction temperature.
The temperature Tb_{chip} is defined as the chip back side. The thermal resistance (Rth_eq) is given for the full circuit, and assumes CW operation mode in the table.

Thermal Resistance(1)	Rth_eq	Tb_{chip} =85°C, Vd=4V, Idq=180mA	94.4	°C/W
Junction Temperature	Tj	Pdiss=720mW	160	°C



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Typical test fixture Sij parameters

Tamb.= +25°C, Vd = +4V, Id = 180mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
2.0	-0.536	63.5	-63.708	-33.2	-64.063	-32.7	-1.074	38.1
3.0	-0.496	6.2	-62.062	-95.3	-62.702	-86.2	-1.033	-30.8
4.0	-0.483	-51.1	-63.501	-168.2	-63.540	-139.8	-1.112	-99.7
5.0	-0.561	-109.3	-70.089	138.5	-55.832	-173.8	-1.361	-169.3
6.0	-0.767	-167.5	-85.253	-158.3	-44.743	79.0	-1.667	120.3
7.0	-1.121	134.9	-67.613	-179.3	-35.106	-37.2	-1.977	49.7
8.0	-1.460	75.7	-63.555	119.1	-27.214	-146.4	-2.276	-20.5
9.0	-1.568	15.4	-62.670	50.8	-21.064	111.5	-2.667	-89.7
10.0	-1.469	-40.6	-62.911	-32.0	-15.864	16.7	-3.357	-158.8
11.0	-1.419	-93.0	-62.089	-151.1	-10.842	-74.3	-4.654	130.3
12.0	-1.508	-148.0	-57.192	98.2	-5.994	-166.0	-6.875	55.3
13.0	-1.615	152.1	-54.717	18.8	-1.919	100.9	-9.987	-27.2
14.0	-1.642	93.8	-53.780	-43.0	1.356	11.2	-12.973	-119.0
15.0	-1.808	39.7	-53.312	-79.4	4.624	-73.5	-14.372	151.0
16.0	-2.399	-17.1	-50.245	-125.4	8.426	-157.7	-15.274	76.4
17.0	-3.591	-84.3	-47.893	178.1	12.565	114.0	-18.240	17.9
18.0	-5.011	-163.3	-45.270	111.7	16.562	20.9	-24.111	-18.4
19.0	-6.054	108.9	-46.489	43.0	20.065	-78.2	-22.958	27.3
20.0	-7.698	27.1	-51.258	-31.8	22.043	-178.4	-14.162	-22.9
21.0	-10.667	-26.5	-59.478	-29.6	24.150	82.1	-15.368	-71.8
22.0	-15.857	-53.8	-63.627	-91.2	25.848	-21.6	-23.513	-123.8
23.0	-15.369	-86.1	-53.877	0.0	25.209	-124.6	-18.889	-85.3
24.0	-14.137	-127.7	-47.362	-70.6	24.783	141.4	-15.789	-107.8
25.0	-10.419	-161.5	-44.950	-129.6	24.392	48.7	-13.171	-144.3
26.0	-8.155	159.9	-43.528	170.8	24.011	-41.4	-13.052	162.1
27.0	-9.443	115.8	-42.957	111.3	24.236	-133.5	-18.511	101.9
28.0	-14.299	58.1	-43.822	52.5	23.907	128.4	-37.993	112.7
29.0	-17.581	-30.3	-45.992	-8.2	22.590	31.8	-30.117	-170.2
30.0	-12.263	-107.2	-52.894	-60.3	21.480	-63.9	-18.299	-149.9
31.0	-6.762	178.2	-54.003	-21.0	19.755	-165.5	-11.250	158.0
32.0	-3.035	106.3	-49.823	-77.4	16.274	92.4	-7.671	92.8
33.0	-1.798	47.5	-50.759	-113.1	11.758	1.2	-6.671	17.7
34.0	-1.675	-8.3	-51.892	-155.5	7.936	-84.3	-6.471	-66.5
35.0	-1.732	-77.5	-51.394	-83.5	4.001	-173.2	-5.856	-154.4
36.0	-1.414	-148.1	-36.881	-169.8	-1.254	99.8	-5.514	118.7
37.0	-1.195	158.7	-34.715	103.1	-6.734	21.0	-5.095	30.3
38.0	-1.142	114.6	-34.098	12.8	-11.972	-55.2	-4.453	-66.9
39.0	-1.136	68.1	-39.290	-54.0	-18.737	-134.3	-3.041	-164.1
40.0	-1.249	17.4	-44.969	-100.3	-27.448	154.8	-2.185	114.4

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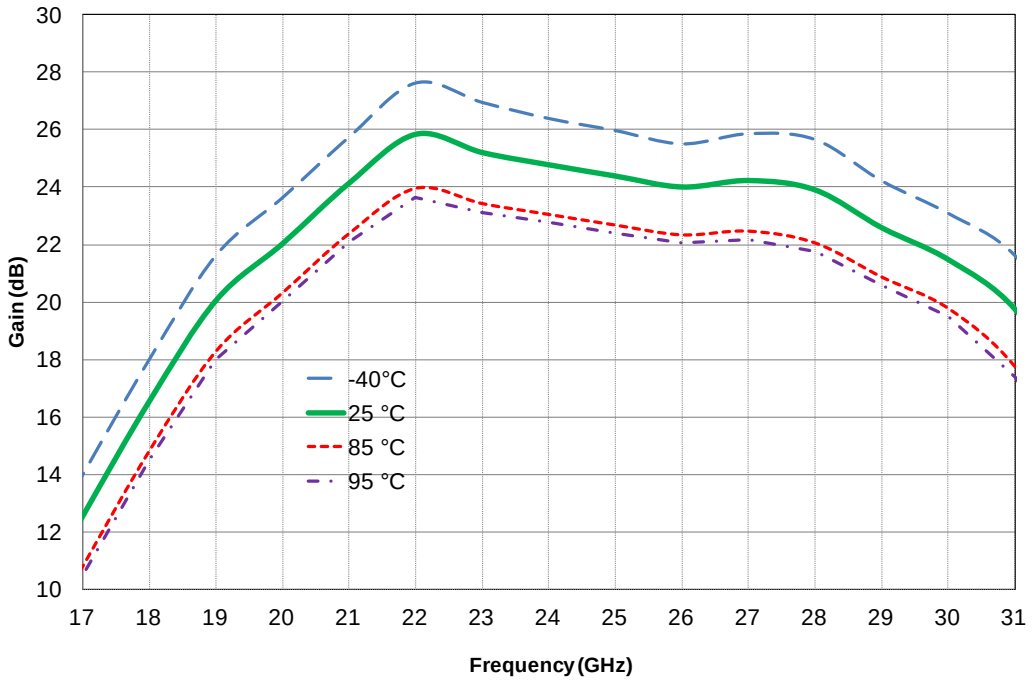
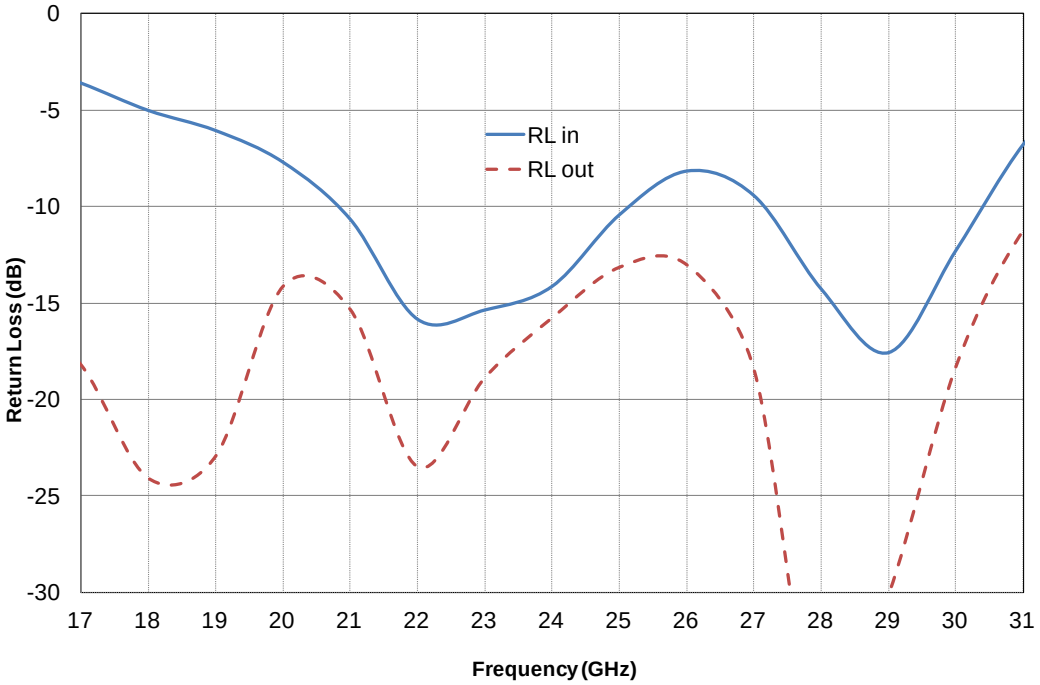
Typical test fixture Measurements

Tamb.= +25°C, Vd = +4.0V, Id = 180mA
These values are representative of test fixture measurements as defined on the drawing in paragraph "Evaluation board".

Linear Gain versus Frequency in Temperature



Return losses versus Frequency



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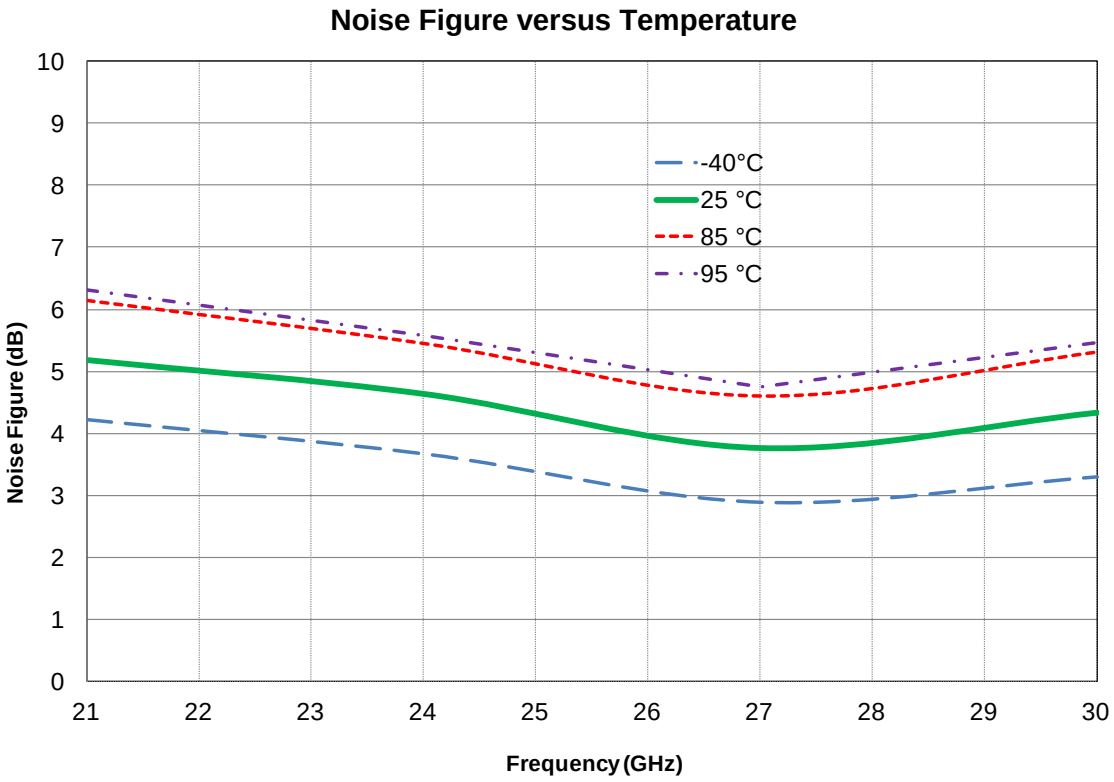
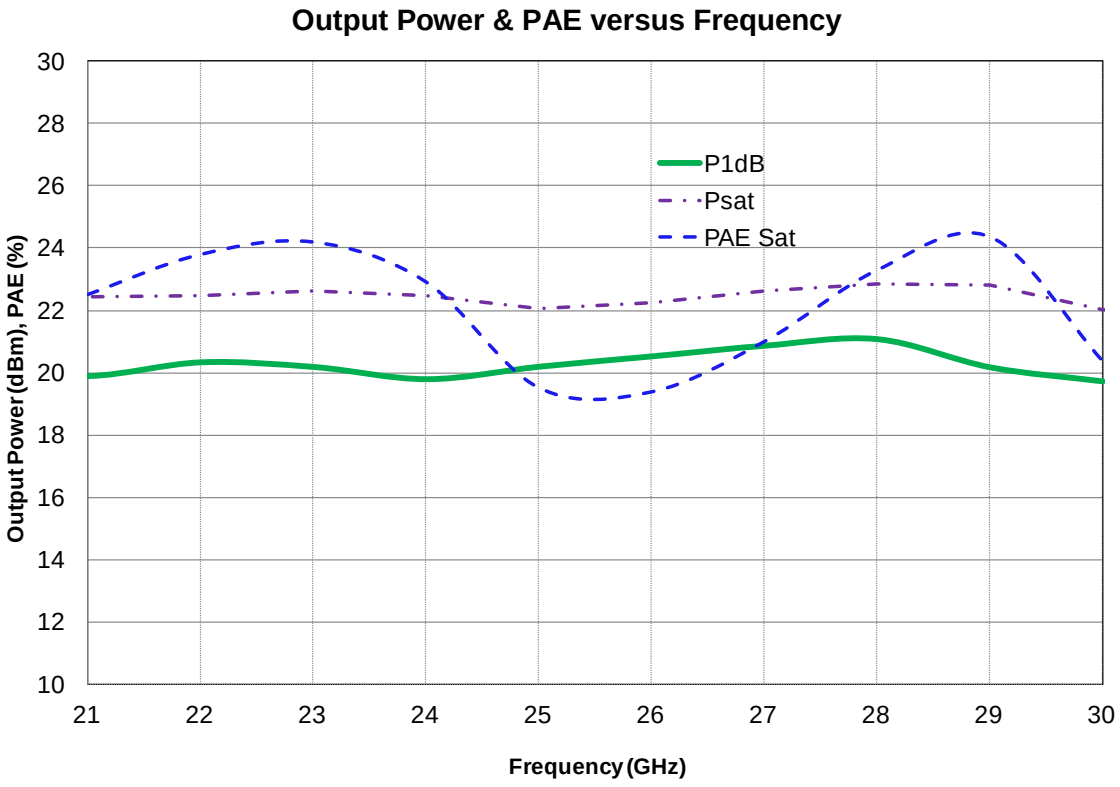
Typical test fixture Measurements

Tamb.= +25°C, Vd = +4.0V, Id = 180mA





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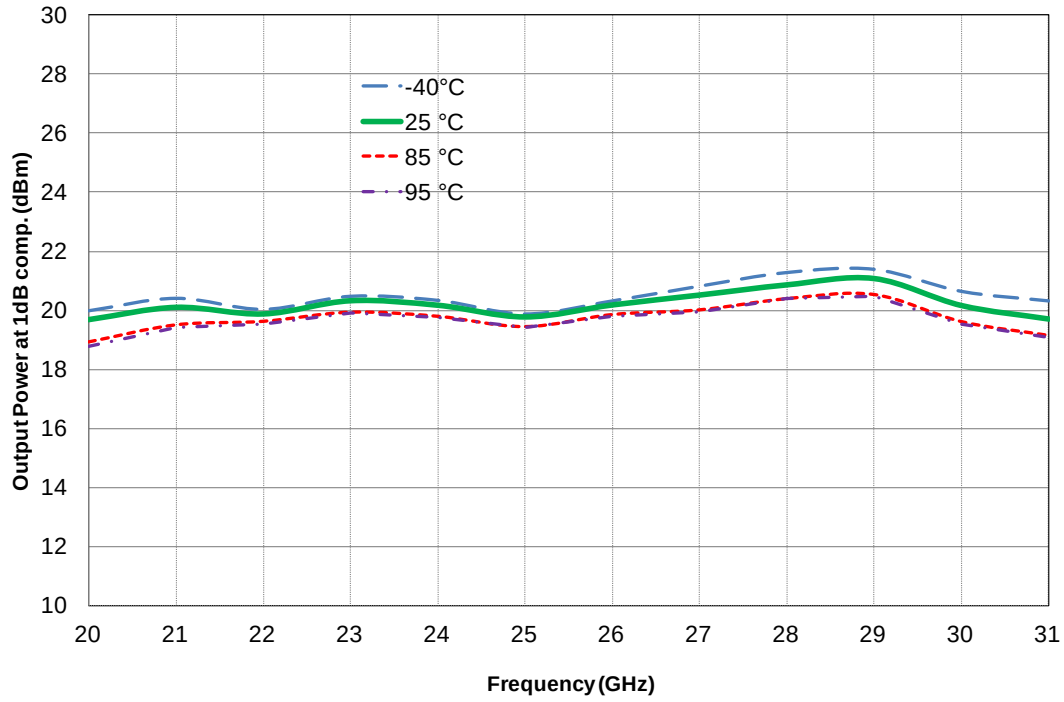
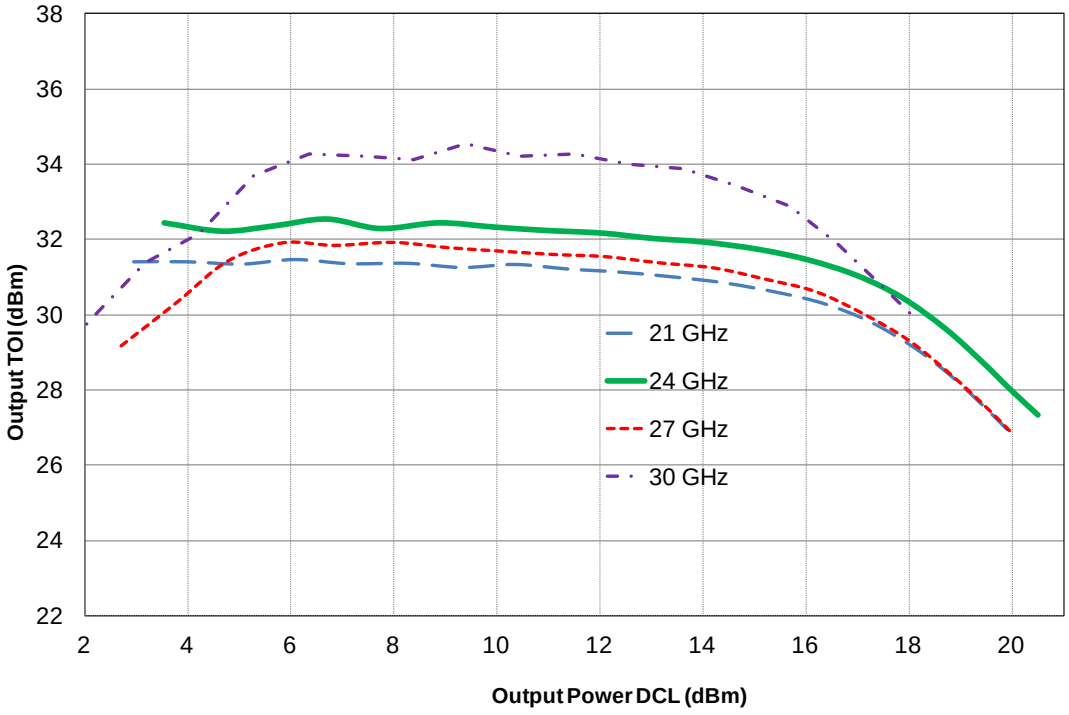
Typical Board Measurements

Tamb.= +25°C, Vd = +4.0V, Id = 180mA

Pout at 1dB compression versus Temperature



Output TOI versus Output Power DCL



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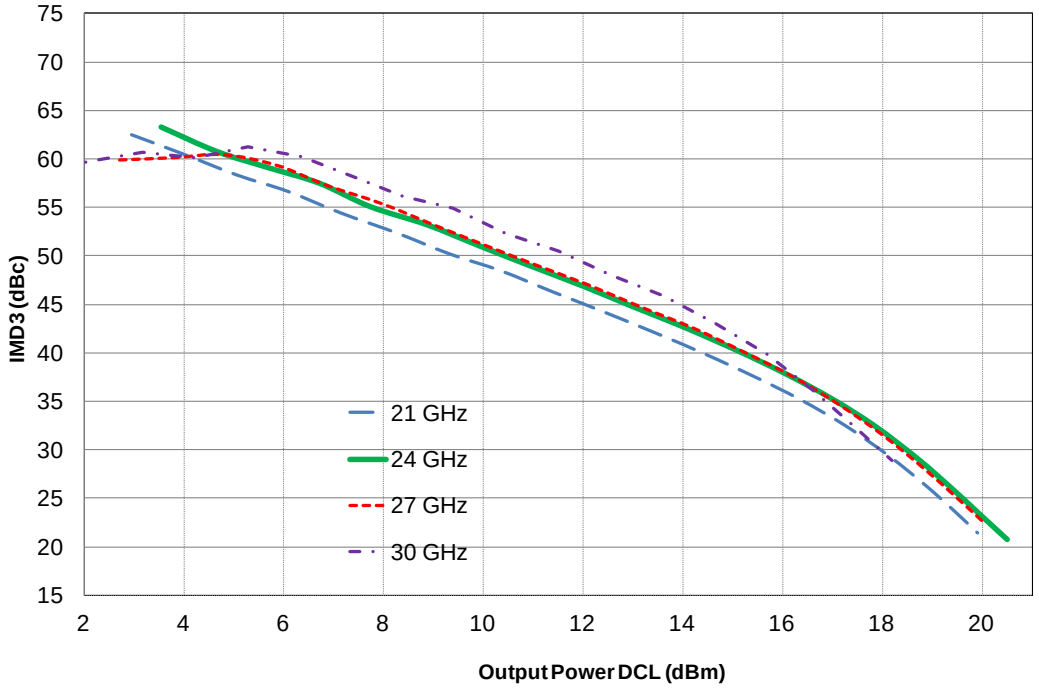
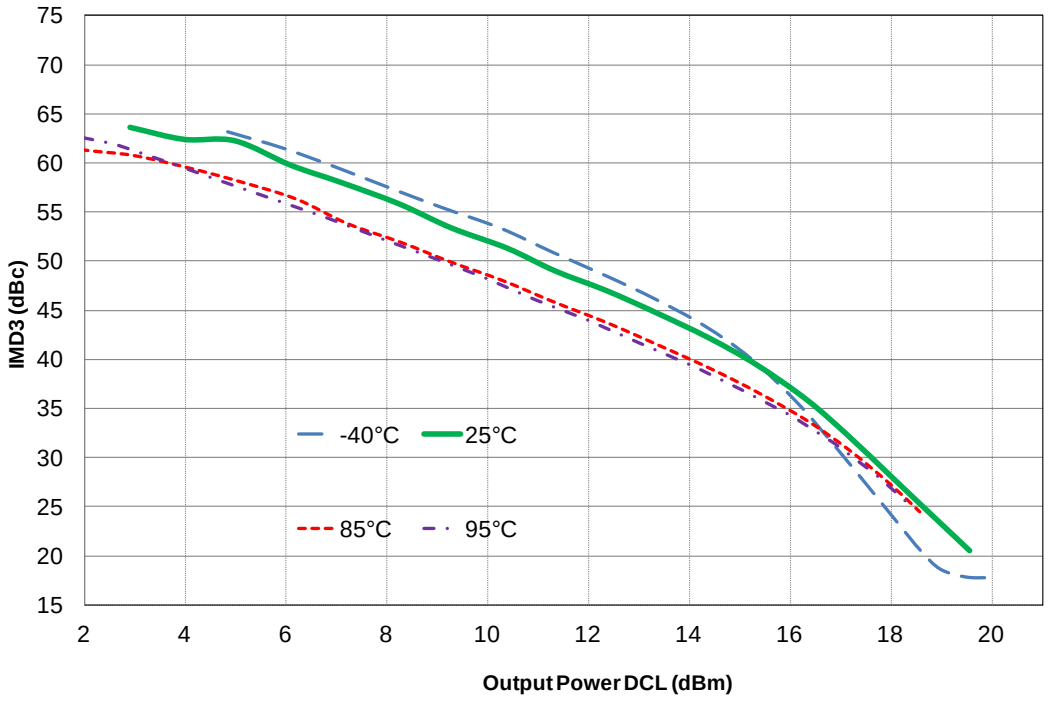
Typical Board Measurements

Tamb.= +25°C, Vd = +4.0V, Id = 180mA

IMD3 versus Output Power DCL



IMD3 versus Temperature at 26GHz



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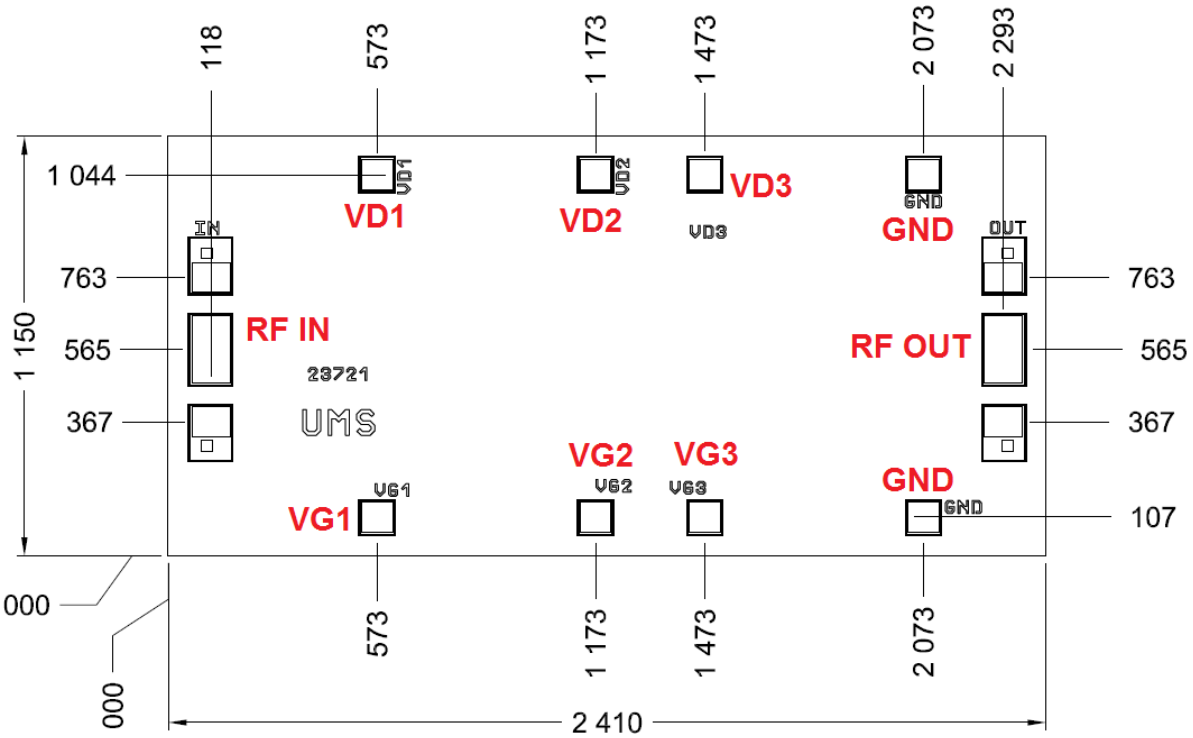
Mechanical data



Chip thickness: 100µm.
Chip size: 2410x1150 ±35µm
DC pad size: 83µm x 86 µm (BCB opening)
RF pad size: 97µm x 146 µm (BCB opening)
All dimensions are in micrometers

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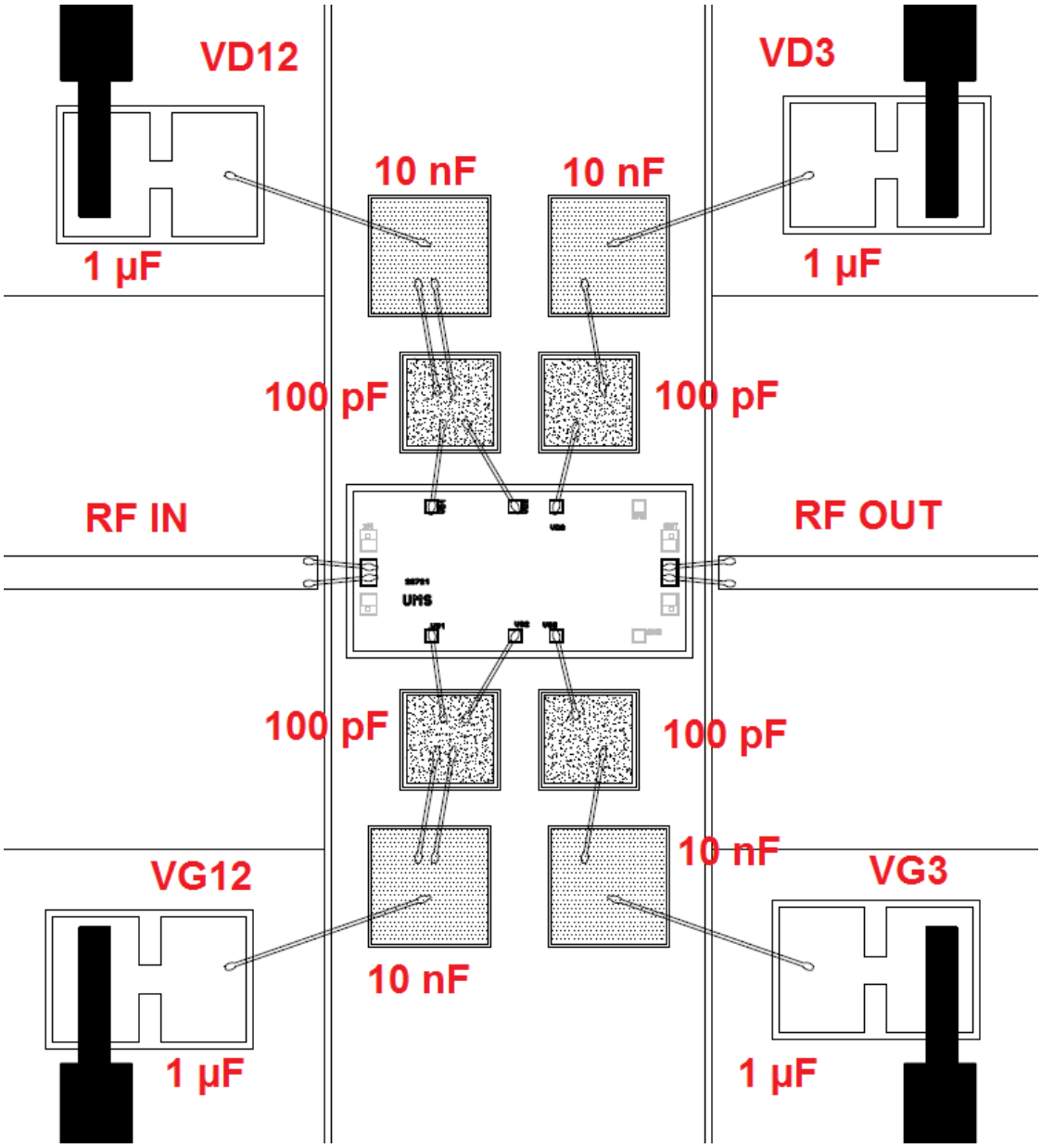
Recommended assembly plan



Note: Supply feed should be bypassed. 25µm diameter gold wire is to be preferred.

Recommended circuit bonding table

Label	Type	Decoupling	Comment
VD12, VD3	Vd	100pF & 10nF & 1µF	Drain Supply
VG12, VG3,	Vg	100pF & 10nF & 1µF	Gate Supply

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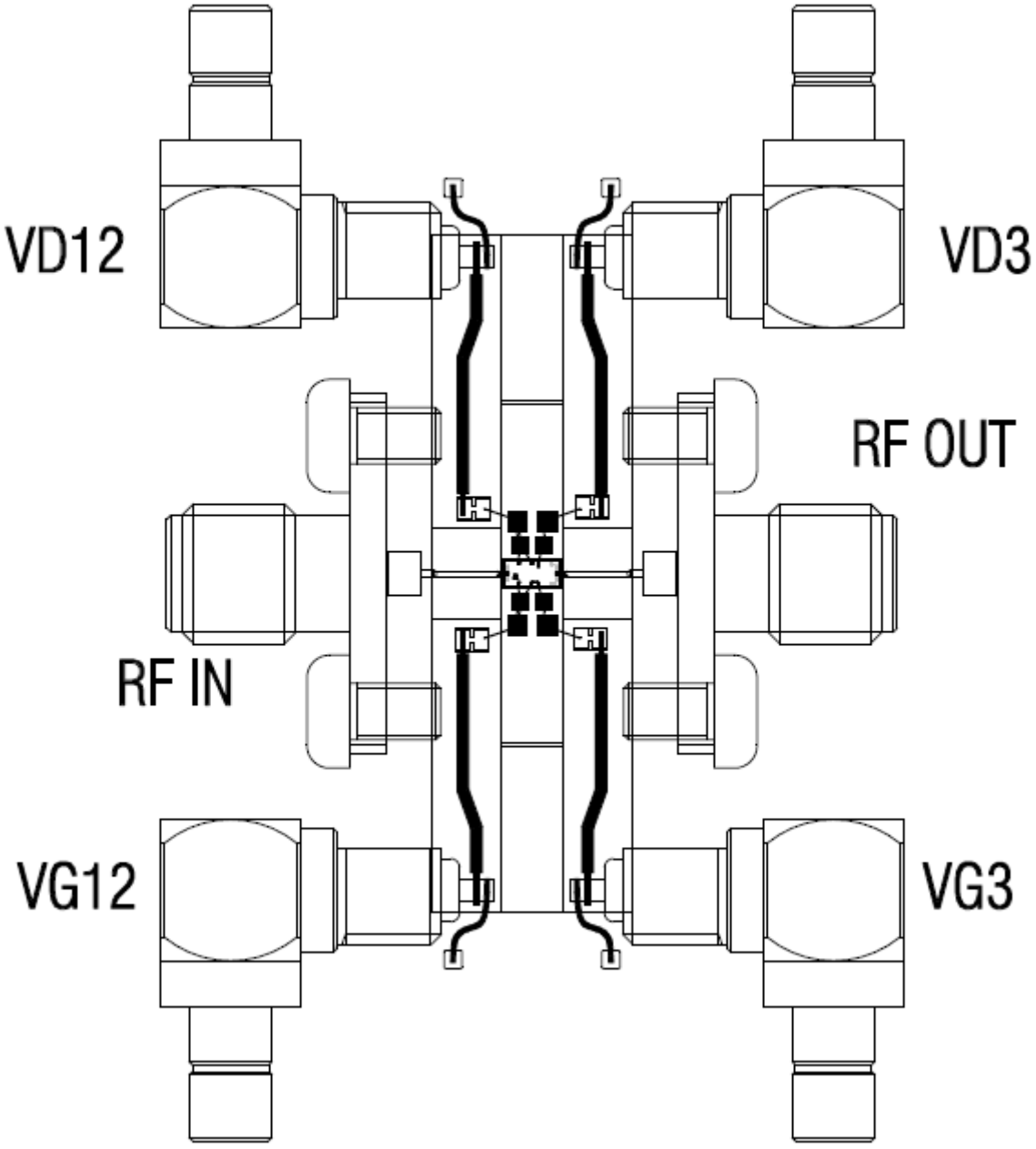
Evaluation mother board

■ Decoupling capacitors of 100nF ±10%, 10nF ±20% and 1µF ±10% are recommended for all DC accesses.
■ Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.



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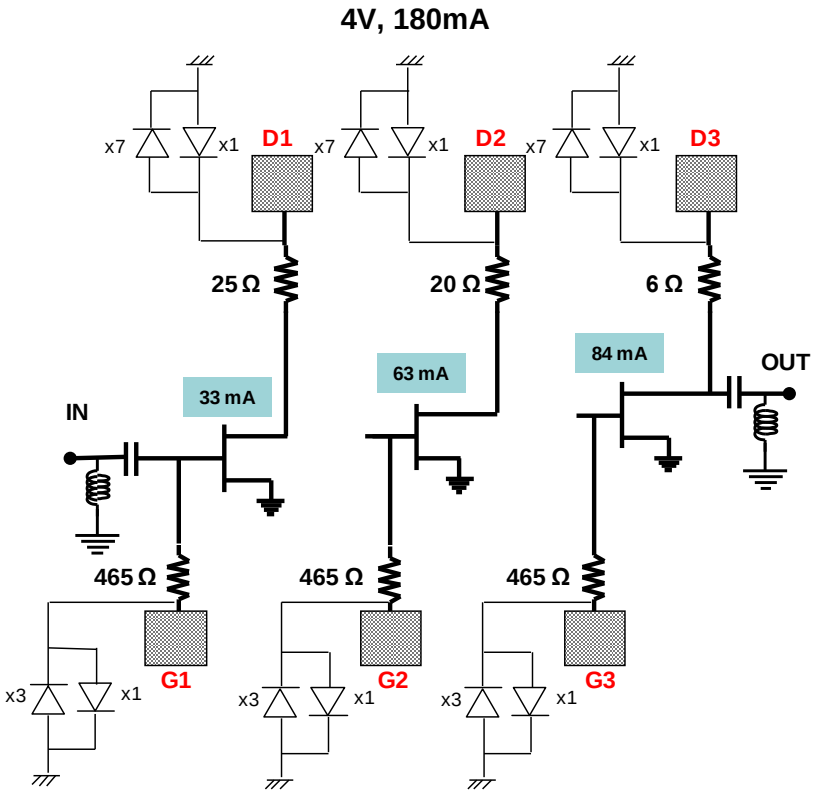
DC Schematic



Notes

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Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

User guide for bare dies

Refer to the application note AN0001 available at https://www.ums-rf.com for UMS user guide for bare dies handling

Ordering Information

Chip form:	CHA3395-98F/00

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