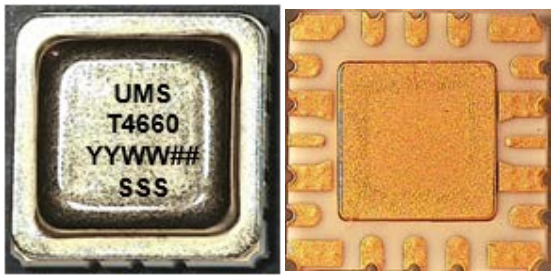
0.5-16GHz Variable Attenuator

GaAs IC in SMD hermetic leadless package

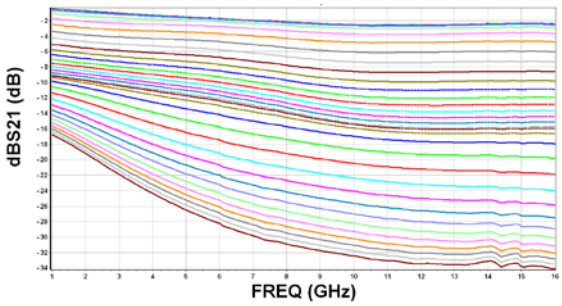
Description

The CHT4660-FAB is a variable 0.5-16GHz attenuator designed for a wide range of applications, for Space, military and commercial communication systems.
The circuit is manufactured with a MESFET process, 0.7µm gate length, via holes through the substrate and air bridges.
It is supplied in RoHS compliant hermetic SMD package.



Main Features

- Broadband performance: 0.5-16GHz
- 27dBm typical input 1dB compression point (Any attenuation)
- 35dB dynamic range
- DC bias: -5V<V1<0V ; -5V<V2<0V
- 6x6mm² hermetic metal ceramic package



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fin	Input frequency range	0.5		16	GHz
Min Att.	|S21| (V1=-5V;V2=-5V) (0,5 to 16GHz)		2		dB
Max Att.	|S21| (V1=0V;V2=0V) (0,5 to 16GHz)		30		dB
Pin1dB	Input 1dB compression point (any attenuation)		27		dBm

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Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	0.5		16	GHz
Min Att.	|S21| (V1=-5V; V2=-5V) (0.5 to 6GHz) |S21| (V1=-5V; V2=-5V) (6 to 10GHz) |S21| (V1=-5V; V2=-5V) (10 to 16GHz)		1.5 2 2.5	2 3 3	dB
Max Att.	|S21| (V1=0V; V2=0V) (0.5 to 6GHz) |S21| (V1=0V; V2=0V) (6 to 10GHz) |S21| (V1=0V; V2=0V) (10 to 16GHz)	16 27 30	23 31 34		dB
RLin	Input Return Loss (any att.)		-10		dB
RLout	Output Return Loss (any att.)		-10		dB
Pin1dB	Input power for 1dB compression (min att.)		27		dBm
V1, V2	Control Voltages	-5		0	V

Recommended Operating Range [3] [4]

Tamb = +25°C

Symbol	Parameter	Values	Unit
V1, V2	Control Voltage	-5 to 0	V
Pin_max	Maximum input power	27-30	dBm

[3] Electrical performances are defined for specified test conditions

[4] Electrical performances are not guaranteed over all recommended operating conditions

Temperature Range

Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
V1	V1 control voltage	-6V to +0.6V	V
V2	V2 control voltage	-6V to +0.6V	V
Pin	RF input power	30	dBm
Tj	Junction temperature	175	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad Nº	Parameter	Values	Unit
V1	20	V1 control voltage	-5 to 0	V
V2	19	V2 control voltage	-5 to 0	V

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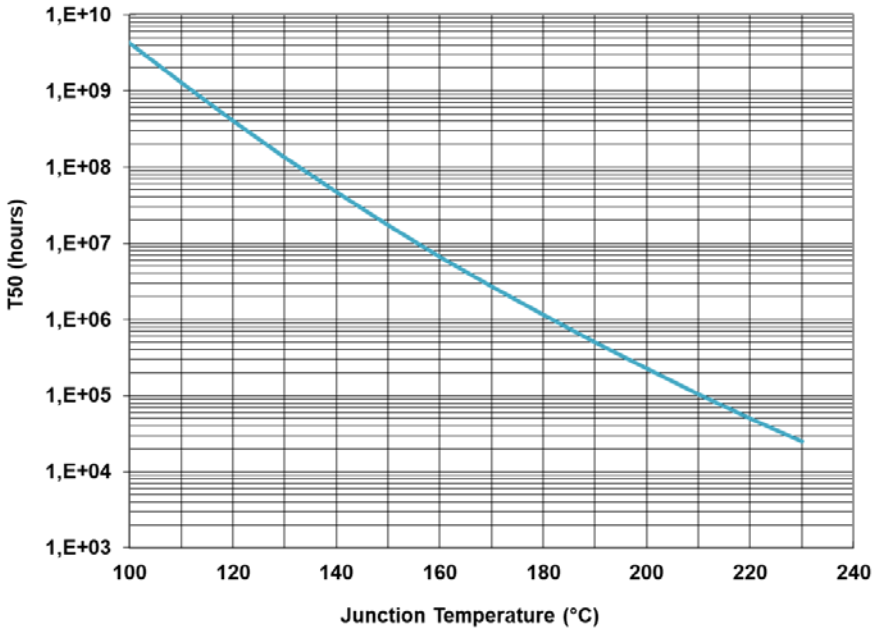
Device thermal performances

All the figures given in this section are obtained assuming that the packaged device is only cooled down by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tcase).
The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Absolute Maximum Ratings table.
So, the system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	Tjunction (°C)	R_{TH} (°C/W)	T50 (hours)
R_{TH} (1) Thermal Resistance (Junction to Case)	V1 = V2 = 0V(2) Pin = 27dBm Pdiss = 0.498W	125	80.5	1.5E+08
R_{TH} (1) Thermal Resistance (Junction to Case)	V1 = V2 = 0V(2) Pin = 29.5dBm Pdiss = 0.88W	175	102.5	2.0E+6

(1) Assuming 85°C Tcase
(2) Worst case for Tj



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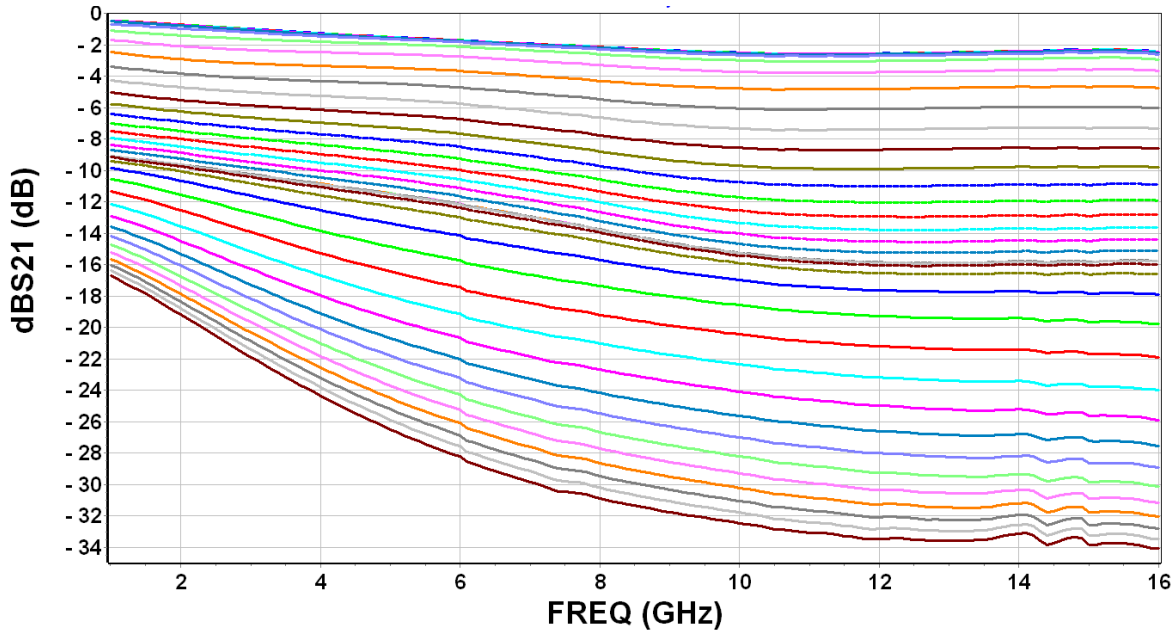
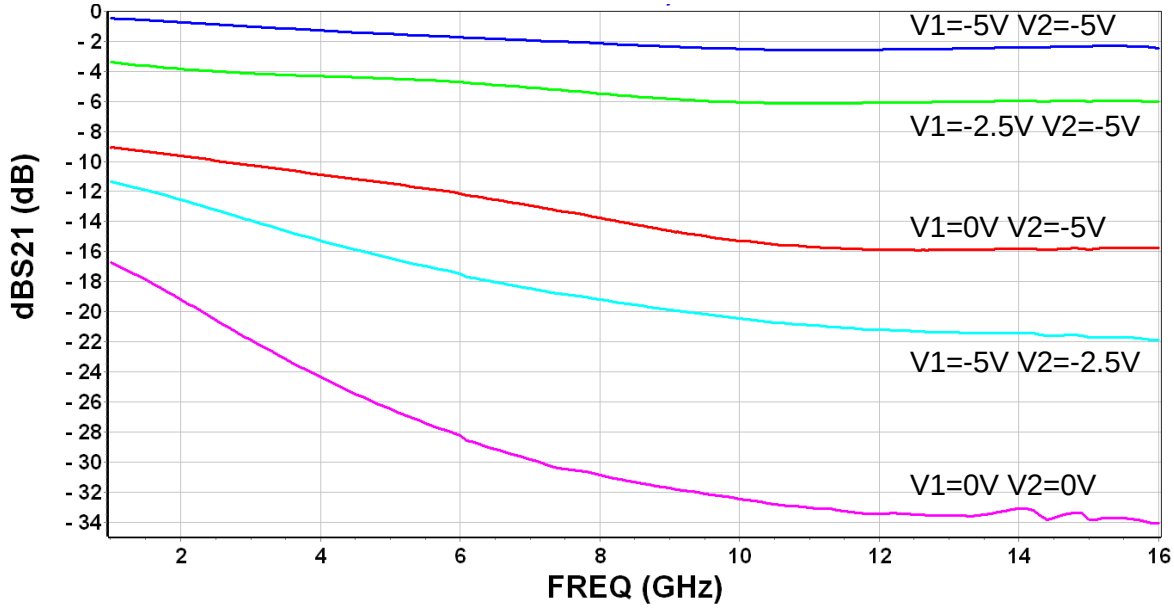
Typical Board Measurements

Temperature = +25°C, V1 = -5 to 0V with V2 = -5V and then V1 = 0V with V2 = -5V to 0V
Measurements in the package access planes

Attenuation versus Frequency (All dynamic range)



Min/Inter/Max attenuation versus Frequency



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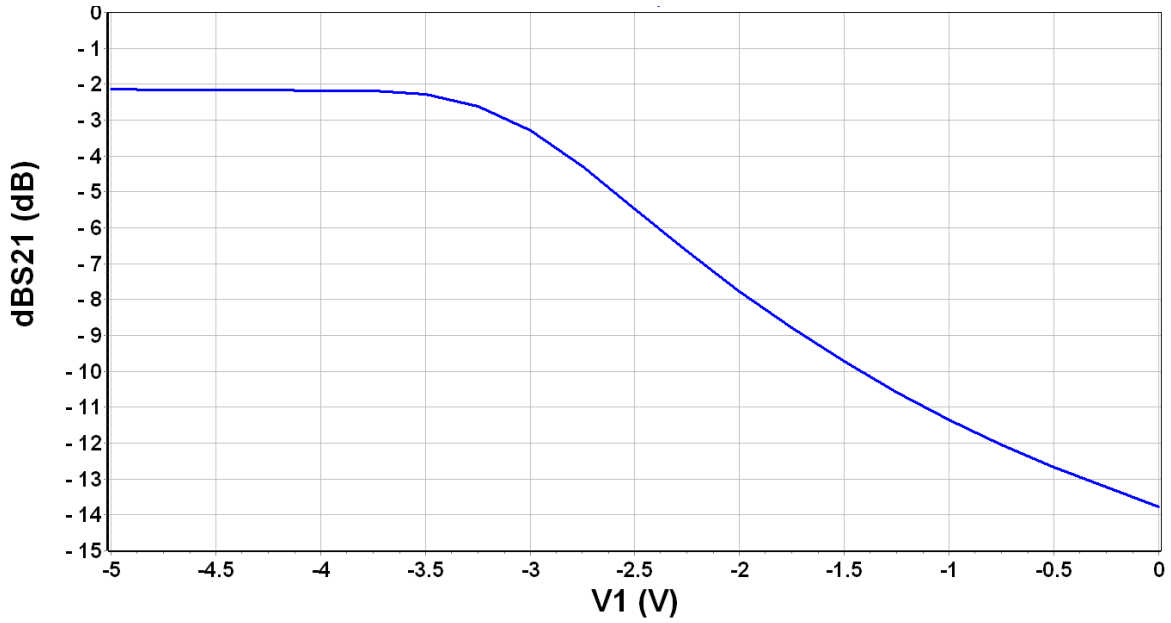
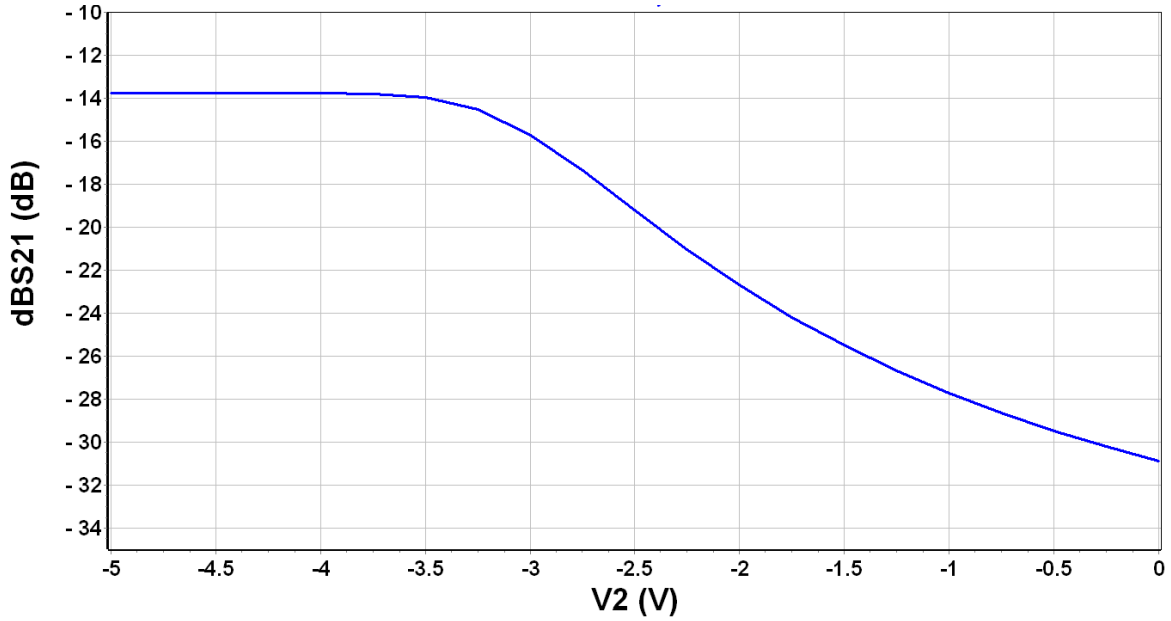
Typical Board Measurements

Temperature = +25°C, V1 = -5 to 0V with V2 = -5V and then V1 = 0V with V2 = -5V to 0V
Measurements in the package access planes

Attenuation control versus V1 @ 8GHz, V2 = -5V



Attenuation control versus V2 @ 8GHz, V1 = 0V



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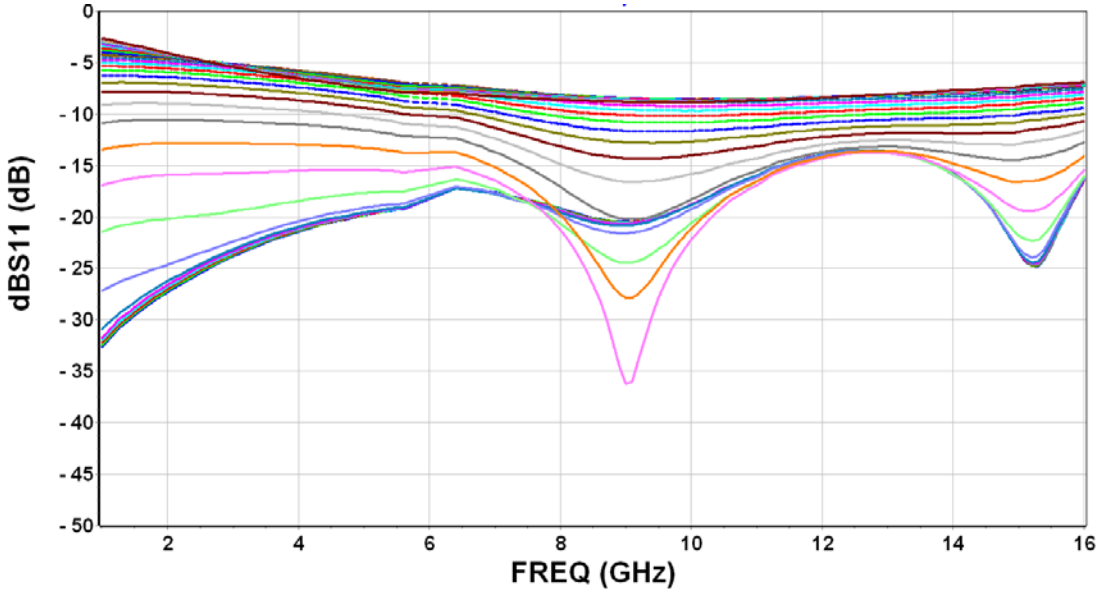
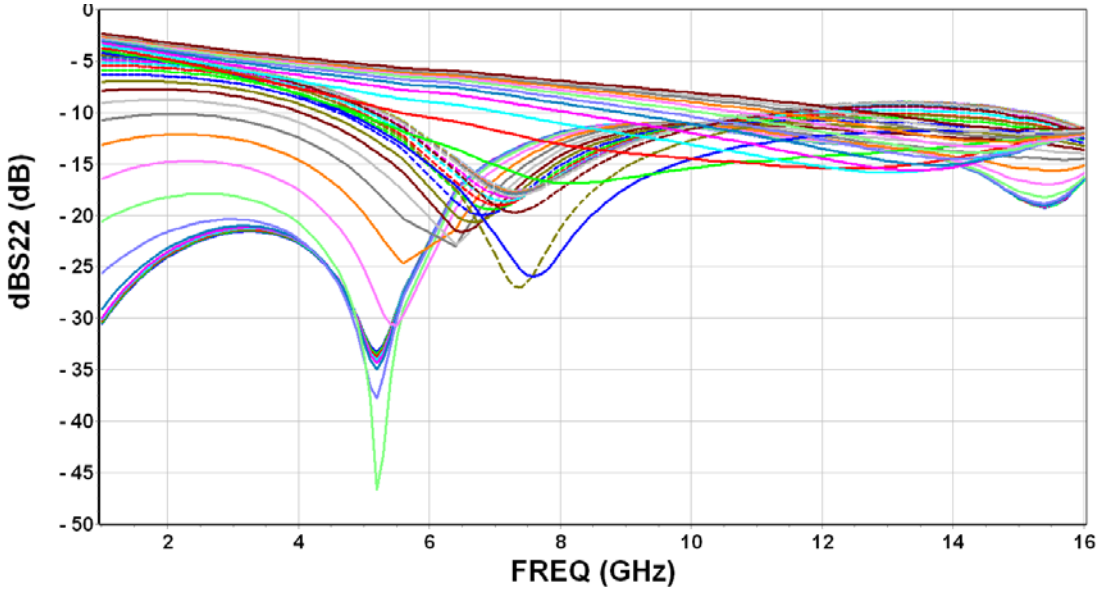
Typical Board Measurements

Temperature = +25°C, V1 = -5 to 0V with V2 = -5V and then V1 = 0V with V2 = -5V to 0V
Measurements in the package access planes

Input Return Loss versus Frequency



Output Return Loss versus Frequency



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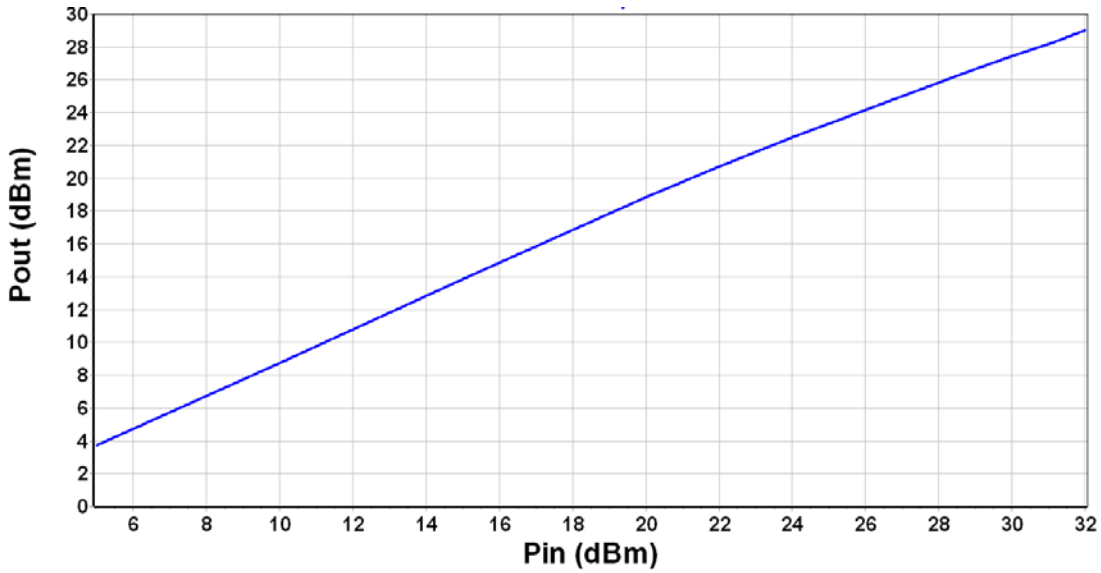
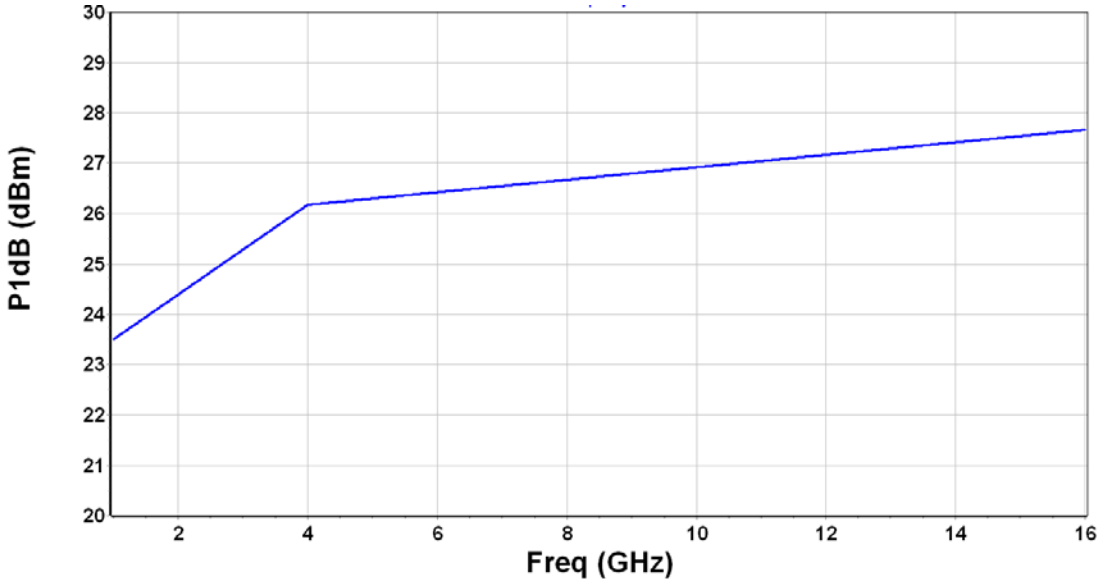
Typical Board Measurements

Temperature = +25°C, V1 = -5 to 0V with V2 = -5V and then V1 = 0V with V2 = -5V to 0V
Measurements in the package access planes

Output power versus Input power @4GHz and V1=V2=-5V



Output power @1dBc versus Frequency @V1=V2=-5V



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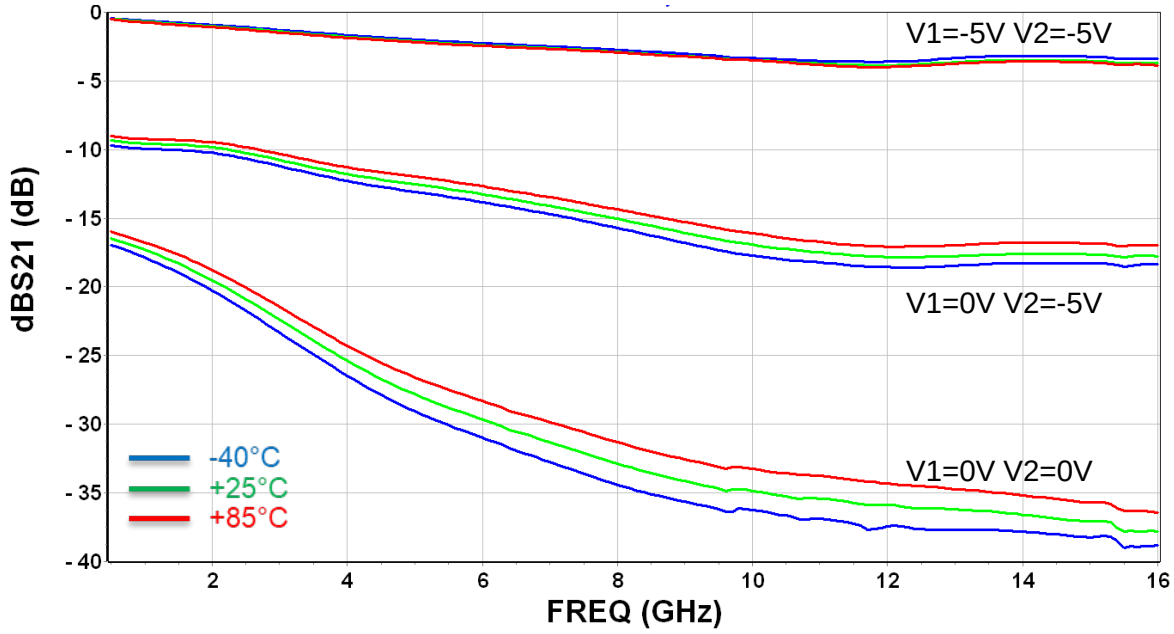
Typical Board Measurements

Temperature = -40, +25, +85°C
Measurements in the Board access planes

Min/Inter/Max attenuation versus Frequency



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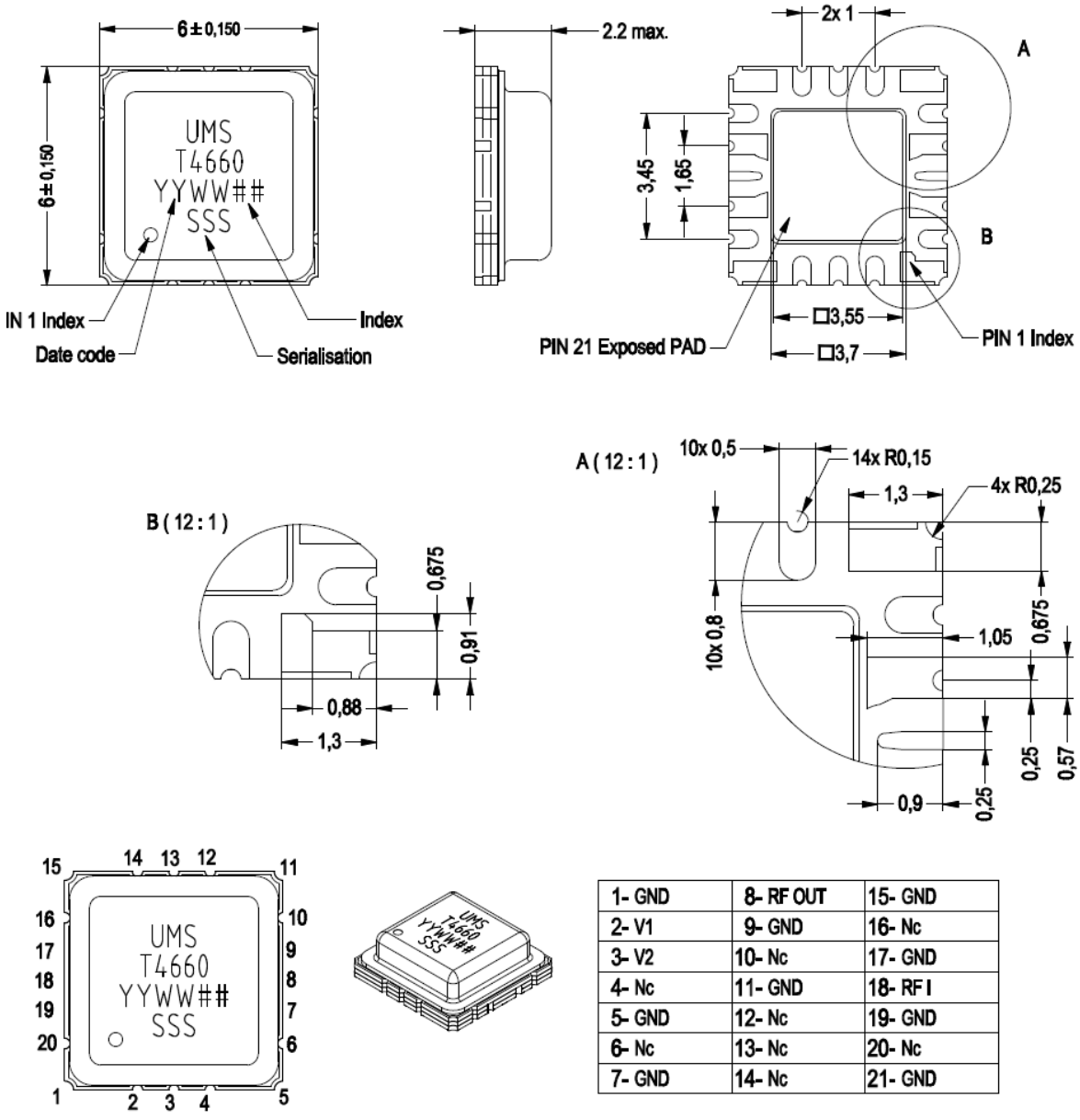
Package outline (1)



1- GND	8- RF OUT	15- GND
2- V1	9- GND	16- Nc
3- V2	10- Nc	17- GND
4- Nc	11- GND	18- RF I
5- GND	12- Nc	19- GND
6- Nc	13- Nc	20- Nc
7- GND	14- Nc	21- GND

All dimensions in mm

1. The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0024 (https://www.ums-rf.com) for exact package dimensions.
2. It is strongly recommended to ground all pins marked “GND” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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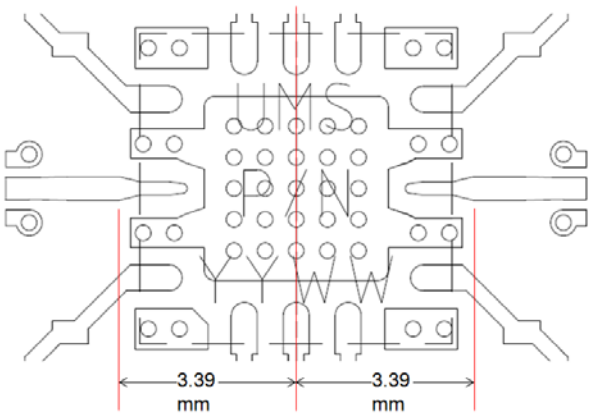
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.39mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".



Package Information

Parameter	Value
Package body material	RoHS-compliant
Lead finish	Gold
Hermetic sealing (fine leak compliant Mil-Std-883 Method 1014.10 Condition A4, tracer gas He at 1atm)	$1x10^{-8}$ ccHe/s/atm

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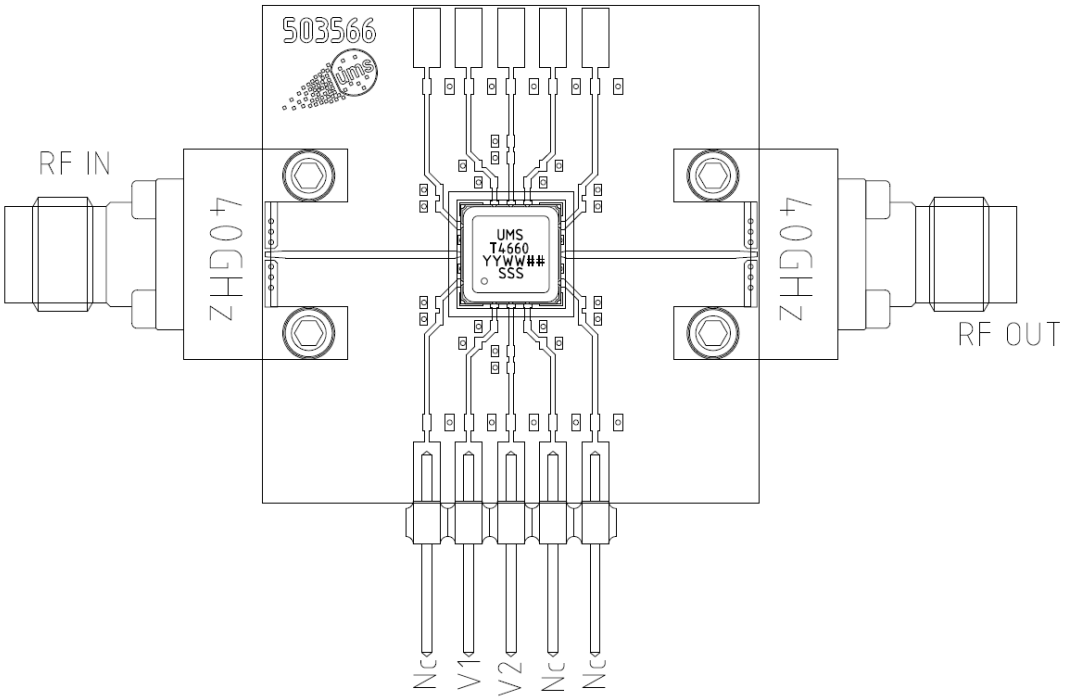
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- See application note AN0017 for details.



Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.

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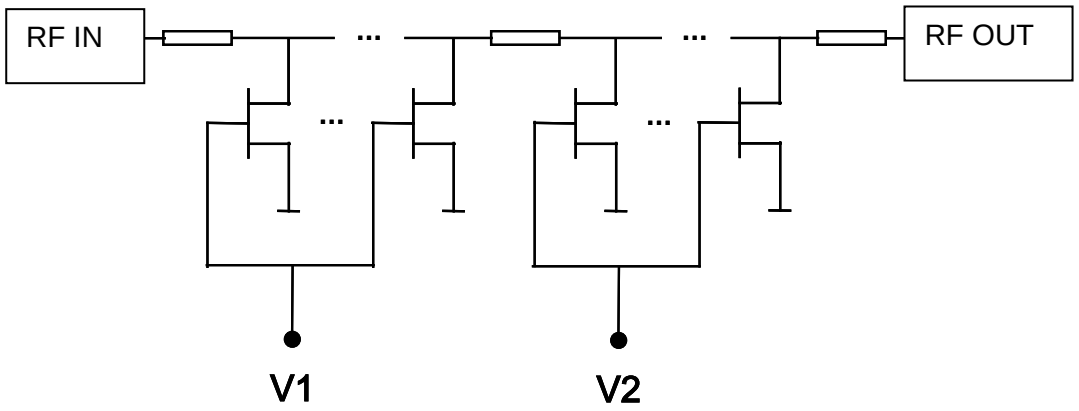
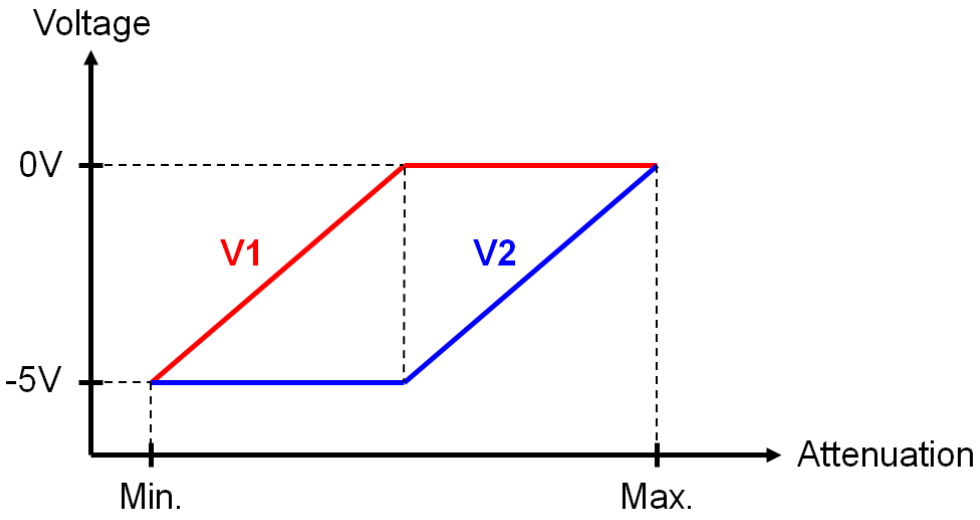
Biasing sequence

Optimum linearity performance of the VVA is achieved by first varying V1 control voltage of the 1st attenuation stage from -5V to 0V with V2 fixed at -5V.
The control voltage of the 2nd attenuation stage, V2, should then be varied from -5V to 0V, with V1 fixed at 0V.





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Recommended package footprint for FAB Package

Refer to the application note AN0024 available at https://www.ums-rf.com for package foot print recommendations and exact package dimensions.

SMD mounting procedure for FAB Package

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0024 available at https://www.ums-rf.com.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

FAB 6x6 package:	CHT4660-FAB/XY Waffle pack: XY = 24

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