DC-6GHz 6-BIT DIGITAL ATTENUATOR

GaAs Monolithic Microwave IC in SMD leadless package

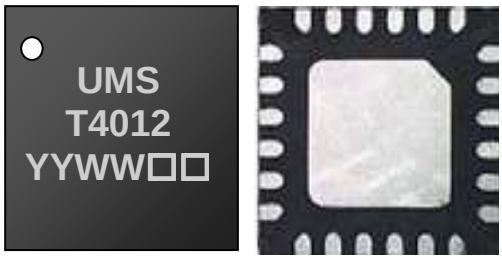
Description

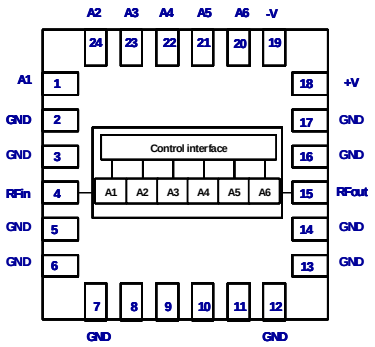
The CHT4012-QDG is a DC-6GHz monolithic 6-bit digital attenuator with a LSB = 0.5dB offering a high dynamic range and a high accuracy, the RMS amplitude error is typically as low as 0.3dB. The circuit provides low insertion loss 2.5dB associated to input and output return losses better than 13dB. A CMOS and TTL compatible interface is available on chip.

It is designed for a wide range of applications, from military to commercial communication systems.

The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

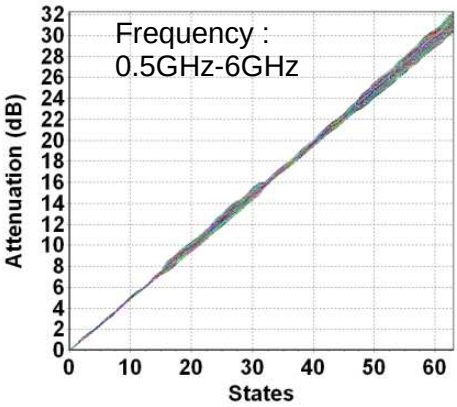
It is supplied in RoHS compliant SMD package.





Main Features

- Broadband performances: DC-6GHz
- Insertion Loss (state 0): 2.5dB
- RMS attenuation error: 0.3dB
- RMS phase variation: 1deg
- DC bias: V+=5V and V-=-5V
- No decoupling capacitance on Input and Output RF accesses
- 24L-QFN4x4
- MSL1



Main Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	DC		6	GHz
IL	Insertion Loss		2.5		dB
Rms_att_err	RMS of attenuation error		0.3		dB
Rms_phivar	RMS of phase variation (0.5 to 6GHz)		1		°

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Main Characteristics

Tamb.= +25℃

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	DC		6	GHz
IL	Insertion Loss		2.5		dB
S11	Input Return Loss		-15		dB
S22	Output Return Loss		-15		dB
P1dB	Input power at 1dB gain compression		20		dBm
Dyn	Dynamic		31.5		dB
LSB	Attenuator elementary step		0.5		dB
Att_err	Attenuation error		-0.7/0.4		dB
Rms_att_err	RMS attenuation error		0.3		dB
Phivar	Phase variation (0.5 to 6GHz)		-3/+2		°
Rms_phivar	RMS phase variation (0.5 to 6GHz)		1		°
Sw_t	Switching time		15		ns
V+	Positive supply voltage		5		V
V-	Negative supply voltage		-5		V
Vctrl_L	Control voltage low level		0	0.4	V
Vctrl_H	Control voltage high level	2.4		7	V
I_V+	Positive supply DC current		5		mA
I_V-	Negative supply DC current		5		mA

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

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Definitions

n: Attenuator state index with $0 \leq n \leq 63$
Phase_S21(n) : Measured phase of S21 in degree at attenuation state n
dB_S21(n) : Measured magnitude of S21 in dB at attenuation state n

Attenuation Error (Att_err)

Att_err(n)= dB_S21 (n) - dB_S21(0) –0.5xn (dB)

The translation of Att_err(n) from dB to linear is given by: Att_err_lin(n) = $10^{\frac{Att\_err(n)}{20}}$

Phase variation (Phivar)

Phivar(n) = Phase_S21(n) - Phase_S21(0) (°)

RMS Attenuation Error (Rms_att_err)

$$\text{Rms\_att\_err} = 20\log\left(1+\sqrt{\frac{1}{64}.\sum_{n=0}^{63}(1-Att\_err\_lin(n))^2}\right) \text{ (dB)}$$

RMS Phase variation (Rms_Phivar)

$$\text{Rms\_Phivar} = \sqrt{\frac{\sum_{n=0}^{63}(Phi\,\text{var}(n))^2}{64}} \text{ (°)}$$

Absolute Maximum Ratings

Tamb.= +25°C (1)

Symbol	Parameter	Values	Unit
V+	Maximum positive voltage	8V	V
V-	Minimum negative voltage	-8	V
Ai	CTRL voltage (Vctrl _low, Vctrl _high)	-2 to 8	V
Pin	Maximum Input power	23	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

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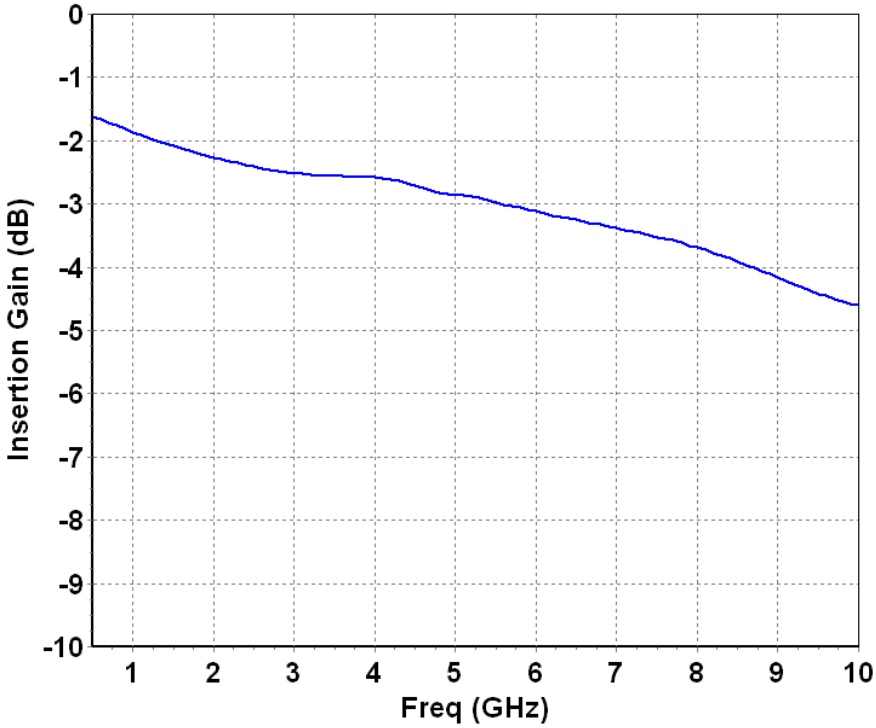
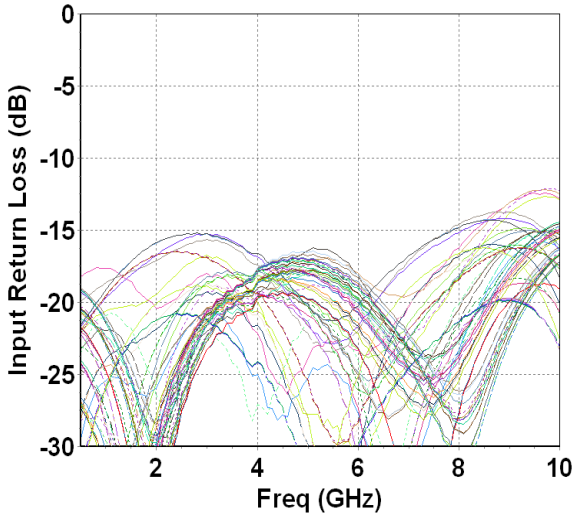
Typical Board Measurements

Tamb.= +25°C, V+ = +5V, V- = -5V

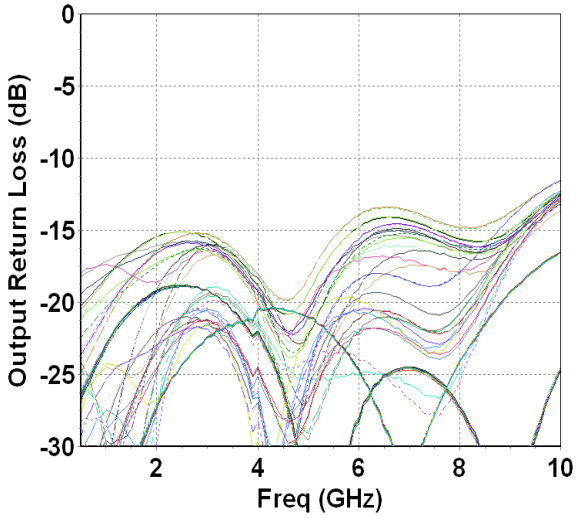
Insertion Loss (Attenuator state 0)



Input Return Loss
All States



Output Return Loss
All States



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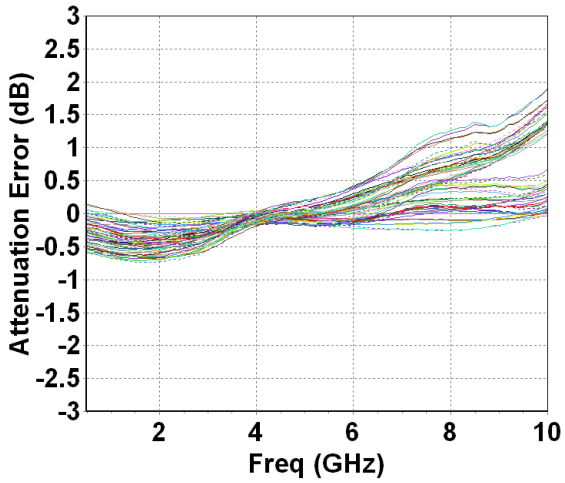
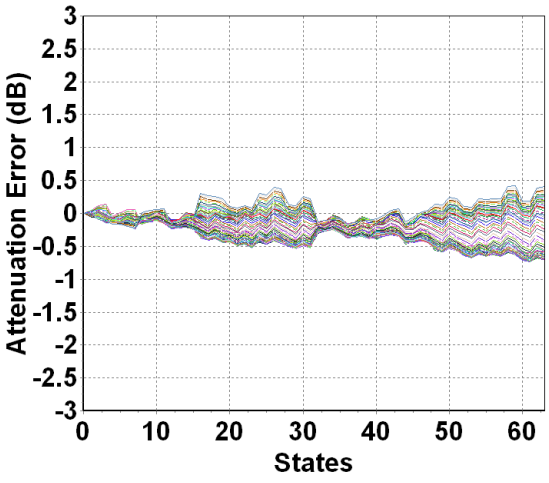
Typical Board Measurements

Tamb.= +25°C, V+ = +5V, V- = -5V

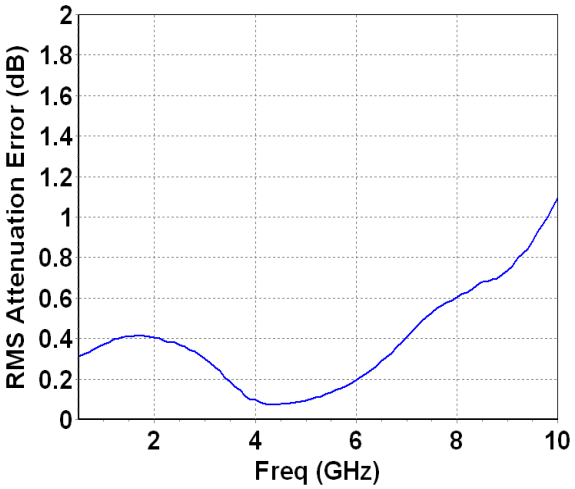
Attenuation Error versus Frequency



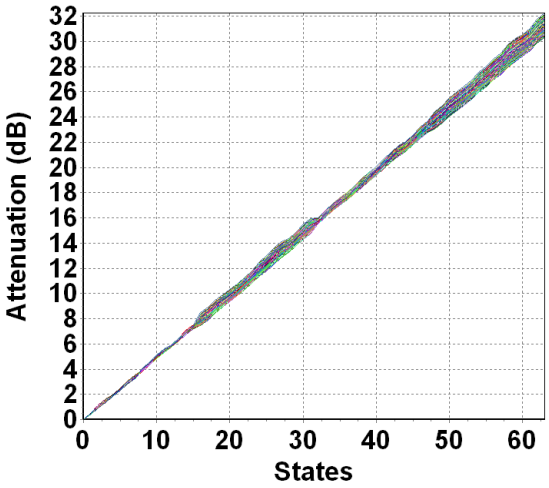
Attenuation Error versus States
0.5GHz < Frequency < 6Ghz



RMS Attenuation Error versus Frequency



Attenuation versus States
0.5GHz < Frequency < 6Ghz



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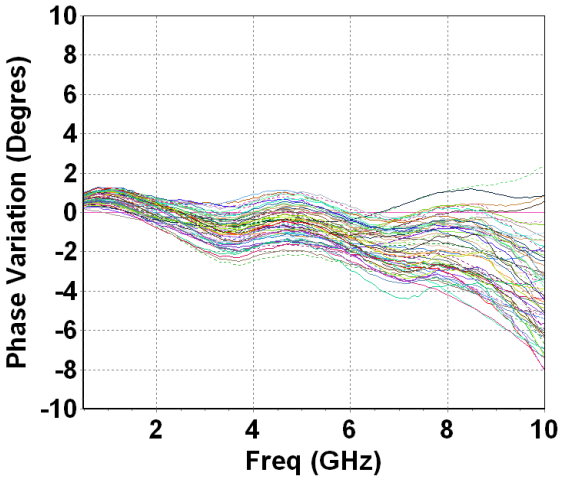
Typical Board Measurements

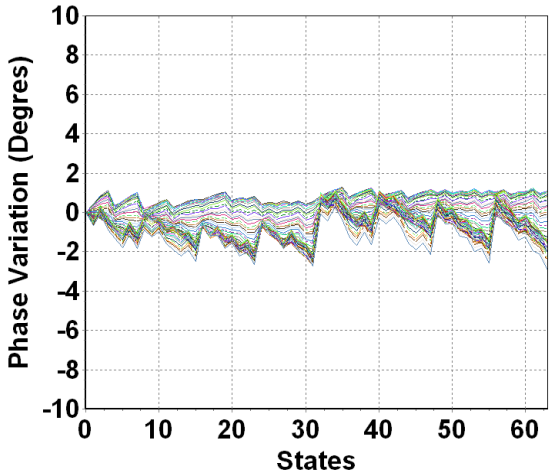
Tamb.= +25°C, V+ = +5V, V- = -5V

Phase Variation versus Frequency

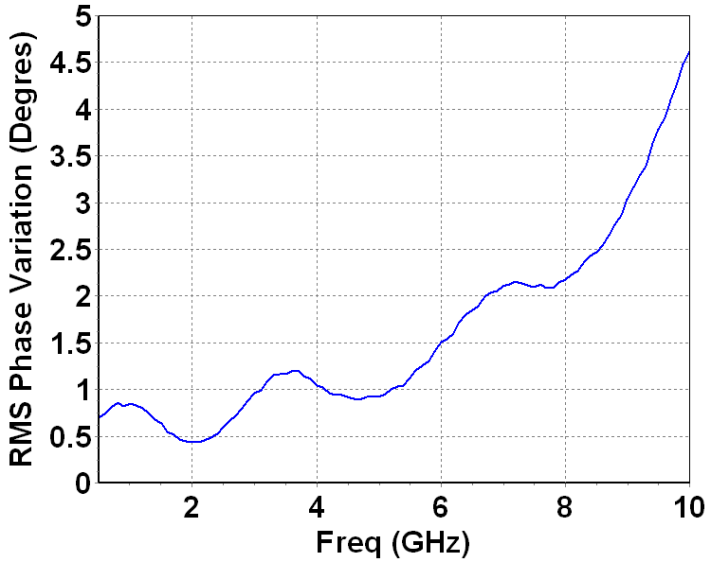


Phase Variation versus States

0.5GHz < Frequency < 6Ghz



RMS of Phase Variation versus Frequency



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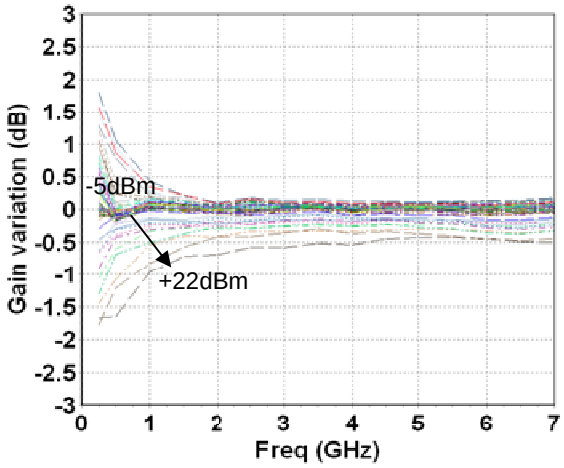
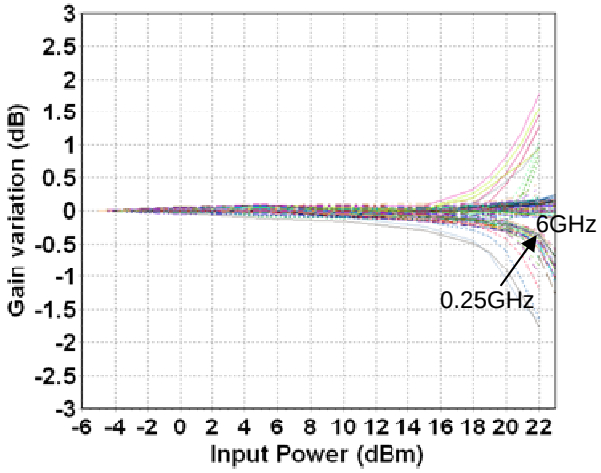
Typical Board Measurements

Tamb.= +25°C, V+ = +5V, V- = -5V

Variation of the Gain versus Frequency
Attenuator states : 0 / 1/ 2 / 4 / 8 / 16 / 32 / 63
Input power : -5 to 22dBm



Variation of the Gain versus Input Power
Attenuator states : 0 / 1/ 2 / 4 / 8 / 16 / 32 / 63
Frequency : 0.25GHz to 6GHz



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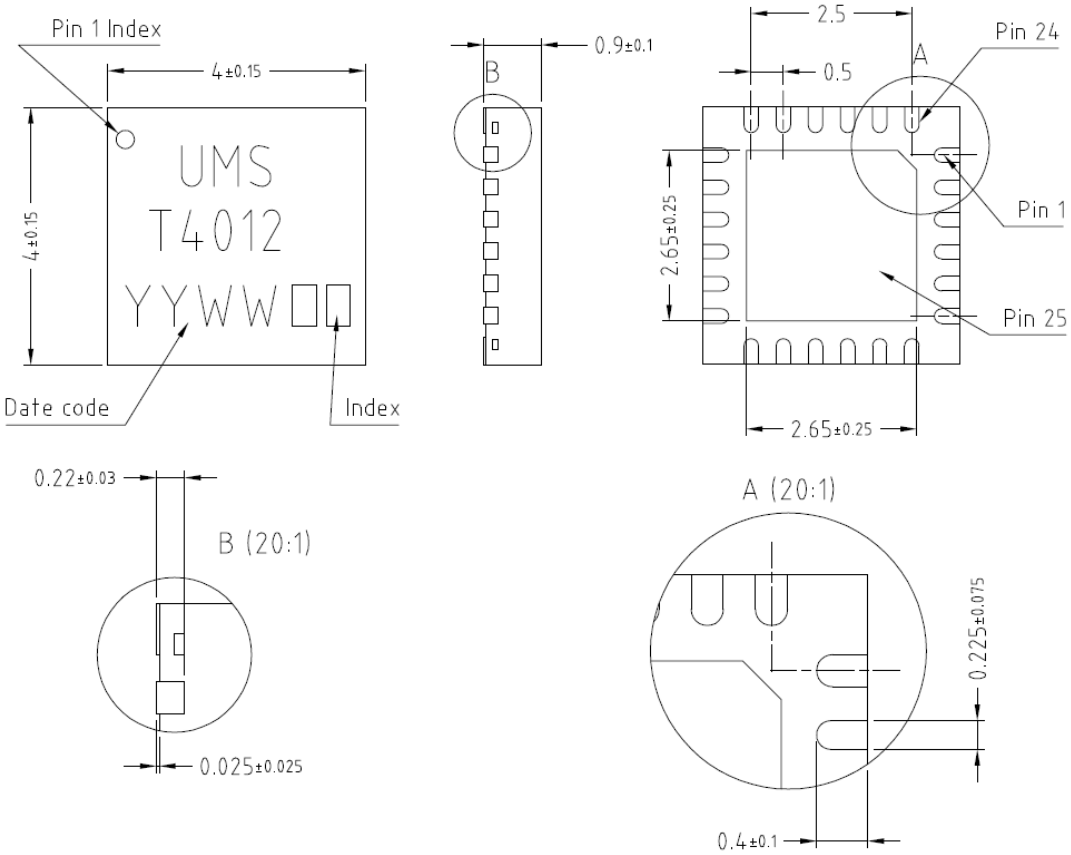
Package outline (1)



Matt tin, Lead Free (Green)	1- A1	9- Nc	17- Gnd(2)
Units : mm	2- Gnd(2)	10- Nc	18- V+
From the standard : JEDEC MO-220 (VGGD)	3- Gnd(2)	11- Nc	19- V-
	4- RF in	12- Gnd(2)	20- A6
25- GND	5- Gnd(2)	13- Gnd(2)	21- A5
	6- Gnd(2)	14- Gnd(2)	22- A4
	7- Gnd(2)	15- RF out	23- A3
	8- Nc	16- Gnd(2)	24- A2

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (http://www.ums-gaas.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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Biasing recommendations

Pin number	Pad name	Value
1	A1	0V / 3.3V or 0V / 5V
24	A2	0V / 3.3V or 0V / 5V
23	A3	0V / 3.3V or 0V / 5V
22	A4	0V / 3.3V or 0V / 5V
21	A5	0V / 3.3V or 0V / 5V
20	A6	0V / 3.3V or 0V / 5V
19	V-	-5V
18	V+	+5V

NOTE:

Control voltages of the attenuator bits are both CMOS and TTL compatible

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Attenuator control table

Voltage to apply on the pads A1 to A6:

state	Att (dB)	A6	A5	A4	A3	A2	A1	state	Att (dB)	A6	A5	A4	A3	A2	A1
0	0	0	0	0	0	0	0	33	16.5	3.3	0	0	0	0	3.3
1	0.5	0	0	0	0	0	3.3	34	17	3.3	0	0	0	3.3	0
2	1	0	0	0	0	3.3	0	35	17.5	3.3	0	0	0	3.3	3.3
3	1.5	0	0	0	0	3.3	3.3	36	18	3.3	0	0	3.3	0	0
4	2	0	0	0	3.3	0	0	37	18.5	3.3	0	0	3.3	0	3.3
5	2.5	0	0	0	3.3	0	3.3	38	19	3.3	0	0	3.3	3.3	0
6	3	0	0	0	3.3	3.3	0	39	19.5	3.3	0	0	3.3	3.3	3.3
7	3.5	0	0	0	3.3	3.3	3.3	40	20	3.3	0	3.3	0	0	0
8	4	0	0	3.3	0	0	0	41	20.5	3.3	0	3.3	0	0	3.3
9	4.5	0	0	3.3	0	0	3.3	42	21	3.3	0	3.3	0	3.3	0
10	5	0	0	3.3	0	3.3	0	43	21.5	3.3	0	3.3	0	3.3	3.3
11	5.5	0	0	3.3	0	3.3	3.3	44	22	3.3	0	3.3	3.3	0	0
12	6	0	0	3.3	3.3	0	0	45	22.5	3.3	0	3.3	3.3	0	3.3
13	6.5	0	0	3.3	3.3	0	3.3	46	23	3.3	0	3.3	3.3	3.3	0
14	7	0	0	3.3	3.3	3.3	0	47	23.5	3.3	0	3.3	3.3	3.3	3.3
15	7.5	0	0	3.3	3.3	3.3	3.3	48	24	3.3	3.3	0	0	0	0
16	8	0	3.3	0	0	0	0	49	24.5	3.3	3.3	0	0	0	3.3
17	8.5	0	3.3	0	0	0	3.3	50	25	3.3	3.3	0	0	3.3	0
18	9	0	3.3	0	0	3.3	0	51	25.5	3.3	3.3	0	0	3.3	3.3
19	9.5	0	3.3	0	0	3.3	3.3	52	26	3.3	3.3	0	3.3	0	0
20	10	0	3.3	0	3.3	0	0	53	26.5	3.3	3.3	0	3.3	0	3.3
21	10.5	0	3.3	0	3.3	0	3.3	54	27	3.3	3.3	0	3.3	3.3	0
22	11	0	3.3	0	3.3	3.3	0	55	27.5	3.3	3.3	0	3.3	3.3	3.3
23	11.5	0	3.3	0	3.3	3.3	3.3	56	28	3.3	3.3	3.3	0	0	0
24	12	0	3.3	3.3	0	0	0	57	28.5	3.3	3.3	3.3	0	0	3.3
25	12.5	0	3.3	3.3	0	0	3.3	58	29	3.3	3.3	3.3	0	3.3	0
26	13	0	3.3	3.3	0	3.3	0	59	29.5	3.3	3.3	3.3	0	3.3	3.3
27	13.5	0	3.3	3.3	0	3.3	3.3	60	30	3.3	3.3	3.3	3.3	0	0
28	14	0	3.3	3.3	3.3	0	0	61	30.5	3.3	3.3	3.3	3.3	0	3.3
29	14.5	0	3.3	3.3	3.3	0	3.3	62	31	3.3	3.3	3.3	3.3	3.3	0
30	15	0	3.3	3.3	3.3	3.3	0	63	31.5	3.3	3.3	3.3	3.3	3.3	3.3
31	15.5	0	3.3	3.3	3.3	3.3	3.3								
32	16	3.3	0	0	0	0	0								

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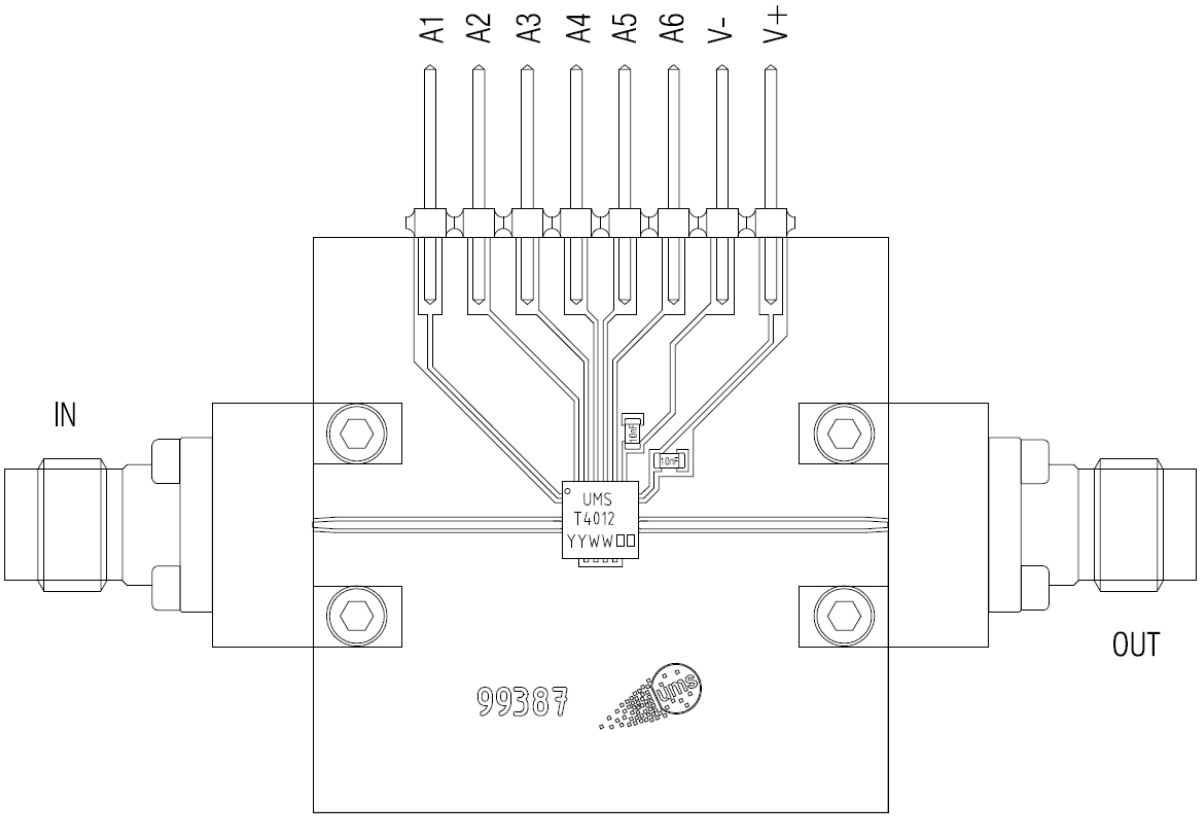
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for indicated DC accesses.
- See application note AN0017 for details.



Note

An external capacitance is requested to protect the device from any external DC voltage that might be present on the RF accesses.

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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

Refer to the application note AN0019 available at http://www.ums-gaas.com for environmental data on UMS package products.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x4 RoHS compliant package:	CHT4012-QDG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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