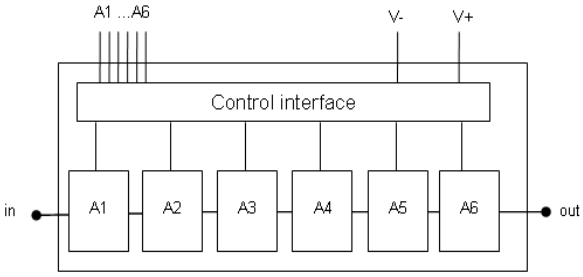
DC-6GHz 6-BIT DIGITAL ATTENUATOR

GaAs Monolithic Microwave IC

Description

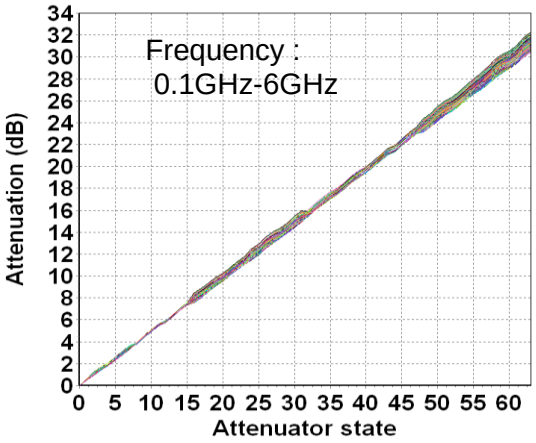
The CHT4012a98F is a DC-6GHz monolithic 6 bit digital attenuator with a LSB = 0.5dB offering a high dynamic range and a high accuracy, the RMS amplitude error is typically as low as 0.3dB. The circuit provides low insertion loss 2.5dB associated to input and output return losses better than 14dB. A CMOS and TTL compatible interface is available on chip.
The circuit is mainly dedicated to defence and space systems and is also well suited for a wide range of microwave applications and systems.



The circuit is manufactured with a pHEMT process, 0.25µm gate length and electron beam gate lithography.
It is available in chip form

Main Features

- Broadband performances: DC-6GHz
- Insertion Loss (state 0): 2.5dB
- RMS attenuation error: 0.3dB
- RMS phase variation: 1deg
- DC bias: V+=5V and V-=-5V
- No decoupling capacitance on Input and Output RF accesses
- Chip size 2.41x1.32x0.1mm



Main Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	DC		6	GHz
IL	Insertion Loss		2.5		dB
Rms_att_er	RMS of attenuation error		0.3		dB
Rms_phivar	RMS of phase variation (0.1 to 6GHz)		1		°

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Main Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Operating frequency	DC		6	GHz
IL	Insertion Loss		2.5		dB
S11	Input Return Loss		-16		dB
S22	Output Return Loss		-14		dB
P1dB	Input power at 1dB gain compression		20		dBm
Dyn	Dynamic		31.5		dB
LSB	Attenuator elementary step		0.5		dB
Att_er	Attenuation error		-0.5/+0.5		dB
Rms_att_er	RMS of attenuation error		0.3		dB
Phivar	Phase variation (0.1 to 6GHz)		-5 / +1		°
Rms_phivar	RMS of phase variation (0.1 to 6GHz)		1		°
Ts	Switching time		15		ns
V+	Positive supply voltage		5		V
V-	Negative supply voltage		-5	-4	V
Vctrl_L	Control voltage low level		0	0.4	V
Vctrl_H	Control voltage high level	2.4		7	V
I_V+	Positive supply DC current		5		mA
I_V-	Negative supply DC current		5		mA

These values are representative of measurements in test fixture

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Definitions

n: Attenuator state index with 0 ≤ n ≤ 63
Phase_S21(n): Measured phase of S21 in degree at attenuation state n
dB_S21(n): Measured magnitude of S21 in dB at attenuation state n

Attenuation Error (Att_err)

Att_err(n)= dB_S21 (n) - dB_S21(0) –0.5xn (dB)

The translation of Att_err(i) from dB to linear is given by: Att_err_lin(n) = $10^{\frac{Att\_err(n)}{20}}$

Phase variation (Phivar)

Phivar(n) = Phase_S21(n) - Phase_S21(0) (°)

RMS Attenuation Error (Rms_att)

Rms_att = $20\log\left(1+\sqrt{\frac{1}{64}.\sum_{n=0}^{63}(1-Att\_err\_lin(n))^2}\right)$ (dB)

RMS Phase variation (Rms_Phivar)

Rms_Phivar = $\sqrt{\frac{\sum_{n=0}^{63}(Phi\,\mathrm{var}(n))^2}{64}}$ (°)

Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
V+	Maximum positive bias voltage	8	V
V-	Minimum negative bias voltage	-8	V
Ai	CTRL voltage (Vctrl _low, Vctrl _high)	-2, 8	V
Pin	Maximum Input power	23	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

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Typical on-wafer Sij parameters at State 0

Tamb.= +25°C, V+ = +5V, V-=-5V

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
0.2	-20.21	0.1	-1.69	-5.6	-1.69	-5.6	-20.37	-0.3
0.4	-20.33	-9.2	-1.75	-9.9	-1.75	-9.9	-20.27	-8.8
0.6	-20.90	-20.2	-1.81	-14.2	-1.82	-14.1	-20.25	-18.0
0.8	-20.77	-32.0	-1.87	-18.3	-1.88	-18.3	-19.96	-27.4
1.0	-20.75	-40.7	-1.90	-22.5	-1.90	-22.6	-19.67	-35.5
1.2	-20.45	-48.7	-1.93	-26.7	-1.94	-26.8	-19.33	-41.9
1.4	-20.59	-54.5	-1.97	-30.9	-1.98	-31.0	-19.26	-48.4
1.6	-20.92	-61.5	-2.03	-35.2	-2.04	-35.3	-19.21	-55.4
1.8	-21.15	-69.9	-2.07	-39.4	-2.07	-39.6	-19.08	-60.8
2.0	-21.24	-77.4	-2.11	-43.7	-2.11	-43.8	-18.96	-65.8
2.2	-21.34	-84.7	-2.15	-47.8	-2.15	-47.8	-18.86	-70.0
2.4	-21.48	-90.7	-2.21	-52.0	-2.21	-52.1	-18.60	-74.1
2.6	-21.80	-94.9	-2.25	-56.1	-2.25	-56.3	-18.46	-78.1
2.8	-22.62	-100.6	-2.30	-60.3	-2.30	-60.4	-18.30	-81.8
3.0	-23.17	-106.8	-2.35	-64.5	-2.35	-64.6	-18.26	-84.9
3.2	-23.97	-113.1	-2.40	-68.7	-2.40	-68.7	-18.19	-88.0
3.4	-24.56	-120.1	-2.44	-72.8	-2.44	-72.9	-17.92	-90.8
3.6	-25.40	-123.3	-2.49	-76.9	-2.49	-76.9	-17.75	-93.7
3.8	-26.78	-125.4	-2.54	-81.0	-2.54	-81.1	-17.59	-95.7
4.0	-28.80	-125.6	-2.59	-85.1	-2.60	-85.2	-17.52	-97.8
4.2	-31.95	-128.2	-2.62	-89.3	-2.63	-89.3	-17.34	-99.0
4.4	-35.79	-128.9	-2.69	-93.4	-2.69	-93.5	-17.22	-100.4
4.6	-42.02	-100.1	-2.74	-97.6	-2.72	-97.6	-17.00	-101.1
4.8	-42.57	-39.9	-2.79	-101.7	-2.79	-101.8	-16.68	-102.1
5.0	-34.86	-19.8	-2.84	-105.9	-2.84	-105.9	-16.44	-103.6
5.2	-30.17	-9.9	-2.89	-109.9	-2.90	-110.1	-16.17	-104.5
5.4	-27.13	-7.3	-2.96	-114.1	-2.95	-114.1	-16.03	-105.6
5.6	-24.54	-5.9	-3.03	-118.3	-3.02	-118.4	-15.72	-107.0
5.8	-22.91	-7.6	-3.07	-122.5	-3.08	-122.6	-15.40	-108.7
6.0	-21.40	-11.8	-3.14	-126.6	-3.14	-126.6	-15.05	-109.6
6.2	-20.12	-17.1	-3.21	-130.6	-3.21	-130.8	-14.69	-111.4
6.4	-18.82	-22.2	-3.28	-134.8	-3.27	-134.9	-14.38	-112.5
6.6	-17.69	-24.7	-3.35	-138.9	-3.35	-139.1	-14.00	-114.3
6.8	-16.78	-28.2	-3.41	-143.1	-3.41	-143.1	-13.77	-116.3
7.0	-16.01	-30.9	-3.49	-147.2	-3.49	-147.3	-13.35	-117.8
7.2	-15.35	-34.9	-3.56	-151.4	-3.56	-151.4	-13.05	-120.4
7.4	-14.54	-38.7	-3.65	-155.5	-3.63	-155.6	-12.73	-122.3
7.6	-13.93	-42.1	-3.71	-159.5	-3.71	-159.6	-12.36	-124.7
7.8	-13.18	-46.1	-3.77	-163.6	-3.77	-163.8	-12.13	-127.3
8.0	-12.71	-48.8	-3.87	-167.8	-3.87	-168.0	-11.82	-129.9

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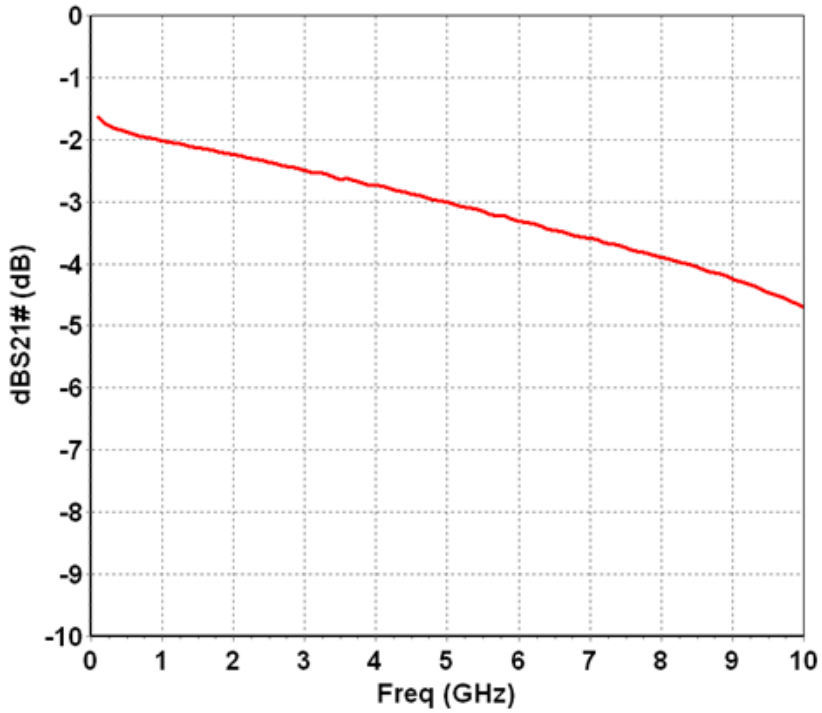
Typical Measurements in test fixture:

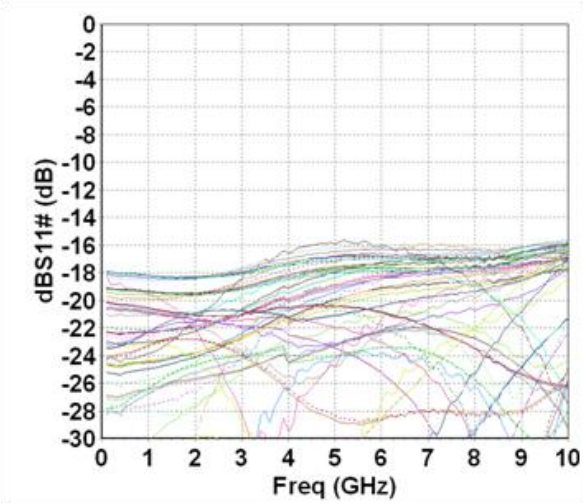
[S] parameters

T= +25°C, V+ = +5V, V- = -5V

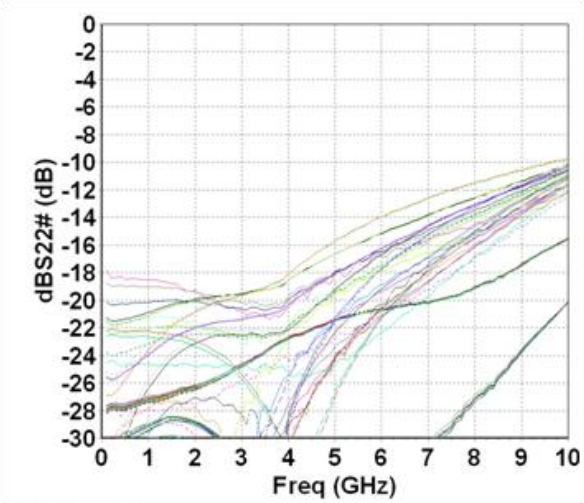
S21 versus Frequency
Attenuator state 0



S11 versus Frequency
All attenuator states



S22 versus Frequency
All attenuator states



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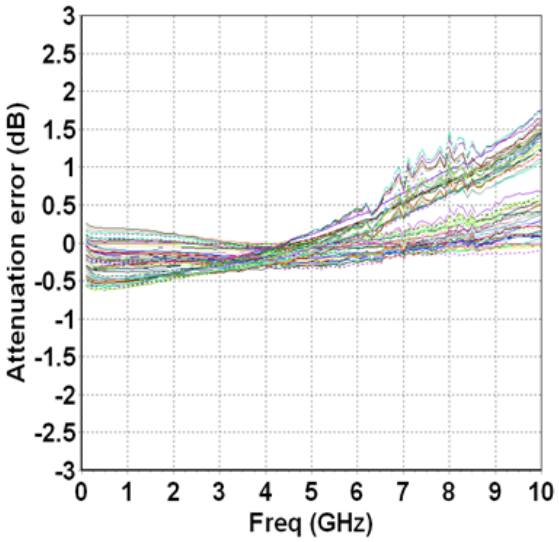
Typical Measurements in test fixture:

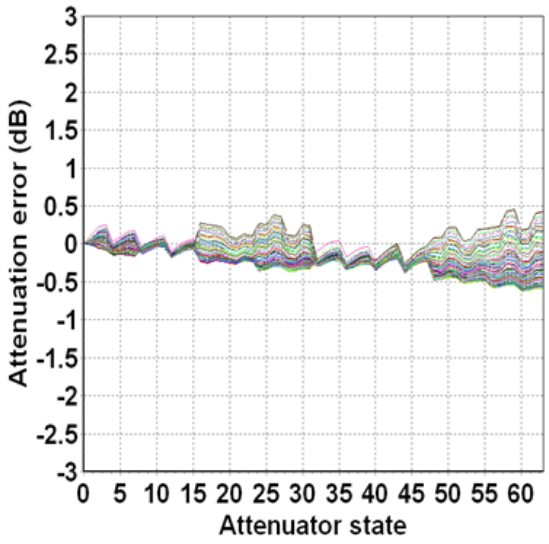
Attenuator performances: Attenuation error

T= +25°C, V+ = +5V, V- = -5V

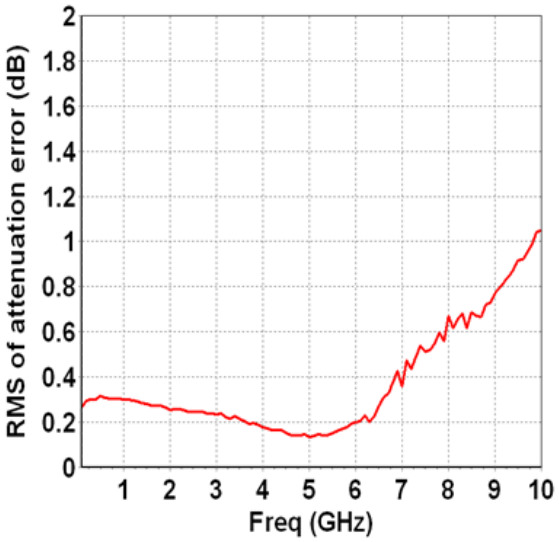
Attenuation error versus frequency
All attenuator states



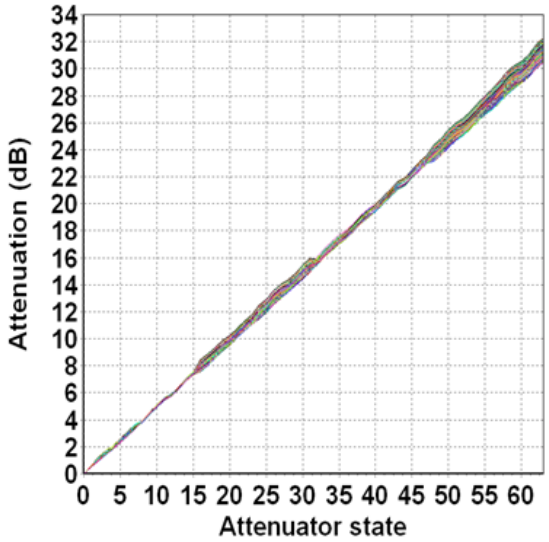
Attenuation error versus Attenuator state
0.1GHz < Freq. < 6GHz



RMS Attenuation error



Attenuation versus Attenuator state
0.1GHz < Freq. < 6GHz



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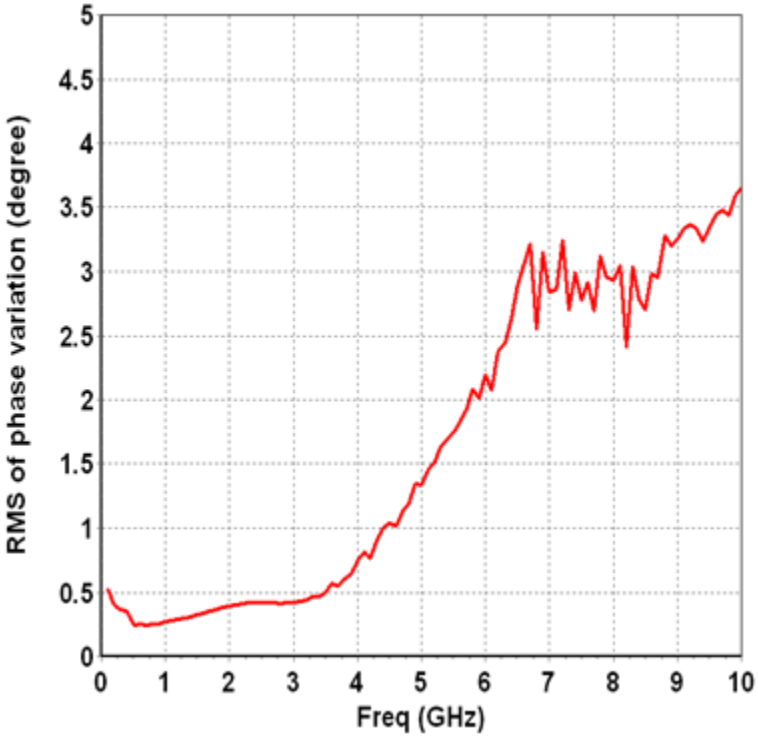
Typical Measurements in test fixture:

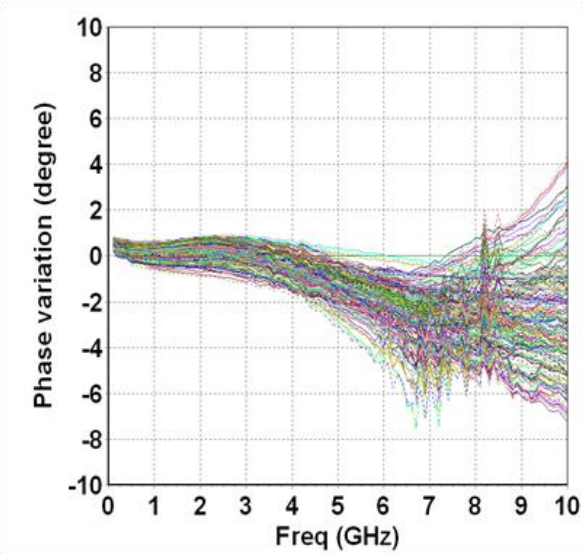
Attenuator performances: Phase variation

T= +25°C, V+ = +5V, V- = -5V

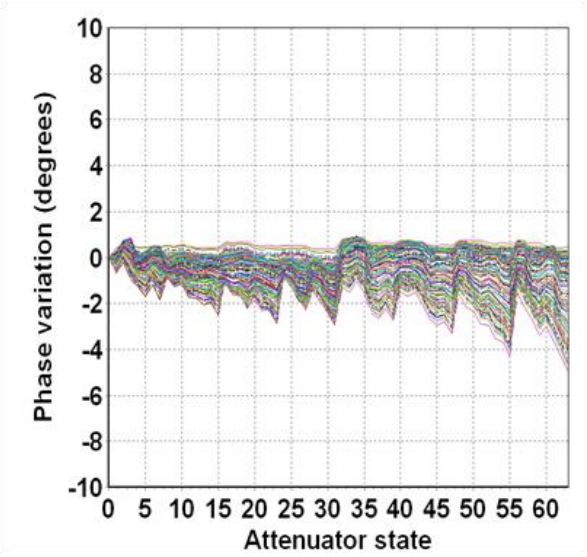
RMS of Phase variation



Phase variation versus Frequency
All attenuator states



Phase variation versus Attenuator state
0.1GHz < Freq. < 6GHz



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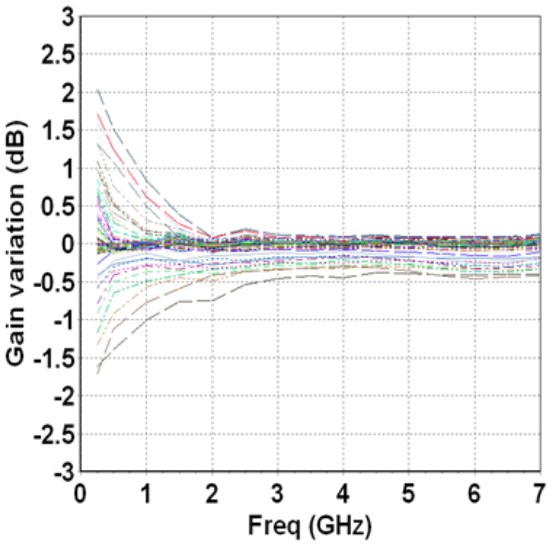
Typical Measurements in test fixture:

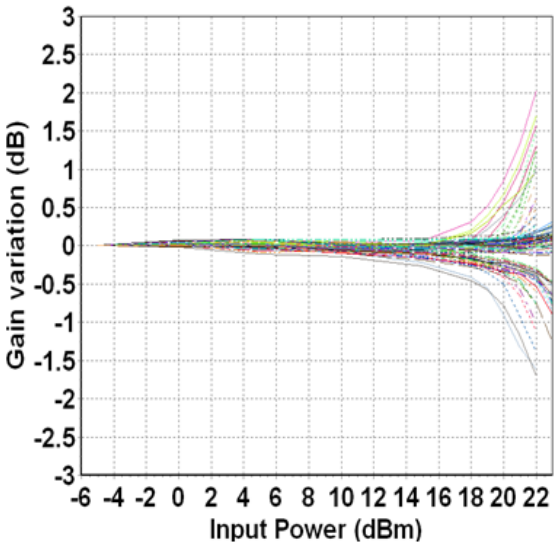
Attenuator performances: Phase variation

T= +25°C, V+ = +5V, V- = -5V

Variation of the Gain versus Frequency
Attenuator states: 0 / 1/ 2 / 4 / 8 / 16 / 32 / 63
Input power: -5 to 22dBm



Variation of the gain versus Input power
Attenuator states: 0 / 1/ 2 / 4 / 8 / 16 / 32 / 63
Frequency: 0.25GHz to 6GHz



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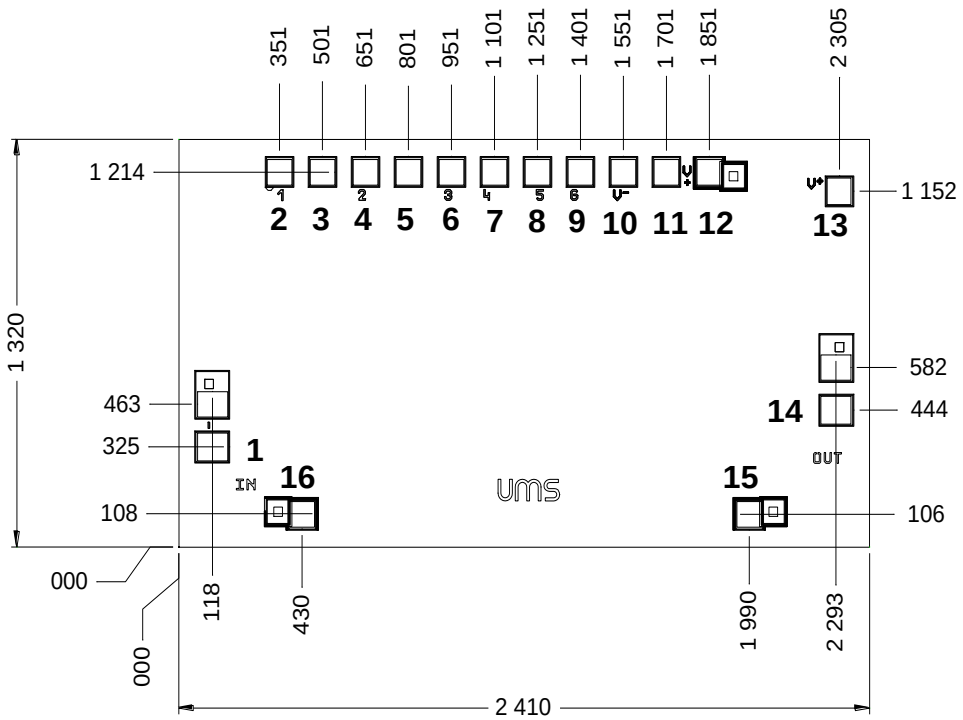
Mechanical dimensions and pad allocation



Chip thickness = 100µm +/- 10µm.
RF pads (1, 14) = 122 x 100µm²
DC and control pads (2, 4, 6, 7, 8, 9, 10, 13, 12, 15, 16) = 100 x 100µm²

Pin number	Pad name	Description
1	IN	Input RF:
2	A1	Attenuator bit 1
4	A2	Attenuator bit 2
6	A3	Attenuator bit 3
7	A4	Attenuator bit 4
8	A5	Attenuator bit 5
9	A6	Attenuator bit 6
10	V-	-5V supply voltage: interface
13	V+	+5V supply voltage: interface (1)
14	OUT	Output RF
3, 5		NC
11	V+	NC (1)
12, 15, 16	GND	NC

(1) Pin n°11 is internally connected to Pin n°13. Each one of these pins can be indifferently used to supply the control interface with +5V

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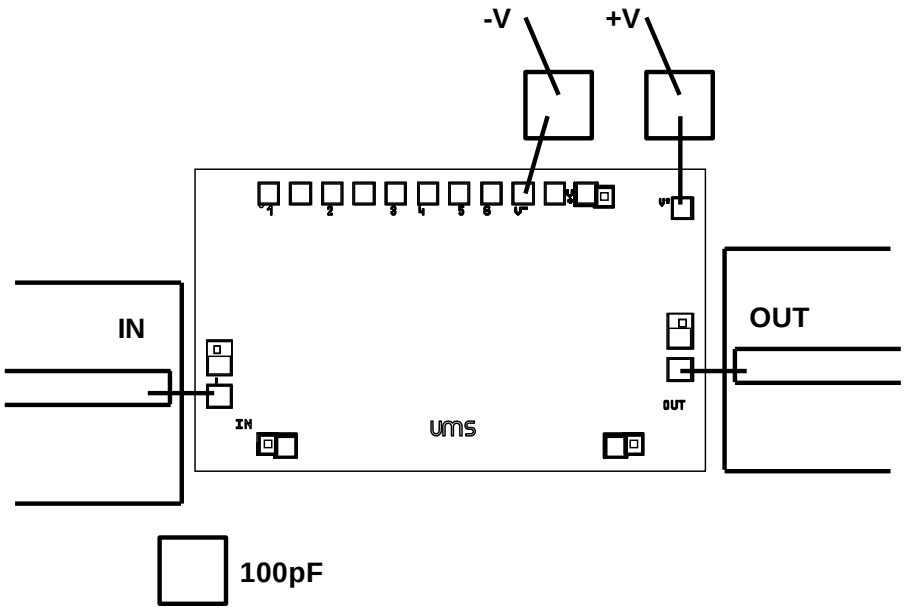
Bonding recommendations

Port	Connection
IN (1) OUT (14)	Inductance (Lbonding) = 0.3nH one wire: diameter 25µm, length 0.4mm
DC and Interface pads	Inductance (Lbonding) = 0.8nH one wire: diameter 25µm, length 1.0mm

Recommended assembly diagram



Note:

An external capacitance is requested to protect the device from any external DC voltage that might be present on the RF accesses.

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Bonding recommendations

Pin number	Pad name	Value
2	A1	0V / 3.3V or 0V / 5V
4	A2	0V / 3.3V or 0V / 5V
6	A3	0V / 3.3V or 0V / 5V
7	A4	0V / 3.3V or 0V / 5V
8	A5	0V / 3.3V or 0V / 5V
9	A6	0V / 3.3V or 0V / 5V
10	V-	-5V
13	V+	+5V

NOTE:

Control voltages of the attenuator bits are both CMOS and TTL compatible

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Attenuator control table

Voltage to apply on the pads A1 to A6:

state	Att (dB)	A6	A5	A4	A3	A2	A1	state	Att (dB)	A6	A5	A4	A3	A2	A1
0	0	0	0	0	0	0	0	33	16.5	3.3	0	0	0	0	3.3
1	0.5	0	0	0	0	0	3.3	34	17	3.3	0	0	0	3.3	0
2	1	0	0	0	0	3.3	0	35	17.5	3.3	0	0	0	3.3	3.3
3	1.5	0	0	0	0	3.3	3.3	36	18	3.3	0	0	3.3	0	0
4	2	0	0	0	3.3	0	0	37	18.5	3.3	0	0	3.3	0	3.3
5	2.5	0	0	0	3.3	0	3.3	38	19	3.3	0	0	3.3	3.3	0
6	3	0	0	0	3.3	3.3	0	39	19.5	3.3	0	0	3.3	3.3	3.3
7	3.5	0	0	0	3.3	3.3	3.3	40	20	3.3	0	3.3	0	0	0
8	4	0	0	3.3	0	0	0	41	20.5	3.3	0	3.3	0	0	3.3
9	4.5	0	0	3.3	0	0	3.3	42	21	3.3	0	3.3	0	3.3	0
10	5	0	0	3.3	0	3.3	0	43	21.5	3.3	0	3.3	0	3.3	3.3
11	5.5	0	0	3.3	0	3.3	3.3	44	22	3.3	0	3.3	3.3	0	0
12	6	0	0	3.3	3.3	0	0	45	22.5	3.3	0	3.3	3.3	0	3.3
13	6.5	0	0	3.3	3.3	0	3.3	46	23	3.3	0	3.3	3.3	3.3	0
14	7	0	0	3.3	3.3	3.3	0	47	23.5	3.3	0	3.3	3.3	3.3	3.3
15	7.5	0	0	3.3	3.3	3.3	3.3	48	24	3.3	3.3	0	0	0	0
16	8	0	3.3	0	0	0	0	49	24.5	3.3	3.3	0	0	0	3.3
17	8.5	0	3.3	0	0	0	3.3	50	25	3.3	3.3	0	0	3.3	0
18	9	0	3.3	0	0	3.3	0	51	25.5	3.3	3.3	0	0	3.3	3.3
19	9.5	0	3.3	0	0	3.3	3.3	52	26	3.3	3.3	0	3.3	0	0
20	10	0	3.3	0	3.3	0	0	53	26.5	3.3	3.3	0	3.3	0	3.3
21	10.5	0	3.3	0	3.3	0	3.3	54	27	3.3	3.3	0	3.3	3.3	0
22	11	0	3.3	0	3.3	3.3	0	55	27.5	3.3	3.3	0	3.3	3.3	3.3
23	11.5	0	3.3	0	3.3	3.3	3.3	56	28	3.3	3.3	3.3	0	0	0
24	12	0	3.3	3.3	0	0	0	57	28.5	3.3	3.3	3.3	0	0	3.3
25	12.5	0	3.3	3.3	0	0	3.3	58	29	3.3	3.3	3.3	0	3.3	0
26	13	0	3.3	3.3	0	3.3	0	59	29.5	3.3	3.3	3.3	0	3.3	3.3
27	13.5	0	3.3	3.3	0	3.3	3.3	60	30	3.3	3.3	3.3	3.3	0	0
28	14	0	3.3	3.3	3.3	0	0	61	30.5	3.3	3.3	3.3	3.3	0	3.3
29	14.5	0	3.3	3.3	3.3	0	3.3	62	31	3.3	3.3	3.3	3.3	3.3	0
30	15	0	3.3	3.3	3.3	3.3	0	63	31.5	3.3	3.3	3.3	3.3	3.3	3.3
31	15.5	0	3.3	3.3	3.3	3.3	3.3								
32	16	3.3	0	0	0	0	0								

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Note

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Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS products.

Ordering Information

Chip form:	CHT4012a98F/00

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