United Monolithic Semiconductors

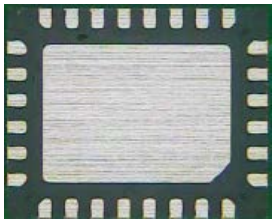
CHC2442-QPG

24GHz ISM SENSOR

Monolithic Microwave IC in SMD leadless package

Description

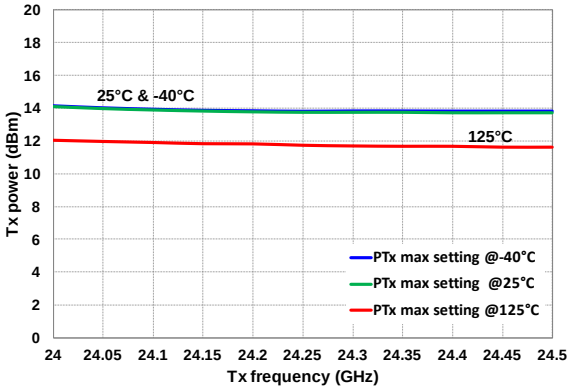
The CHC2442-QPG is a multifunction chip which integrates a low phase noise VCO, Tx MPA, two double balanced mixer based Rx and a switchable prescaler. The circuit is controlled by SPI and monitored with power and temperature sensor.
It is designed for signal generation and reception for automotive radar applications.
It is supplied in RoHS compliant SMD package.



Main Features

- Frequency Band: 24-24.5GHz
- >13dBm Max Tx Power
- 12dB Tx Power control range
- 37dB Rx gain
- 24dB Rx gain control range
- 11dB Rx SSB NF @ IF≥100kHz, max RF gain
- -16dBm IP1dB RF power @ min RF VGA gain
- Temperature range from -40°C to +125°C
- DC bias: 3.3V / 205-225mA @ Pout @ stage 8-0
- 28L-QFN4X5 SMD leadless package
- MSL1

Tx maximum output power over full temperature range



Main Electrical Characteristics

Tcase= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	24		24.5	GHz
Gain	Voltage gain (Nom RF & IF gain)		37		dB
NF	Noise Figure SSB (Nom RF & IF gain)		11.5		dB
Pout	Output Power (max setting)		>13		dBm
CP1dB	IP1dB compression point (Nom RF gain)		-18		dBm

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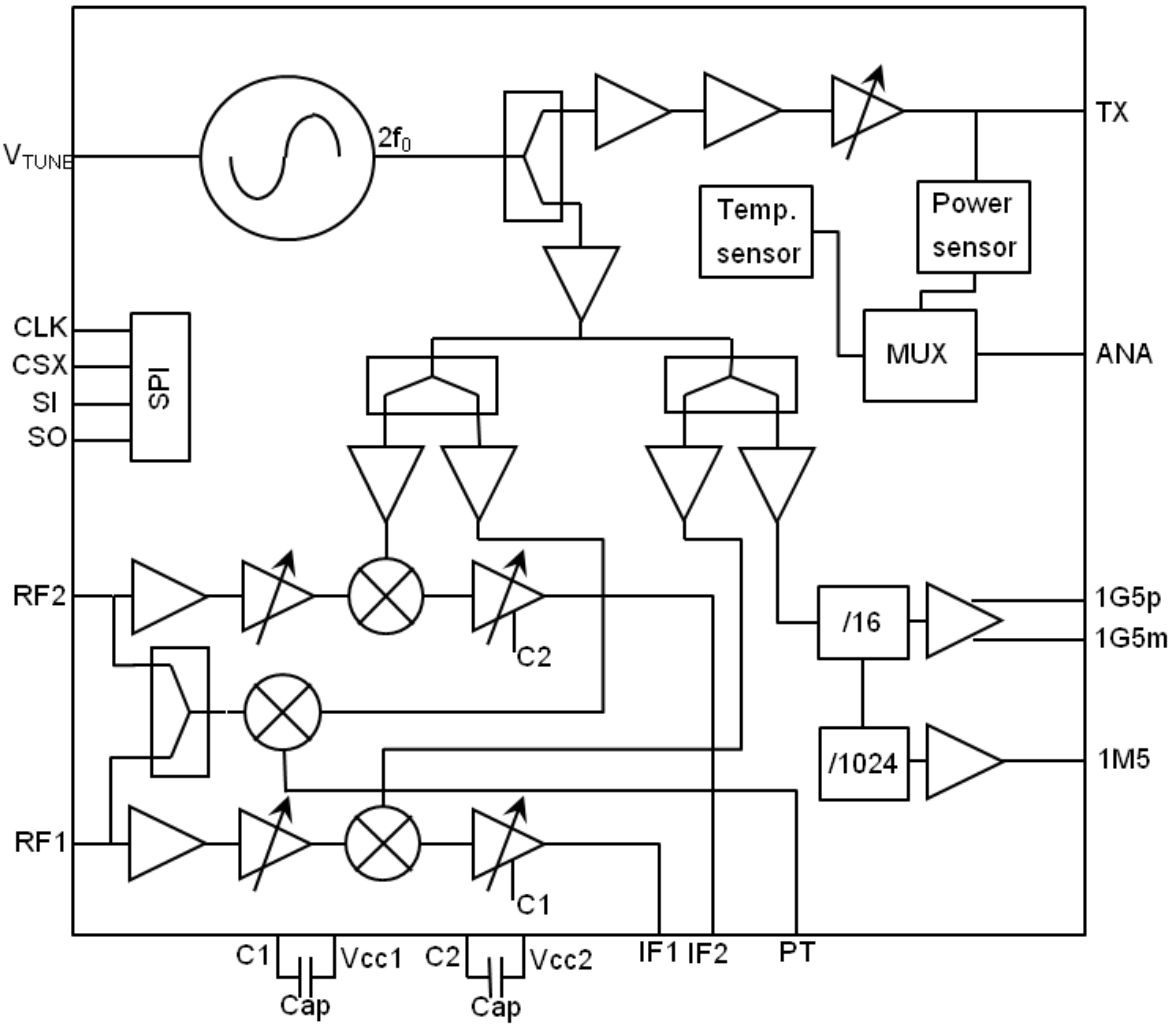
BLOCK DIAGRAM



POWER/TEMPERATURE

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	3.1	3.3	3.5	V
I_tot	Total Supplies Current (@ Pout stage 0)		225	390	mA
I_{CC1},I_{CC2}	Supply Current			80	mA
I_{DD}	Supply Current			28	mA
I_{VCO}	Supply Current			57	mA
$I_{LO,TX}$	Supply Current			145	mA
T_{Case}	Operating Temperature (lead frame slug #29)	-40		+125	°C
T_S	Storage Temperature	-40		+150	°C

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TX section

T_{Case}.= -40°C to +125°C, Vcc = +3.1 V to 3.5V, unless specified: (*) =>Vcc ≤ +3.4V

Symbol	Parameter	Min	Typ	Max	Unit
$f_{VCO,1}$	VCO Frequency Range 1	24.00		24.25	GHz
$f_{VCO,2}$	VCO Frequency Range 2	24.00		24.5	GHz
$V_{tune,1}$	VCO Tuning Voltage Range 1	0.3		4.5	V
$V_{tune,2}$	VCO Tuning Voltage Range 2	0.3		5.3	V
f_{core}	Core VCO Frequency	22		26	GHz
$\Delta f / \Delta V_{tune,1}$	VCO Tuning Sensitivity 1	350	600	1000	MHz/V
$\Delta f / \Delta V_{tune,2}$	VCO Tuning Sensitivity 2	300	550	1000	MHz/V
$I_{\_Tune}$	DC Current into V_TUNE Pin: Frequency Range 1 Frequency Range 2		< 0.001	0.5 2	mA
Δf / °C	VCO Frequency Drift over Temperature			6	MHz/°C
$P_{N100kHz}$	VCO Phase Noise @ 100kHz offset		-90	-80	dBc/Hz
$\Delta f / \Delta V_{CC}$	VCO Pushing		50	200	MHz/V
Δf_{int1}	VCO Pulling vs. MPA, LO, PT Buffer Adjust			8	MHz
Δf_{int2}	VCO Pulling vs. Prescaler (B12='1' & B13 alternate btw '0' & '1') (w/o thermal drift)		0.05	0.5	MHz
Δf_{int3}	VCO Pulling vs. Mute (w/o thermal drift) @ 3.3V 3.1-3.5V		1.5	3 5	MHz
Δf_{ext}	TX Load Pulling into 3:1 VSWR @ MPA power control settled to Max @ MPA power control settled to Max-5dB		1.5 0.25	4 1	MHz
Z_{TXLoad}	TX Load Impedance		50		Ω
$\Delta P_{O(f)}$	TX Power Variation over Frequency			+/- 1	dB
$\Delta P_{O(f \& temp)}$	TX Power Variation range over Frequency and Temperature: @ MPA power control B7B6B5B4="0000" B7B6B5B4="0001" B7B6B5B4="100X" & "1010"		2.6 2.5 0.5	4 3.5 (*) 1.3	dB
$P_{O, ctr}$	TX Output Power @ f_{VCO} @ MPA power control B7B6B5B4="0001" B7B6B5B4="1000" B7B6B5B4="1001" B7B6B5B4="1010"	8.5 5.5 5 4	12.5 8.5 8 7.4	14.5 (*) 11 10.5 10	dBm

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$P_{O,max}$	TX Maximum Output Power @ f_{VCO} (with power control)	9.5	13.2	14.5	dBm

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TX section (cont'd)

T_{Case}.= -40°C to +125°C, Vcc = +3.1 V to 3.5V, unless specified: (*) =>Vcc ≤ +3.4V

$P_{O,min}$	TX Minimum Output Power @ f_{VCO} (with power control)	-3	1.5	6	dBm
N_{PO}	TX Output Power Steps		16		
P_{TX}	TX Power Sensor Voltage @ max TX power (sensor voltage linear with power)	0.8	1.9	3.1	V
f_{TXPS}	TX Power Sensor Frequency Response	10	20		kHz
D_{Q1}	Prescaler 1 Division Ratio		16		
P1G5	Prescaler 1 Output Power on 1G5p & 1G5m (Bit17='1' / Nominal Prescaler power setting)	-10	-6	-2	dBm
D_{Q2}	Prescaler 2 Division Ratio		1024		
V_{Q2}	Prescaler 2 Output Voltage Adjust Range (bit21='0' / P1M5 Full swing)	0.1	-	Vcc	V
$Z_{P1M5\ Out}$	Output Impedance of Prescaler 2 for P1M5 (Bit21='1' / P1M5=100mVpp)		50		Ω
$Z_{P1M5\ Load}$	Load of Prescaler 2 for P1M5	3.5		20	kΩ
$P_{O(mute)}$	TX Power Disable (Mute)		-40	-25	dBm
H_{n_Tx}	TX Harmonics (12, 36, 48 & 60GHz)		-30	-24	dBm
H_{n_SUPPLY}	Bias ports Harmonics (12, 36, 48 & 60GHz) w/o external decoupling		-18	-10	dBm
H_{pres}	Prescaler Harmonics rejection (B17='1')		-27	-20	dBc
Sp_{TX}	Non-harmonic Spurious Rejection (prescaler OFF)		-80	-70	dBc

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RX section

T_{Case} = -40°C to +125°C, Vcc = +3.1 V to 3.5V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	24		24.5	GHz
Z_{RXn}	RXn Port Impedance		50		Ω
RL_{RXn}	RXn Return Loss		-20	-10	dB
$Z_{IFn\ Out}$	Output Port Impedance of IF Amplifier			50	Ω
$Z_{IFn\ Load}$	Load of IF Amplifier (Bit 17='1' / nominal power)	150			Ω
$Z_{IFn\ Load}$	Load of IF Amplifier (Bit 17='0' / low power)		500		Ω
CG_{total}	Conversion Gain (Min VGA, Nom mixer, Nom IF gain / 150 Ω IF load)	21	28	34	dB
	Conversion Gain (Nom VGA , Nom mixer, Nom IF gain / 150 Ω IF load)	25	32	39	
	Conversion Gain (Max VGA , Nom mixer, Nom IF gain / 150 Ω IF load)	27	35	42	
ΔCG_{RF}	Conversion Gain Variation vs RXn Frequency			± 1	dB
ΔCG_{total_cp}	Conversion Gain over Temperature (With VGA gain settings, see P17 Rx Gain)			±1	dB
ΔCG_{total}	Conversion Gain variation range over Temperature @ Nominal Gain (RF & IF)		±2.5	±3	dB
ΔG_{RF}	RF gain adjust range		10		dB
ΔG_{IF}	IF Gain adjust range		14		dB
$I_{TX/RXn}$	TX to RXn Isolation @ MPA power control settled to Max @ MPA power control settled to Max-5dB	 45 40	 50 45		dB
$I_{LO/RXn}$	TX/LO to RXn leakage @ any MPA power control settings		 -40	 -34	dBm
$I_{LO/IFn}$	LO to IFn leakage		-35	-30	dBm
$I_{RX1/IF2}$	RX1 to IF2 Isolation	30	38		dB
$I_{RX2/IF1}$	RX2 to IF1 Isolation	30	38		dB
$I_{RXi/RXj}$	RX1 to RX2 & RX2 to RX1 Isolation	30	35		dB
$f_{IF\ HP}$	Lower cut-off frequency of IF Amplifier (HP characteristic)		DC	10	kHz
$f_{IF\ LP}$	Upper cut-off frequency of IF Amplifier (LP characteristic)	10	25	40	MHz
FS_if	Roll-off factor of IF Amplifier			20	dB/dec
τ_{IF}	IF Amplifier time constant τ			0.7	µs
$N_{SSB(10kHz)}$	Noise Figure SSB at IF=10kHz (HPF=OFF) nominal RF & IF gain		<15	18	dB
$N_{SSB(\geq 100kHz)}$	Noise Figure SSB at IF≥100kHz (HPF=OFF) nominal RF & IF gain		11.5	15	dB

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RX section (cont'd)

T_{Case} = -40°C to +125°C, Vcc = +3.1 V to 3.5V

IF_{noise}	IF Noise Power Density @ CG_{RF} gain with 150 Ω IF load and IF=100kHz and HPF=OFF		-136	-130	dBm/Hz
ΔIF_{noise}	IF Noise Power Variation over Temperature (With VGA gain settings, see P17 Rx Gain)			±2.5	dB
f_{Cn}	IFn Noise Corner Frequency (HPF=OFF)		10		kHz
IP_{1dB}	RF Input Compression Point (Min VGA, Nom mixer, Min IF gain)	-19	-14		dBm
	RF Input Compression Point (Nom VGA , Nom mixer, Min IF gain)	-24	-18		
	RF Input Compression Point (Max VGA , Nom mixer, Min IF gain)	-28	-21		
IIP_3	3rd Order Input Intercept Point (Min VGA, Nom mixer, Min IF gain)	-9	-5		dBm
	3rd Order Input Intercept Point (Nom VGA , Nom mixer, Min IF gain)	-14	-9		
	3rd Order Input Intercept Point (Max VGA , Nom mixer, Min IF gain)	-18	-12		
$V_{IFn(1dB comp)}$	IFn Output Voltage at 1dB Compression Point (HPF ON / BIT10='0')	2	2.5	3	V_{p-p}
H_{pIF}	IFn Harmonics (P_RF<IP1dB-3dB)		-30	-20	dBc
Sp_{IF}	Mixing Products Spurious			-30	dBc
$\Delta_{\varphi Diff}$	Phase Tracking between IF1, IF2 (calibrated)	-3		3	Deg
$\Delta_{\varphi Diff,uncal}$	Phase Difference Variation (ØIF1 – ØIF2) for equal phase RX input	0	±1	±15	deg
$\Delta_{\varphi Diff,power,up}$	Phase Difference Variation (ØIF1 – ØIF2) for equal phase RX input and power up with calibrated Frequency Range	0	±1	±2	deg
ΔP_{IF}	Amplitude Tracking between IF1, IF2 (calibrated)		±0.25	±1	dB
H2 & H3	RF & LO Harmonics (2nd & 3rd) at IF Ports			-30	dBm
V_{ANA}	ANA output voltage	0.2		3.1	V
R_{ANA}	ANA resistive load	9	10	11	kΩ
C_{ANA}	ANA capacitive load			15	nF
ΔV_{Temp}	Temperature Sensor Voltage Sensitivity	6.25	7	7.75	mV/°C
V_{Temp}	Temp. Sensor Voltage @ T_{Case} = +25°C	0.7	1.65	2.33	V
	Temp. Sensor Voltage @ T_{Case} = +125°C	1.47		3.1	
	Temp. Sensor Voltage @ T_{Case} = -40°C	0.2		1.83	
$t_{TempSet}$	Temperature Sensor Settling Time			1	ms

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

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ABSOLUTE MAX RATINGS

Parameter	Min Rating	Max Rating	Unit
V_{CC} to GND	-0.3	3.8	V
Digital I/O Voltage to GND	-0.3	V_{CC}+0.3	V
Analog Voltage AMUX to GND	-0.3	V_{CC}+0.3	V
Analog I/O Voltage to GND	-0.3	V_{CC}+0.3	V
Analog Voltage V_TUNE to GND	-0.3	7.5	V
DC Current into IF1, IF2 Pin	0	12.5	mA
DC Current into ANA Pin	0	0.4	mA
DC Current into V_TUNE Pin (1)		9	mA
RF Power Input at RX1, RX2 Pin		0	dBm
DC Voltage at RF Output Tx Pin and RF Input RX1, RX2 Pin		0	V
Total DC Power Dissipation		1.36	W
Absolute T_{Case} Operating Temperature (lead frame slug #29)	-40	+125	°C
Non-operating Temperature Range (Storage)	-40	+150	°C
Peak Soldering Temperature		+260	°C

Operation of this device above anyone of these parameters may cause permanent damage or reduce MTTF. All functions activated (max DC current SPI configuration)
(1) Voltage applied through external serial resistor to limit V_TUNE current below 9mA DC.

Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (T_{Case}) as shown below.
The system maximum temperature must be adjusted in order to guarantee that T_{Case} remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

Thermal Performance Specifications

All functions activated (max DC current SPI configuration)
Maximum continuous dissipated power at T_{case} = +125ºC: 1.36 Watts
Power dissipation de-rating above T_{case} = +130ºC: 68mW/ ºC
(De-rating applied to all Voltage Supply)

Detailed max devices Tj:

Package ICs Max devices Tj	Absolute Max Tj	Max Pdiss Max Tj	Tx Stage 0 Nom Tj	Mute Tx Nom Tj
GaAs Tx	+175°C	T_{Case} + 45°C	T_{Case} + 40°C	T_{Case} + 20°C
SiGe Rx	+150°C	T_{Case} + 16°C	T_{Case} + 12°C	T_{Case} + 12°C

Nominal Pdiss=0.8W (@ DP='1' / Ptx Stage 0)

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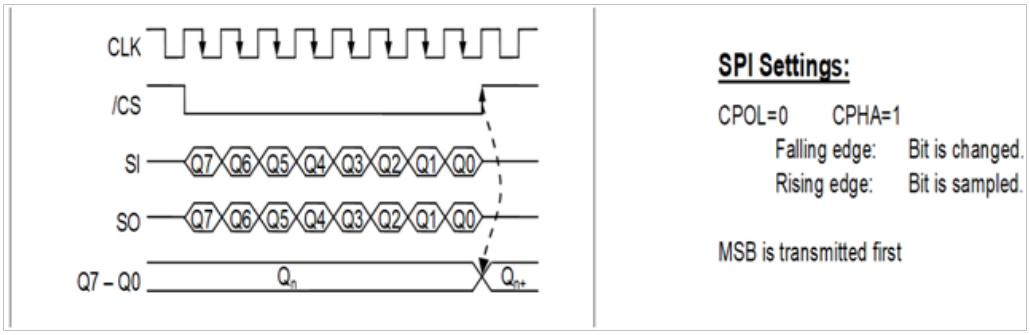
SPI

The digital input should use standard 4-wires synchronous serial peripheral interface (SPI) with data read and write capabilities. The SPI has hardwired Power-On Reset, such that the output bits for Control Bus will be set to default state (low power mode) after turning on 3.3V supply. Data transmission is enabled by negative edge of CS (Chip Select) and serial data input (SI) are then read at the falling edge of CLK (SPI Clock). The timing diagram in the next picture describes the principle of the SPI timing and handling between shift and storage register.



SPI TIMING

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Serial clock frequency			30	50	MHz
Serial SI and CSX high time		10			ns
Serial SI and CSX low time		10			ns

Digital I/O Levels

Symbol	Parameter	Min	Typ	Max	Unit
V_{OH}	High Level Output	2.4			V
V_{OL}	Low Level Output			0.4	V
V_{IH}	High Level Input	2.0			V
V_{IL}	Low Level Input			0.8	V
$I_{O,Load}$	Output Load Current		0.4	1	mA
$I_{O,Peak}$	Output Peak Current	2			mA
C_{Load}	Capacitive Load			100	pF

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SPI MAIN TABLE

Data Bit	Function	Description
LSB B0	VGA Gain	8 VGA gain settings(1)
B1		
B2		
B3	IF Low Pass Filter	IF Low Pass Filter(2)
B4	MPA Power	16 MPA gain settings(3)
B5		
B6		
B7		
B8	MPA Mute	TX OFF mode(4)
B9	LO AMPS	LO amplifier enable(5)
B10	IF High Pass Filter	IF High Pass Filter(6)
B11	Not Used	Not Used
B12	Prescaler	4 prescaler settings(7)
B13		
B14	Pilot Tone	RX channels self test(8)
B15	MUX	4 Analog outputs(9)
B16		
B17	DC Power mode	2 loads(10)
B18	IF Amp Gain	8 IF gain settings(11)
B19		
B20		
B21	1.5MHz mode	2 voltage swing setting(12)
B22	Mixer Gain	2 Mixer gain settings(13)
MSB B23	IC Enable	IC Enable(14)

VGA NOMINAL GAIN SETTINGS TABLE (1 from SPI main table)

B2	B1	B0	VGA Gain
0	0	0	+2.6 dB
0	0	1	+1.2 dB
0	1	0	Nominal / 0 dB
0	1	1	-1.1 dB
1	0	0	-1.9 dB
1	0	1	-2.9 dB
1	1	0	-3.6 dB
1	1	1	-4.3 dB

LO AMPLIFIER SETTINGS TABLE (5 from SPI main table)

Bit9	LO amplifier enable
0	OFF
1	ON

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MPA NOMINAL POWER SETTINGS TABLE (3 from SPI main table)

B7	B6	B5	B4	Tx Power stage	MPA Power variation
0	0	0	0	0	Nominal / 0 dB
0	0	0	1	1	-0.7 dB
0	0	1	0	2	-1.3 dB
0	0	1	1	3	-1.9 dB
0	1	0	0	4	-2.5 dB
0	1	0	1	5	-3.0 dB
0	1	1	0	6	-3.6 dB
0	1	1	1	7	-4.2 dB
1	0	0	0	8	-4.7 dB
1	0	0	1	9	-5.2 dB
1	0	1	0	10	-5.8 dB
1	0	1	1	11	-6.5 dB
1	1	0	0	12	-7.3 dB
1	1	0	1	13	-8.3 dB
1	1	1	0	14	-9.6 dB
1	1	1	1	15	-11.7 dB

MIXER NOMINAL GAIN SETTINGS TABLE (13 from SPI main table)

Bit22	Mixer Gain
0	nominal -3dB
1	nominal

PRESCALER MODE SETTINGS TABLE (7 from SPI main table)

B13	B12	Prescaler mode
0	0	OFF
0	1	Frequency output 1.5MHz
1	0	Frequency output 1.5GHz
1	1	OFF / Low Pulling

1.5MHz MODE SETTINGS TABLE (12 from SPI main table)

Bit21	1.5MHz mode
0	Full output swing 0-Vcc
1	0.1Vpp / 50Ω

DC POWER MODE SETTINGS TABLE (10 from SPI main table)

Bit17	DC power mode
0	Zif ≥ 500Ω / P1G5 -3dB / Reduced DC power
1	Zif ≥ 150Ω / P1G5 nominal

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MPA MUTE SETTINGS TABLE (4 from SPI main table)

Bit8	MPA mute
0	TX OFF
1	TX ON

MUX SETTINGS TABLE (9 from SPI main table)

B16	B15	Mux mode
0	0	ANA=∞ Ω
0	1	ANA=T°C
1	0	ANA=PTX

IC ENABLE (14 from SPI main table)

Bit23	IC Enable
0	IC OFF (except core VCO)
1	IC ON

IF GAIN SETTINGS TABLE (11 from SPI main table)

B20	B19	B18	IF gain settings
0	0	0	+4dB
0	0	1	+2dB
0	1	0	Nominal / 0dB
0	1	1	-2dB
1	0	0	-4dB
1	0	1	-6dB
1	1	0	-8dB
1	1	1	-10dB

IF LOW PASS FILTER SETTINGS TABLE (2 from SPI main table)

Bit3	IF low pass characteristic
0	F_{cut}=25MHz (nominal)
1	F_{cut}=60MHz

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IF HIGH PASS FILTER SETTINGS TABLE (6 from SPI main table)

Bit10	**IF High Pass Filter**			
0	Nominal IF High Pass Filter*			
	Capacitor value	Cap=1nF	Cap=10nF	Cap=100nF
	f_{cut}	10kHz	1KHz	100Hz
	Rx Gv @ 100kHz	**Nom**	**Nom**	**Nom**
	Rx Gv @ 10kHz	Nom – 3dB	**Nom**	**Nom**
	Rx Gv @ 1kHz	Nom -17dB	Nom – 3dB	**Nom**
	Rx Gv @ 100Hz	Nom - 20dB	Nom -17 dB	Nom – 3dB
	Rx NFssb @ 100kHz	Nom + 2dB	**Nom**	**Nom**
	Rx NFssb @ 10kHz	Nom + 25dB	Nom + 5dB	**Nom**
	Rx NFssb @ 1kHz	Nom + 62dB	Nom + 28dB	Nom + 20dB
	Rx NFssb @ 100Hz	Nom + 102dB	Nom + 48dB	Nom + 43dB
1	IF low pass through			

The table is valid for gain settings VGA at max gain and Mixer at nominal gain & any IF gain

*In order to have a pass band characteristic, capacitors must be connected between the pin 2-28 for RX1 and 7-9 for RX2 (see pin-out)

If HPF not used (bit10='1'), pins 2 and 7 can be left open

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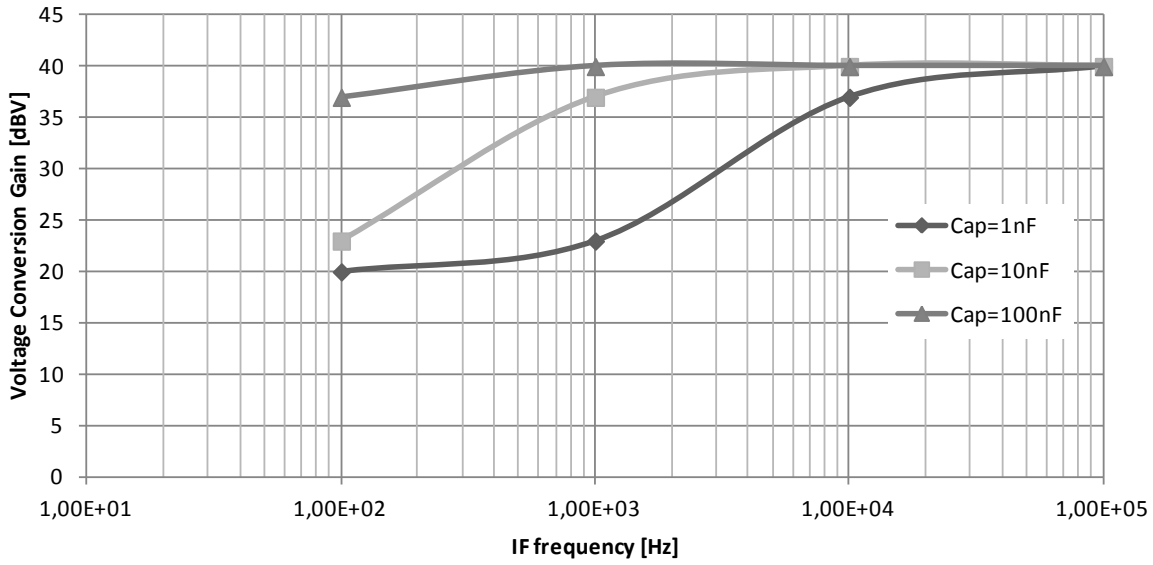
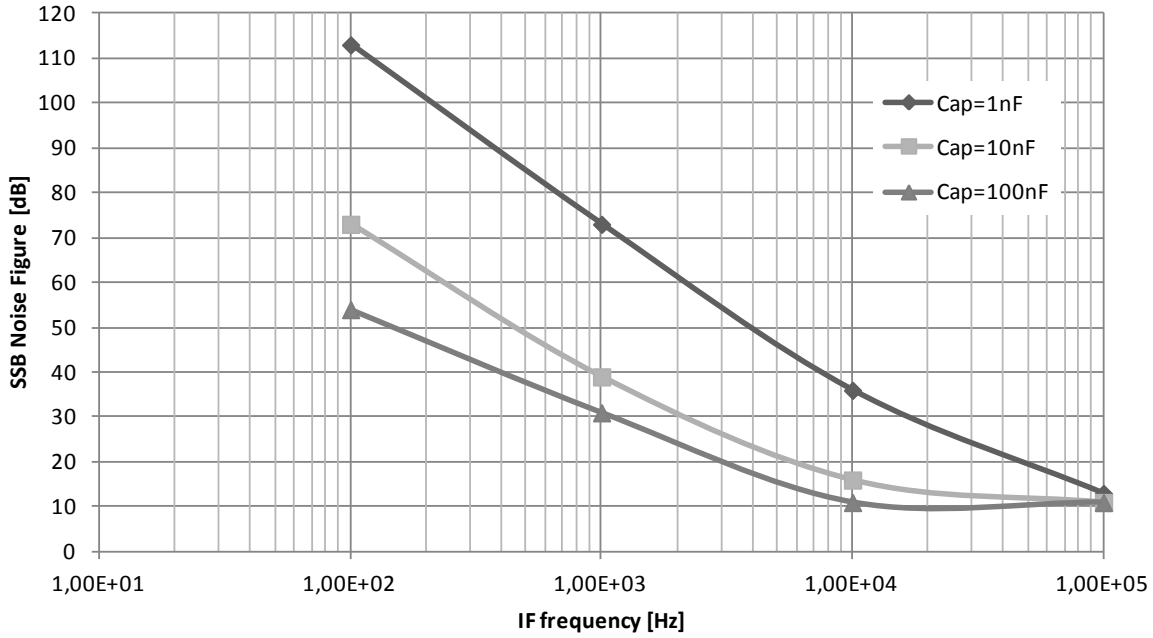
Measurements on “Evaluation mother board”

Conversion gain versus IF frequency and HPF cap
(nominal RF & IF gain)



SSB Noise Figure versus frequency and HPF cap



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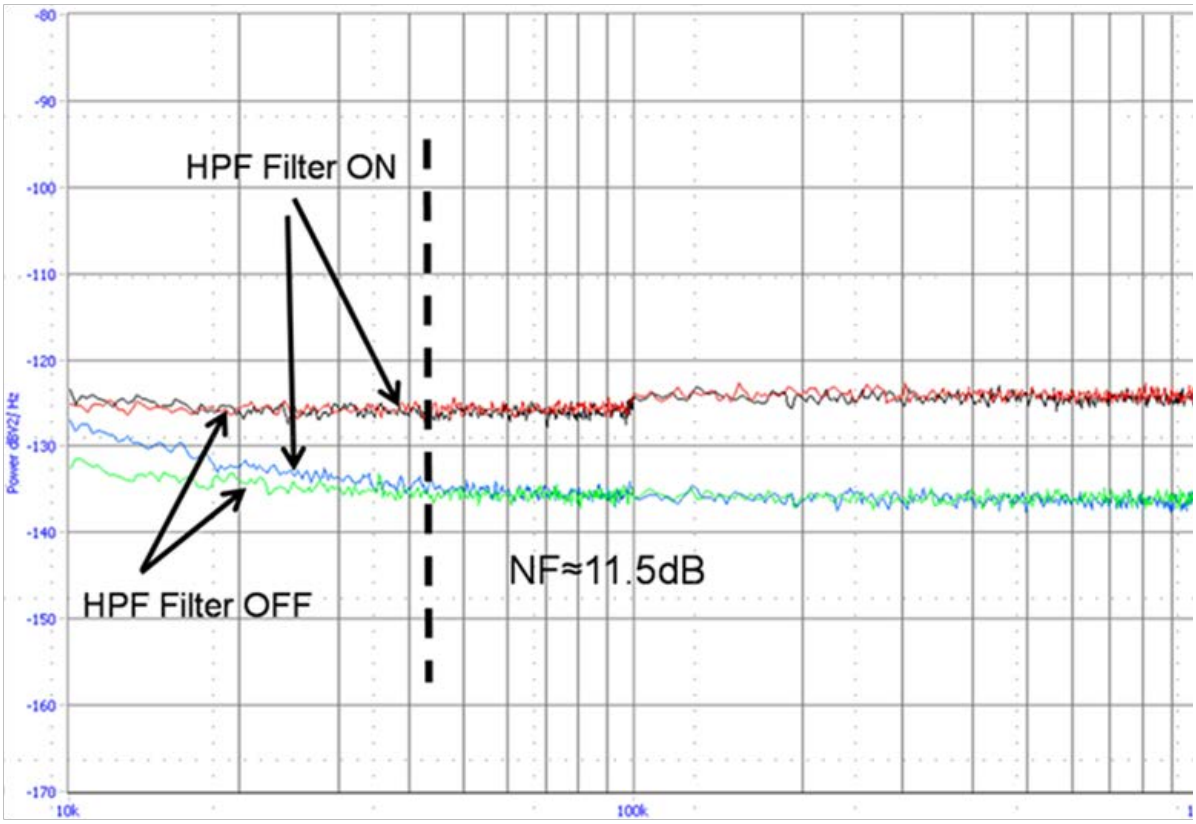
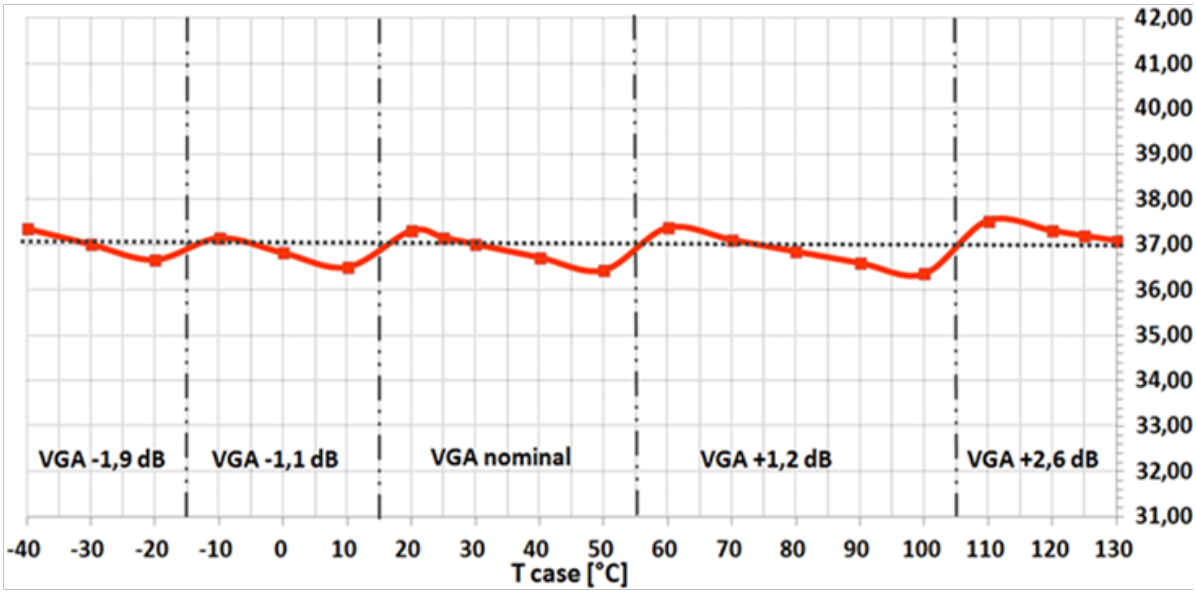
Measurements on “Evaluation mother board” (cont’d)

SSB Noise Figure versus IF frequency
(HPF Cap=10nF / nominal RF & IF gain / HPF on-off)



Rx Gain over Tcase using VGA settings
(Nominal 3.3V supplies)



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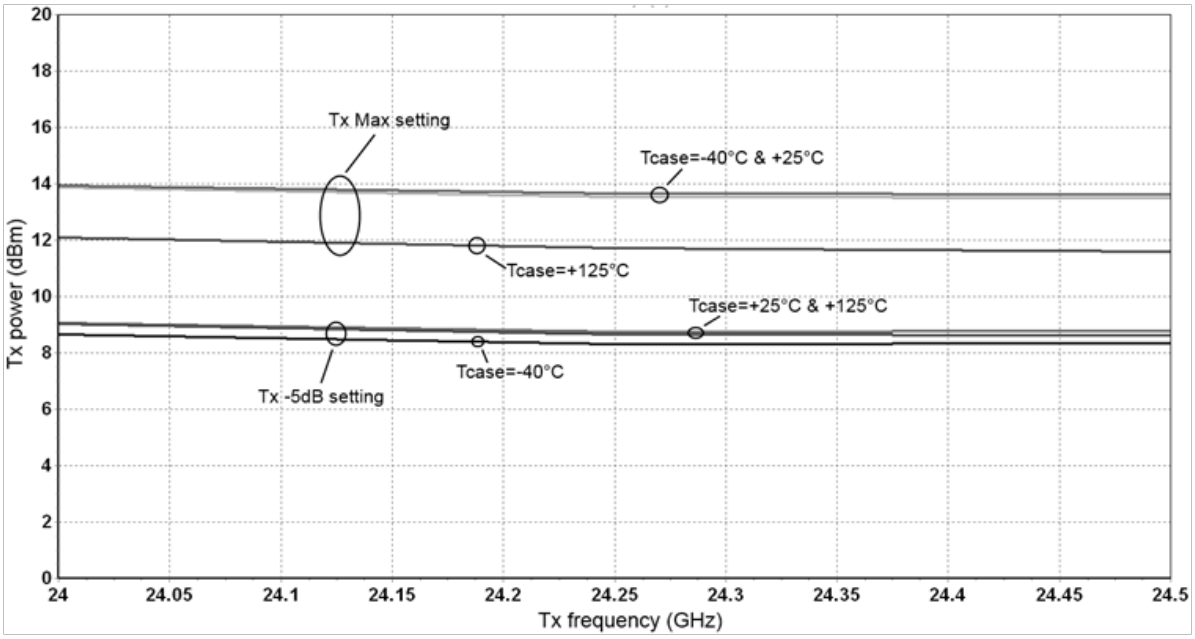
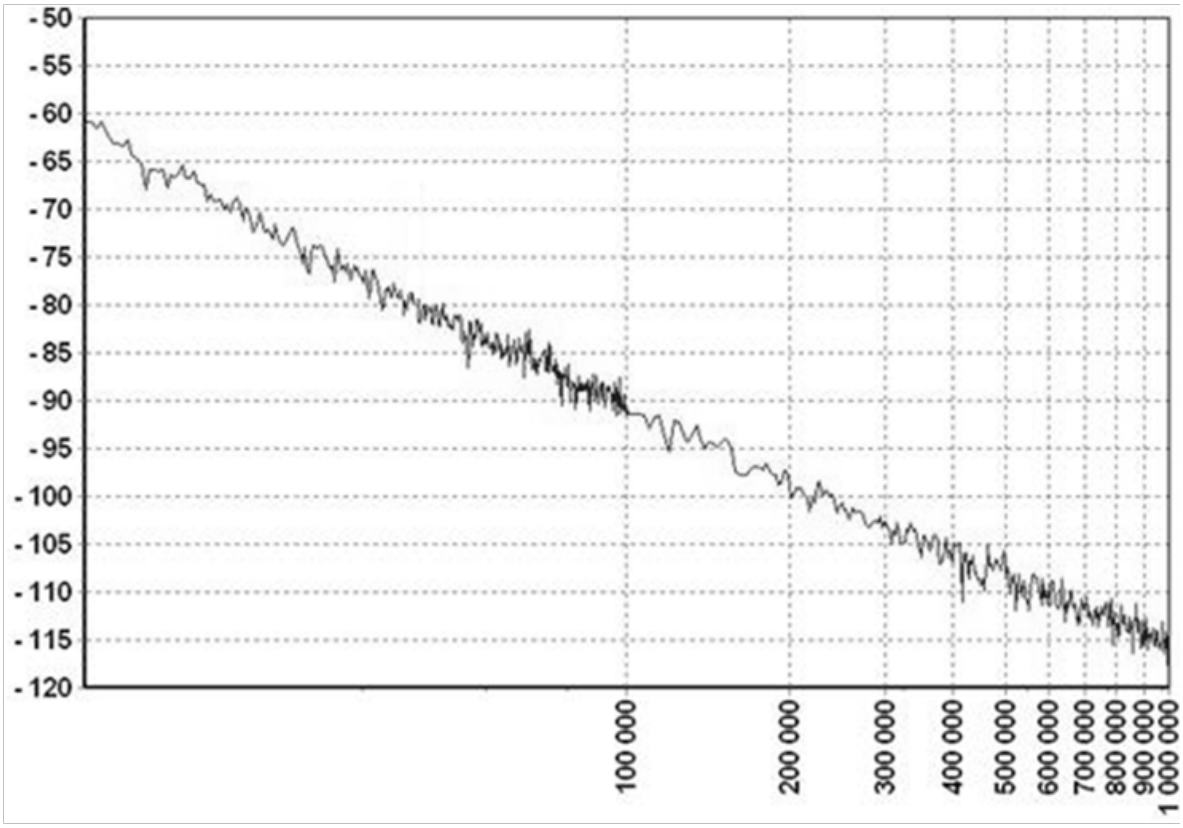
Measurements on “Evaluation mother board” (cont’d)

Tx output power versus RF frequency & Tcase
(Nominal 3.3V supplies)



Tx Phase Noise versus offset frequency in dBc/Hz versus Hz
(Nominal @ 24.25GHz)



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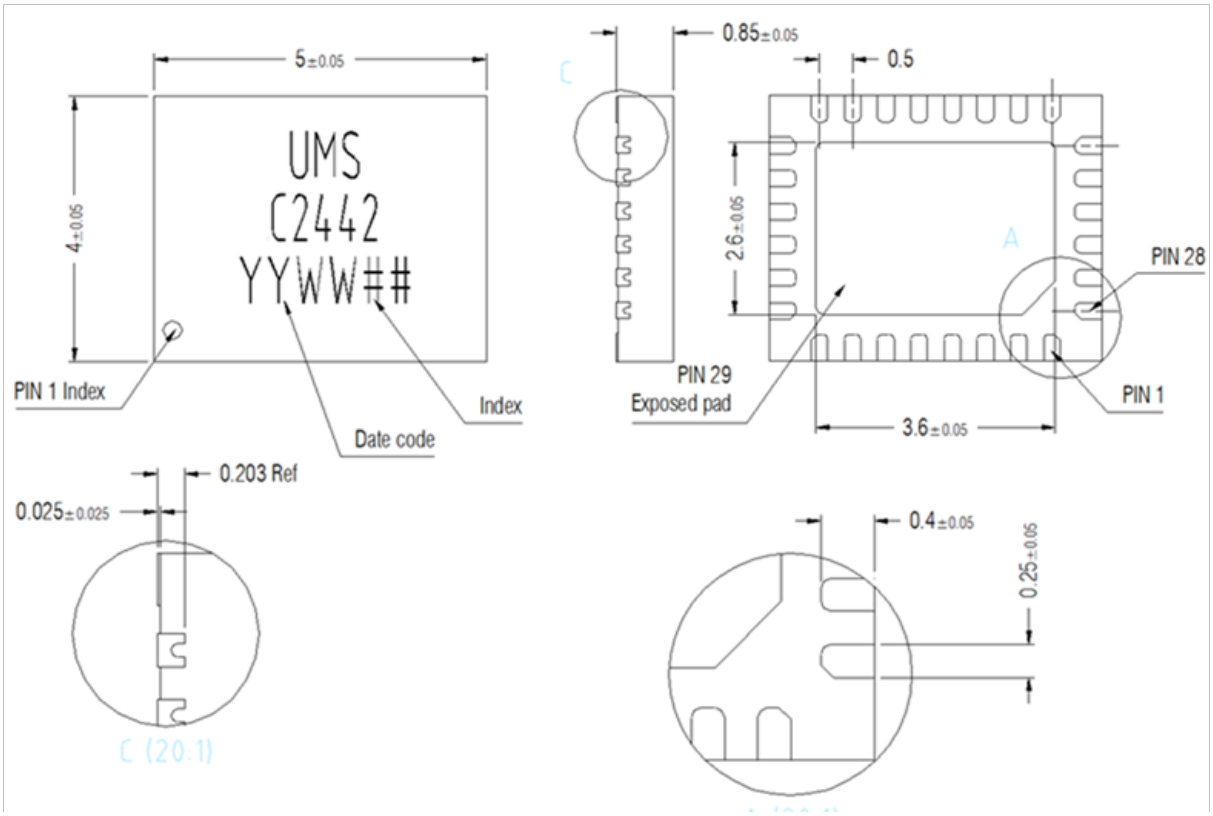
Package outline (1)



Lead Free	(Green)	1- IF1	11- VDD	21- VTX2
Units :	mm	2- C1	12- P1G5N	22- VLO
From the standard :	JEDEC MO-220	3- RF1	13- P1G5P	23- ANA
		4- Gnd (2)	14- P1M5	24- CSX
		5- Gnd (2)	15- Gnd (2)	25- SI
		6- RF2	16- TX	26- CLK
		7- C2	17- Gnd (2)	27- SO
		8- IF2	18- Vtune	28- VCC1
		9- VCC2	19- Vvco	29- Gnd (2)
		10- PT	20- VTX1	

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (http://www.ums-gaas.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package Gnd & Pin #29.

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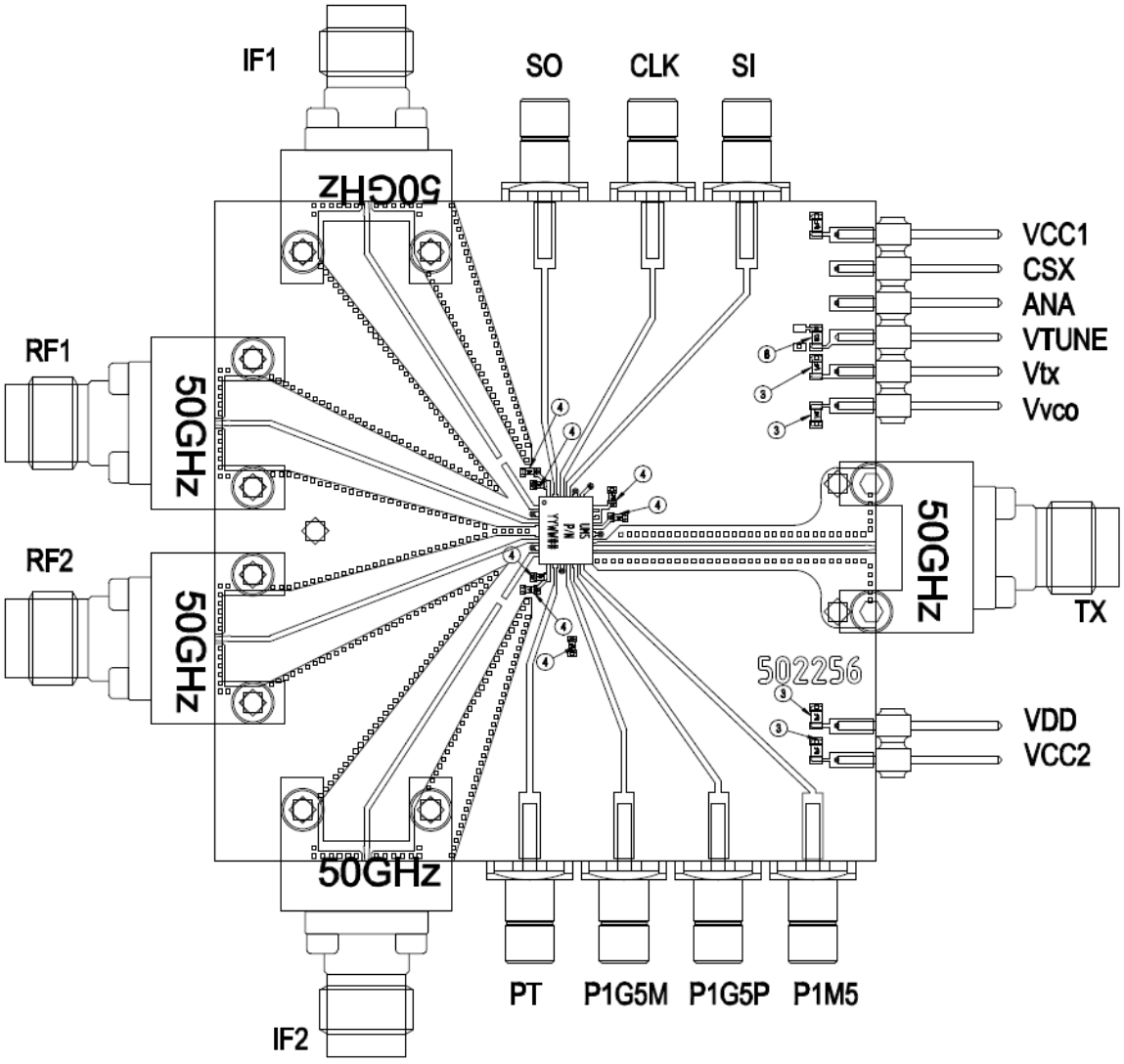
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF near the packaging and 1µF near the connectors are recommended for all DC accesses.



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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x5 RoHS compliant package:	CHC2442-QPG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

Special clearance required for Space & military application

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