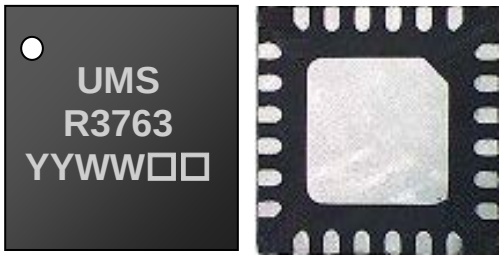
CHR3763-QDG

12-16GHz Integrated Down Converter

GaAs Monolithic Microwave IC in SMD leadless package

Description

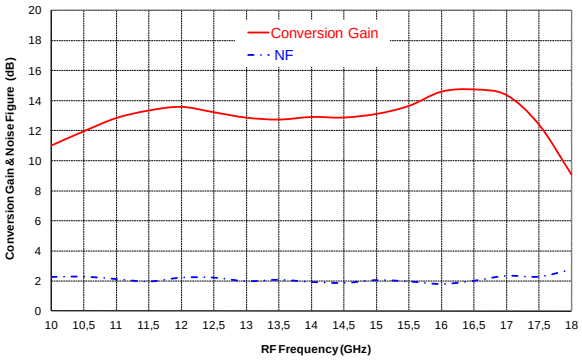
The CHR3763-QDG is a multifunction monolithic receiver, which integrates a balanced cold FET mixer, a LO buffer, and a RF low noise amplifier.
It is designed for a wide range of applications, from military to commercial communication systems.
The circuit is manufactured with a pHEMT process, 0.25µm gate length.
It is supplied in RoHS compliant SMD package.



Main Features

- Broadband RF performances: 12-16GHz
- 12dB Conversion Gain
- 2.3dB Noise Figure
- 0dBm Input IP3
- DC bias: Vd=3.0V @Id= 80mA
- 24L-QFN4x4
- MSL1

Conversion Gain & Noise Figure versus RF frequency @ IF = 2GHz (LSB mode)



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF Frequency	12		16	GHz
F_{IF}	IF frequency	DC		3.5	GHz
G	Conversion gain	10	12	14	dB
NF	Noise Figure		2.3	2.8	dB

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Specifications

Tamb.= +25°C, VD1= VD2= VD3 = +3.0V (1)

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF Frequency range	12		16	GHz
F_{LO}	LO frequency range	8.5		19.5	GHz
F_{IF}	IF frequency range	DC		3.5	GHz
G	Conversion gain (2)	10	12	14	dB
NF	Noise Figure		2.3	2.8	dB
Im_rej	Image rejection (2)	15	20		dBc
LO_IF	LO to IF isolation	15			dBc
LO_RF	LO to RF isolation	25			dBc
P_{LO}	LO Input power	1	5		dBm
IP1dB	Input power at 1 dB compression	-10	-8		dBm
IIP3	Input IP3	-1	0		dBm
LO RL	LO return loss		12		dB
RF RL	RF return loss		10		dB
VDx	DC drain voltage (1)		3		V
VG1	1st stage LNA DC gate voltage		-0.52		V
VG2	2nd stage LNA DC gate voltage		-0.46		V
VG3	LO buffer DC gate voltage		-0.46		V
VG4	Mixer DC gate voltage		-1		V
Id	Total drain current (ID1+ID2+ID3) (3)		80		mA

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

(1) VD1: 1st stage LNA drain bias voltage. VD2: 2nd stage LNA drain bias voltage.
(1) VD3: LO-chain drain bias voltage.
(2) An external combiner 90° is required on I / Q.
(3) ID1: 1st stage LNA drain current, typically 14mA, should be tuned with VG1.
(3) ID2: 2nd stage LNA drain current, typically 31mA, should be tuned with VG2.
(3) ID3: LO-chain drain current, typically 35mA, should be tuned with VG3.

Electrostatic discharge sensitive device observe handling precautions!

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vdx	Drain bias voltage	3.5	V
Id	Drain bias current	120	mA
VG1,VG2	LNA gate bias voltages	-2 to +0.4	V
VG3	LO buffer gate bias voltage	-2 to +0.4	V
VG4	Mixer gate bias voltage	-2 to +0.4	V
P_RF	Maximum peak input power overdrive (2)	+15	dBm
P_LO	Maximum LO input power	+11	dBm
Tj	Junction temperature	175	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) Duration < 1s.

Recommended Operating Range 3, 4

Symbol	Parameter	Values	Unit
VD1, VD2, VD3	Drain bias voltage	2.5 to 3	V
Id	Drain bias current	70 to 90	mA
VG1, VG2, VG3	LNA and LO buffer gate bias voltages	-1 to 0	V
P_LO	LO input power	+1 to +7	dBm
P_RF	RF power	-30 to -10	dBm

(3) Electrical performances are defined for specified test conditions

(4) Electrical performances are not guaranteed over all recommended operating conditions

Temperature Range

Ta	Operating temperature range	-40 to +95	°C
Tstg	Storage temperature range	-55 to +150	°C

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Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad Nº	Parameter	Values	Unit
VDx	13,15,18	DC drain voltages	3	V
Id	13,15,18	Total drain current	80	mA
VG1	12	1st stage LNA DC gate voltage (14mA)	-0.52	V
VG2	14	2nd stage LNA DC gate voltage (31mA)	-0.46	V
VG3	19	LO buffer DC gate voltage (35mA)	-0.46	V
VG4	17	Mixer DC gate voltage	-1	V

“Power ON” sequence

1. Bias LNA, LO buffer and Mixer gate bias voltages VG1, VG2, VG3 and VG4 at Vg close to Vpinch-off (Typically: Vg ≈ -2V)
2. Apply 3V on VD1, VD2 and VD3
3. Apply -1V on Mixer gate bias voltage VG4
4. Increase slowly LNA, LO buffer and Mixer gate bias voltages VG1, VG2 and VG3 up to quiescent bias drain current Idq =80 mA
5. Apply RF signal

“Power OFF” sequence

1. Turn off RF signal
2. Bias LNA, LO buffer and Mixer gate bias voltages VG1, VG2, VG3 and VG4 at Vg close to Vpinch-off (Typically: Vg ≈ -2V)
3. Turn VD1, VD2 and VD3 bias voltage to 0V

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4. Turn LNA, LO buffer and Mixer gate bias voltages VG1, VG2, VG3 and VG4 to 0V

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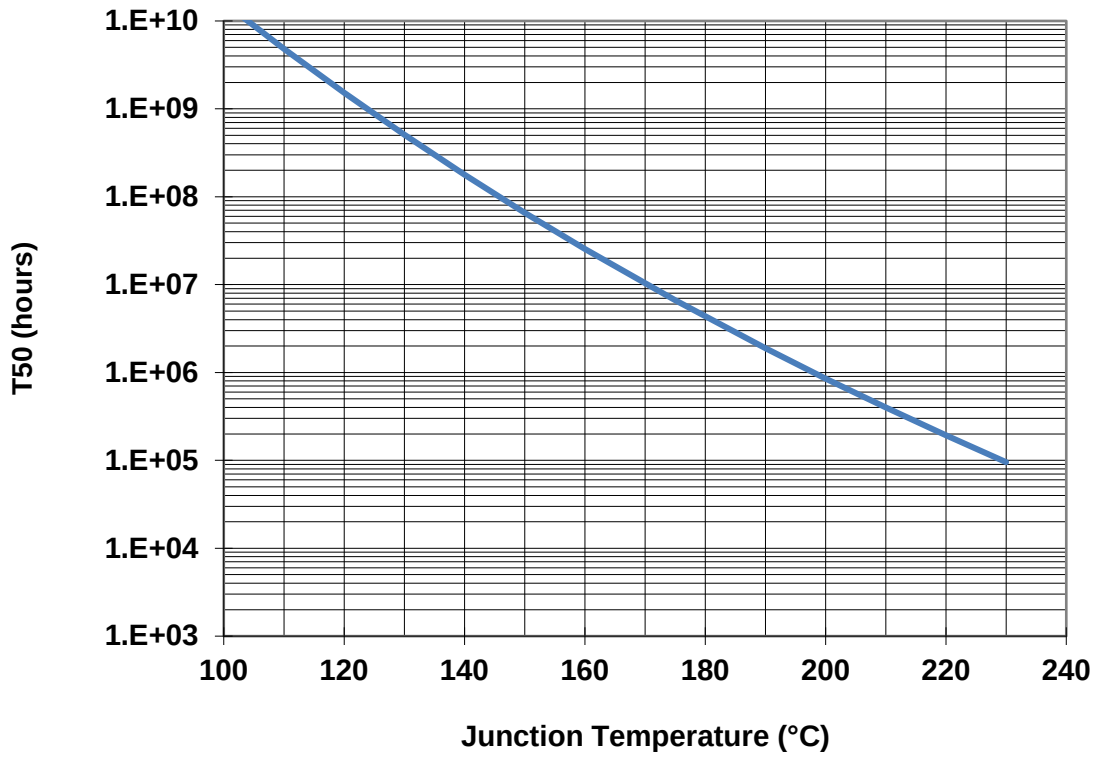
Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is only cooled down by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tcase).
The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Absolute Maximum Ratings table.
So, the system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	Tjunction (°C)	R_{TH} (°C/W)	T50 (hours)
R_{TH} [1] Thermal Resistance (Junction to Case)	Vd= 3V Id= 80mA Pdiss= 0.24W	139	201.5	1.97E+08

[1] Assuming 85°C Tcase



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Typical Board Measurements

Tamb.= +25°C, VD1= VD2= VD3= +3V, VG4= -1V, P_LO = +5dBm
These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board". Data are given in the package access planes.

Conversion Gain versus RF & LO power at IF = 2GHz
(LSB mode)

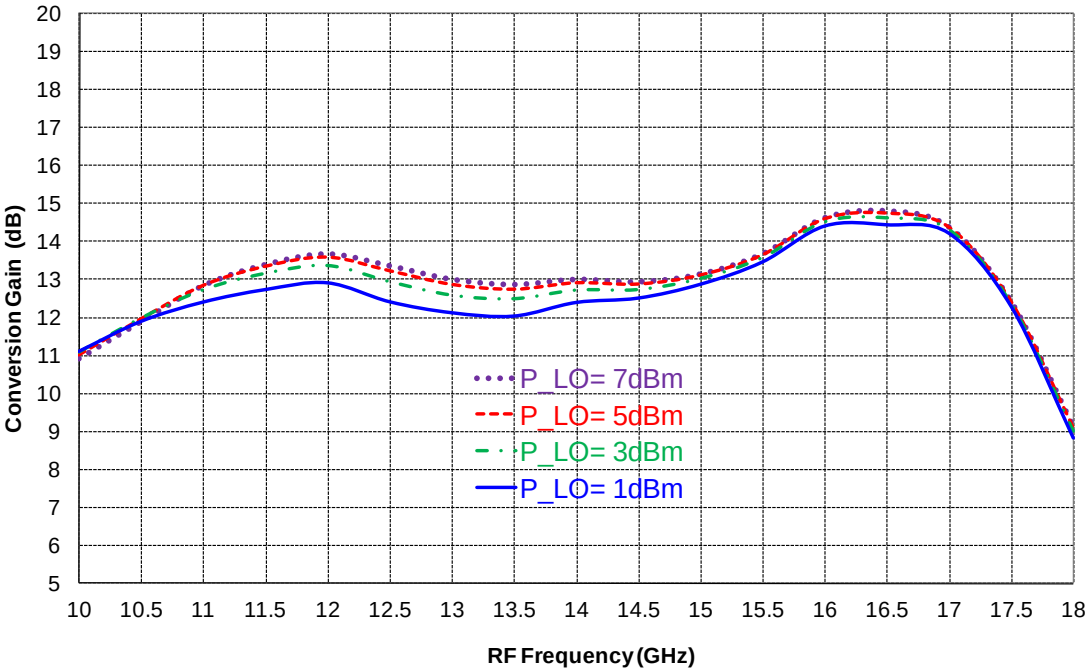
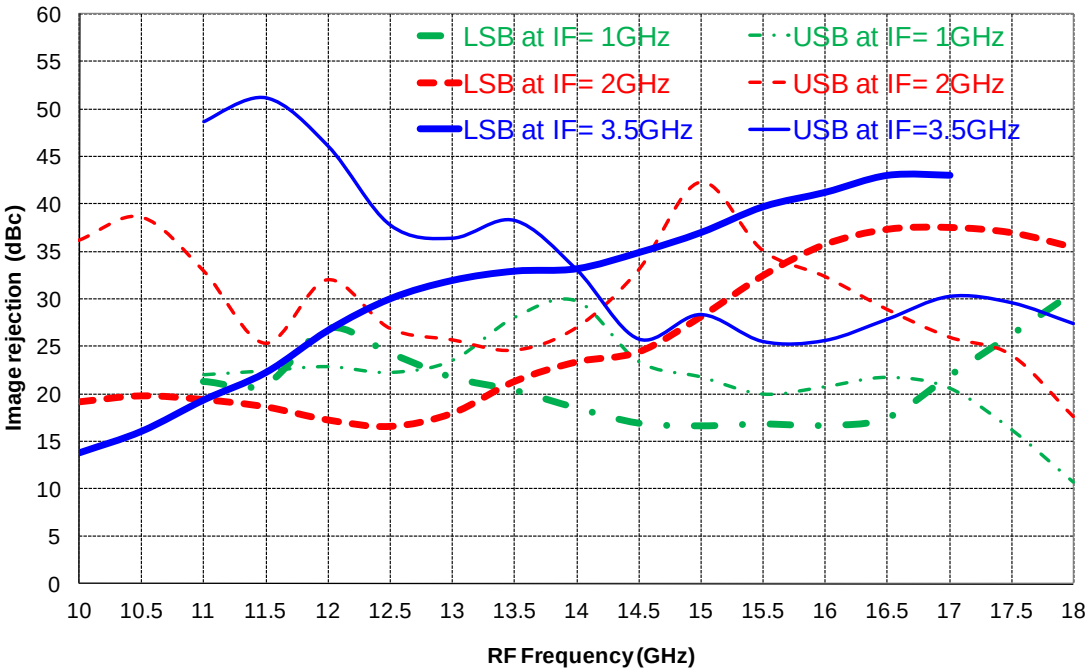


Image Rejection versus RF and IF frequencies



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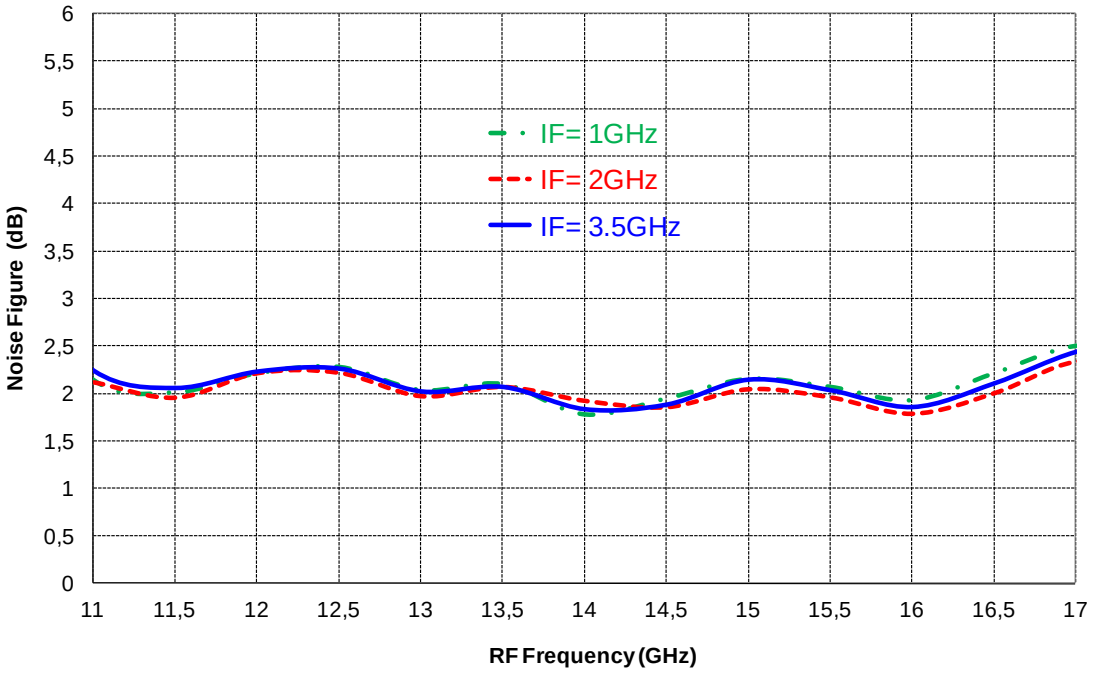
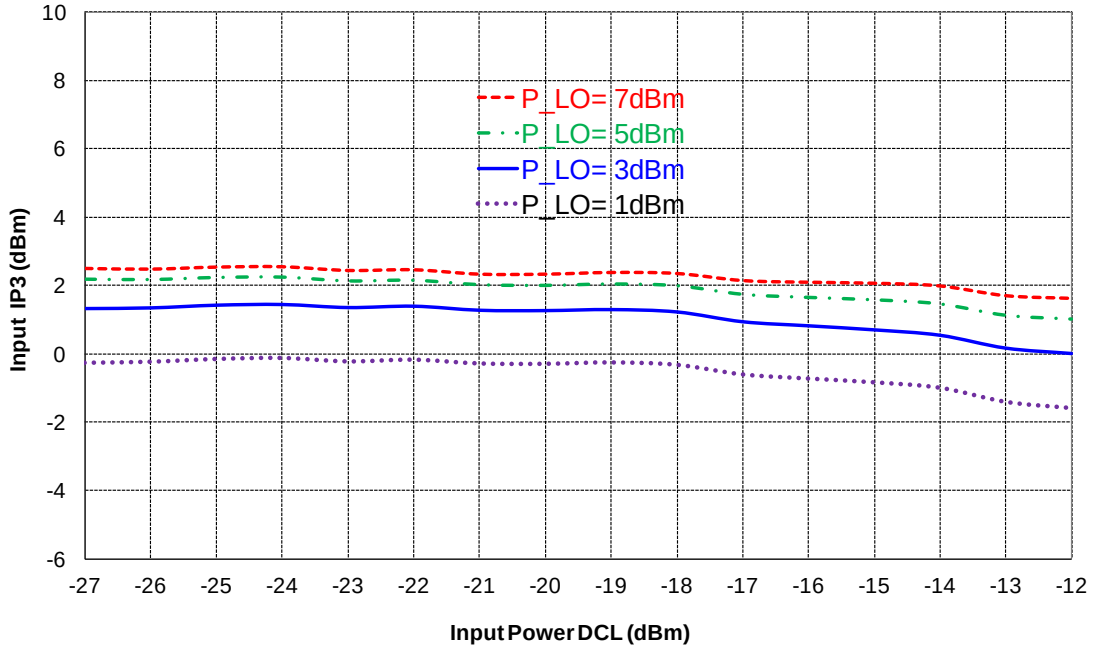
Typical Board Measurements

Tamb.= +25°C, VD1= VD2= VD3= +3V, VG4= -1V, P_LO = +5dBm

Noise Figure versus RF and IF frequencies
(LSB mode)



Input IP3 versus LO power at RF =14.5GHz & IF = 2GHz
(USB mode)



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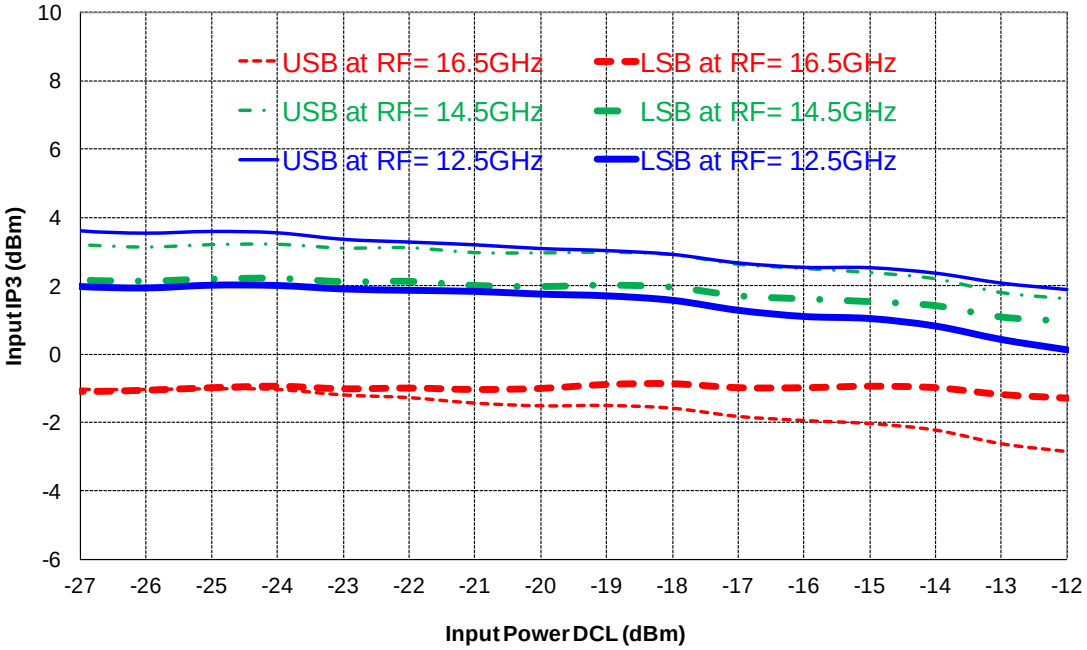
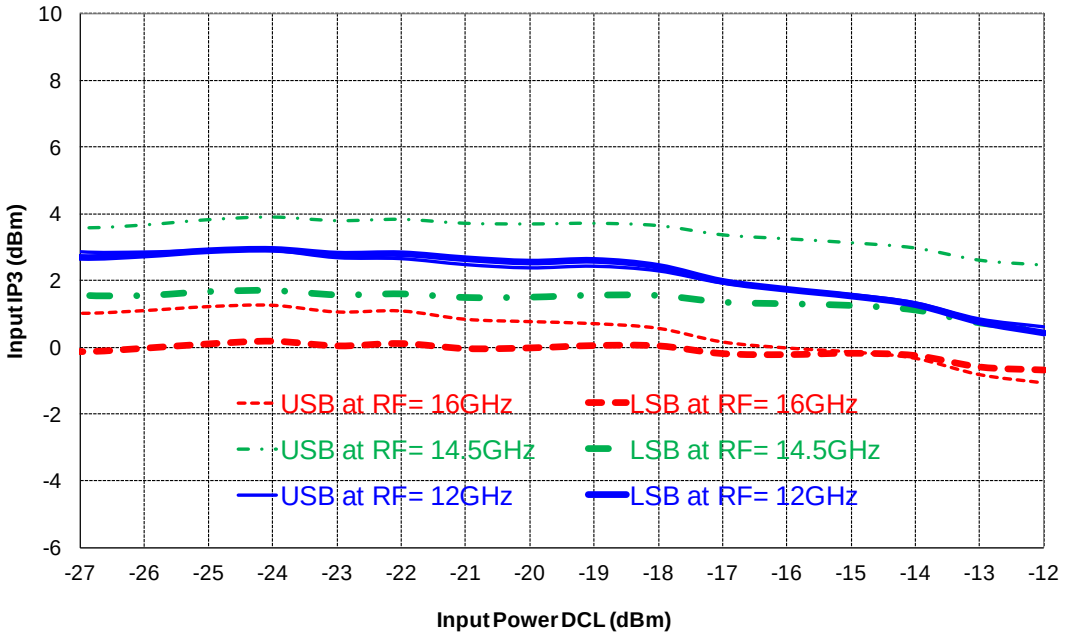
Typical Board Measurements

Tamb.= +25°C, VD1= VD2= VD3= +3V, VG4= -1V, P_LO = +5dBm

Input IP3 versus RF frequency at IF = 2GHz
(USB & LSB modes)



Input IP3 versus RF frequency at IF = 3.5GHz
(USB & LSB modes)



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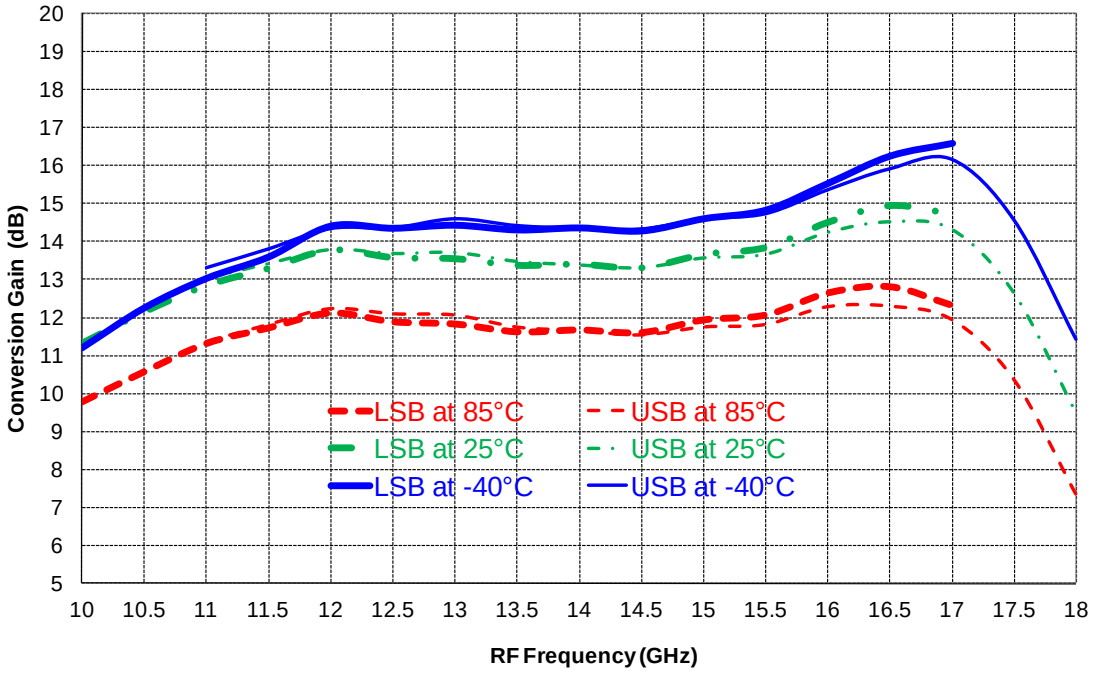
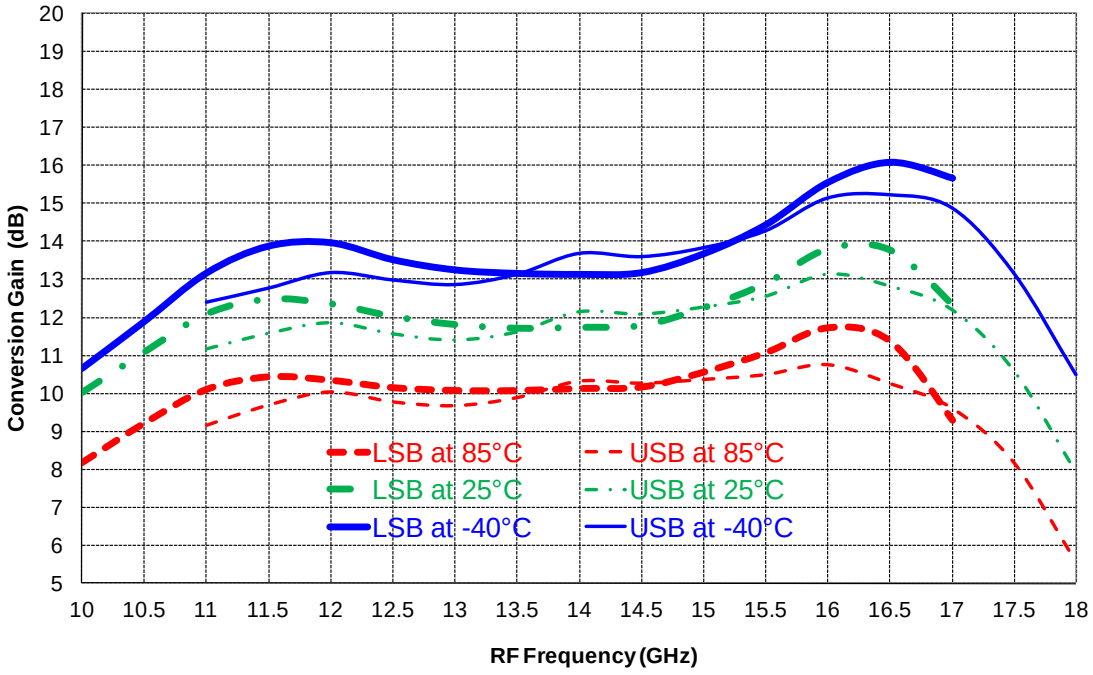
Typical Board Measurements

Tamb.= +25°C, VD1= VD2= VD3= +3V, VG4= -1V, P_LO = +5dBm

Conversion Gain versus temperature at IF = 1GHz
(USB & LSB modes)



Conversion Gain versus temperature at IF = 3.5GHz
(USB & LSB modes)



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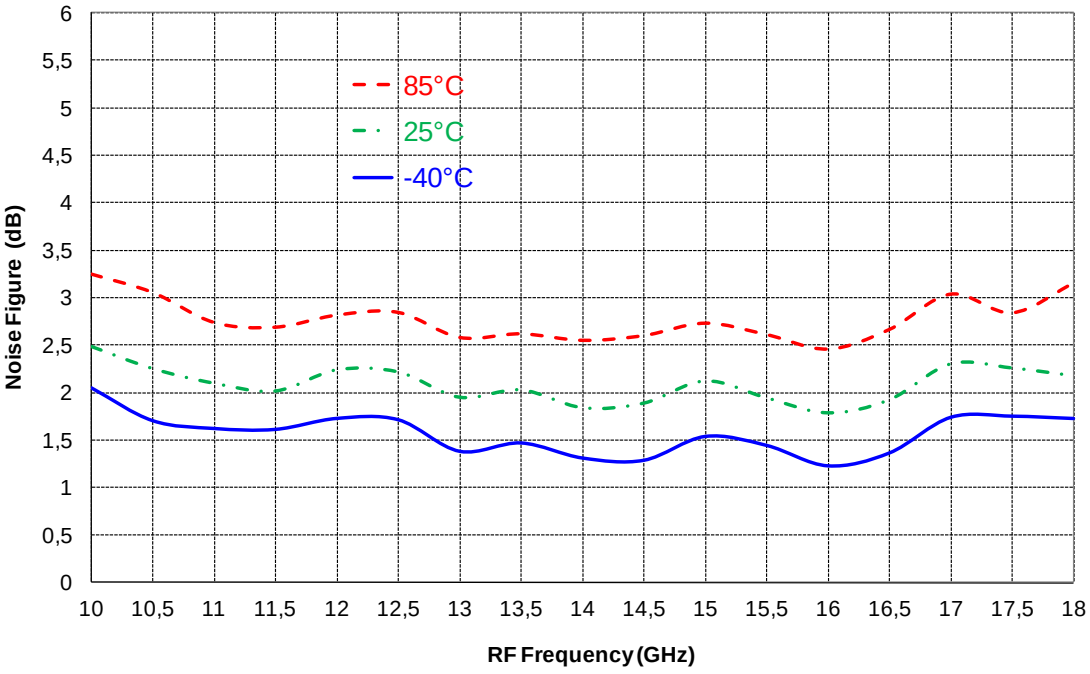
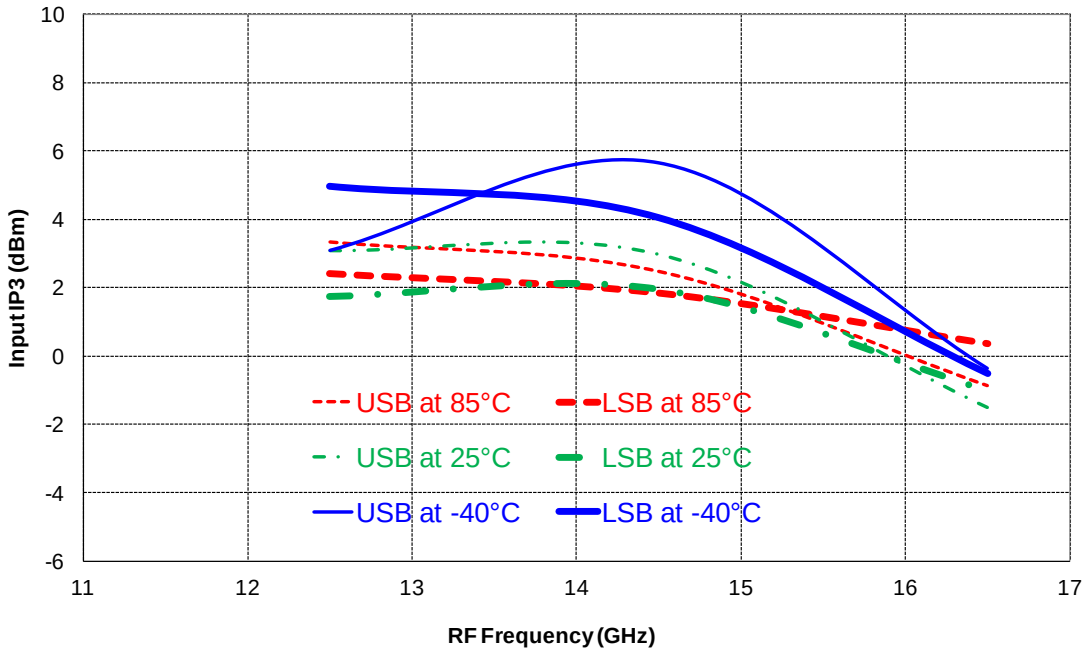
Typical Board Measurements

Tamb.= +25°C, VD1= VD2= VD3= +3V, VG4= -1V, P_LO = +5dBm

Noise Figure versus temperature at IF = 3.5GHz
(USB mode)



Input IP3 versus temperature at IF = 2GHz
(USB & LSB modes – RF = -20dBm DCL)



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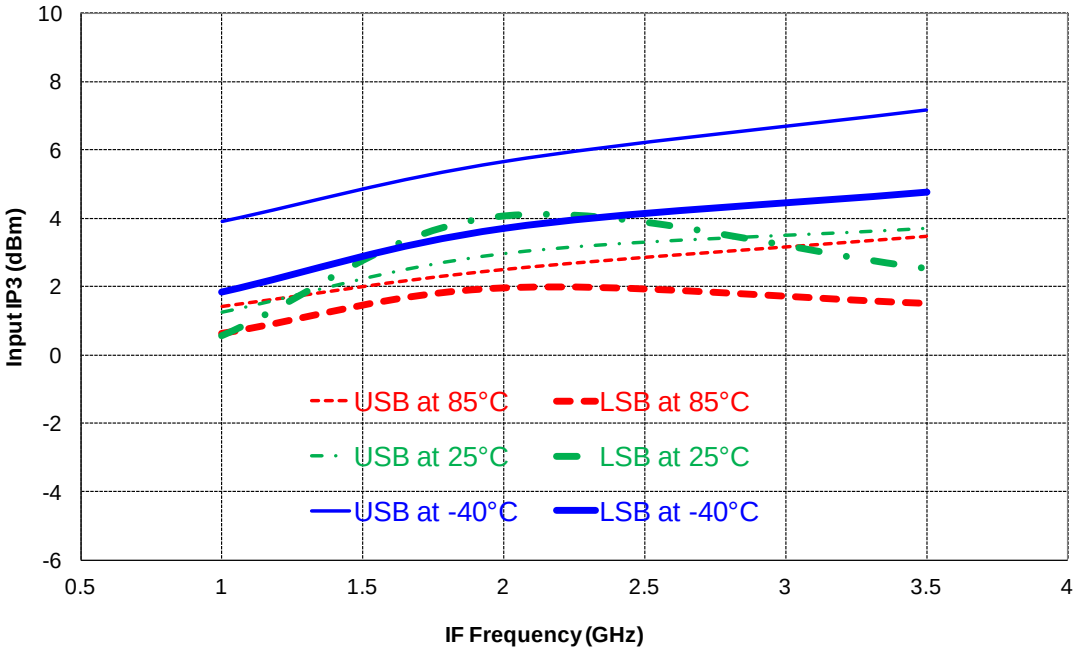
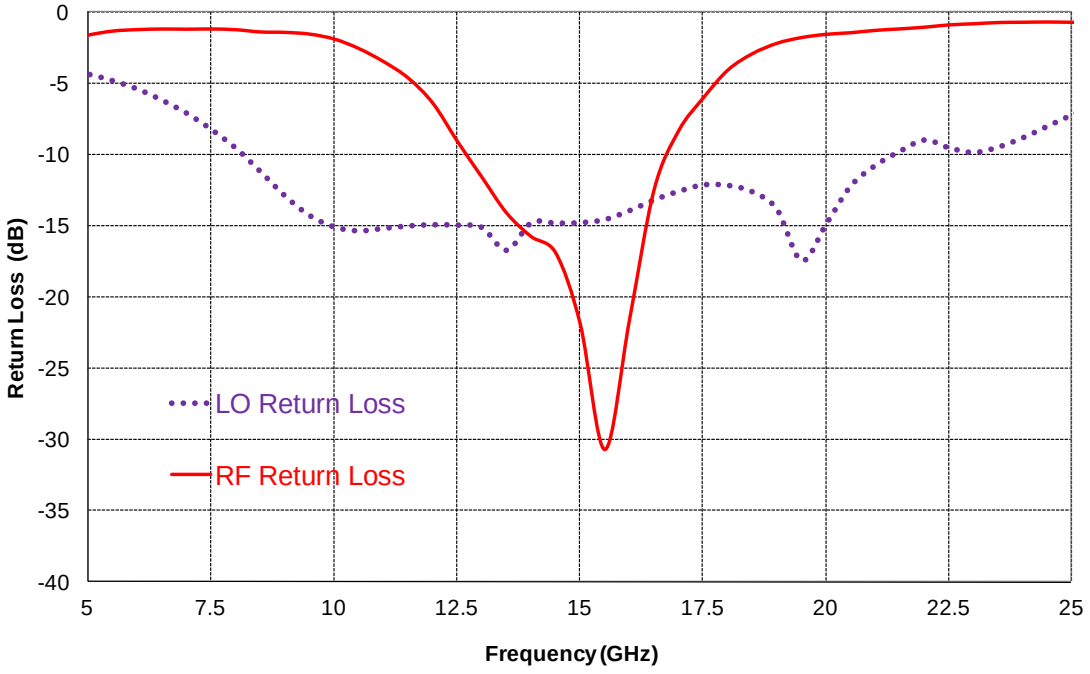
Typical Board Measurements

Tamb.= +25°C, VD1= VD2= VD3= +3V, VG4= -1V, P_LO = +5dBm

Input IP3 versus temperature at RF = 14.5GHz
(USB & LSB modes – RF = -20dBm DCL)



Return Loss LO & RF



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Typical Board Measurements

Tamb.= +25°C, VD1= VD2= VD3= +3V, VG4= -1V, P_LO = +5dBm

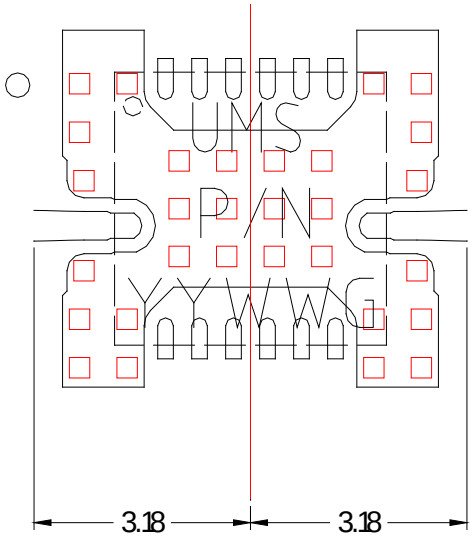
Spurious on IF outputs
RF = LO + IF
P_RF = -20dBm @ 14.5GHz / P_LO = +5dBm @ 12.5GHz

	nLO				
mRF	**0**	**1**	**2**	**3**	**4**
0	**xx**	**13**	**27**	**47**	**>90**
1	**23**	**0**	**38**	**44**	**>90**
2	**>90**	**60**	**29**	**50**	**58**
3	**>90**	**>90**	**>90**	**53**	**>90**
4	**>90**	**>90**	**>90**	**>90**	**>90**

All values in dBc below IF power level (IF = 2GHz).
Data measured without external hybrid coupler.

Definition of the package access planes

The package access planes are symmetrical from the axis of the package (see drawing beside). The input and output reference planes are located at 3.18mm offset (input wise and output wise respectively) from this axis.



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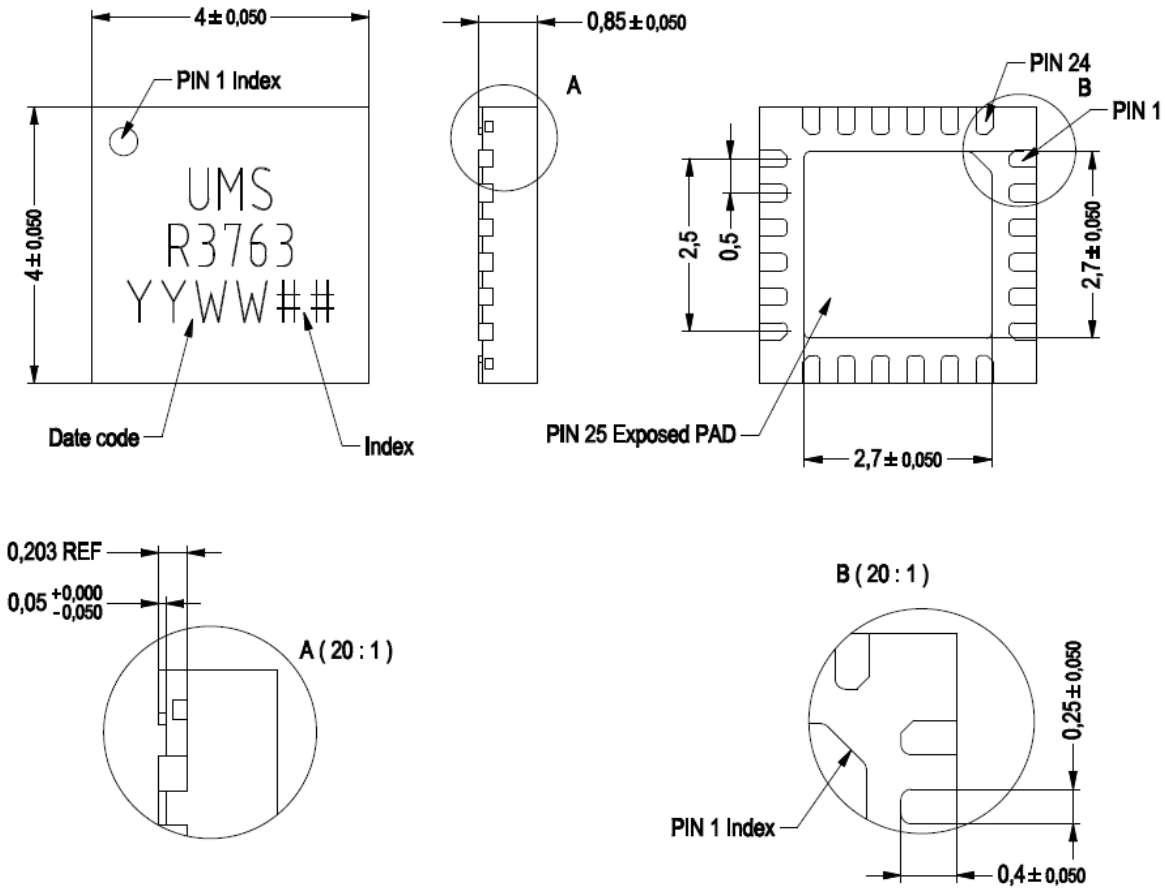
Package outline (1)



Matt tin, Lead Free (Green)	1- Nc	9- RF in	17- VG4
Units : mm	2- IF_Q	10- Gnd(2)	18- VD3
From the standard : JEDEC MO-220 (VGGD)	3- Gnd(2)	11- Nc	19- VG3
	4- Gnd(2)	12- VG1	20- Nc
25- GND	5- IF_I	13- VD1	21- Gnd(2)
	6- Nc	14- VG2	22- LO in
	7- Nc	15- VD2	23- Gnd(2)
	8- Gnd(2)	16- Nc	24- Nc

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (http://www.ums-gaas.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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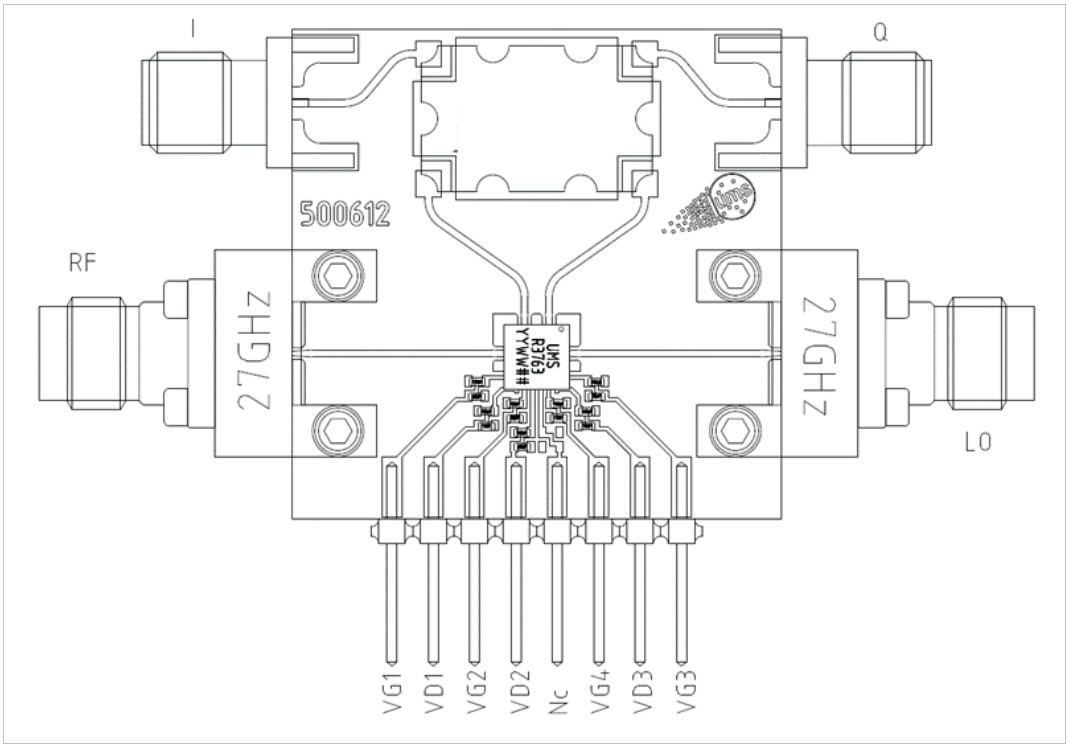
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for implementation of this product on a module board.
- Decoupling capacitors of 100pF ±5% and 10nF ±10% are recommended for all DC accesses.
- See application note AN0017 for details.
- Hybrid coupler 90° for 1-2GHz or 2-4GHz.



Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.

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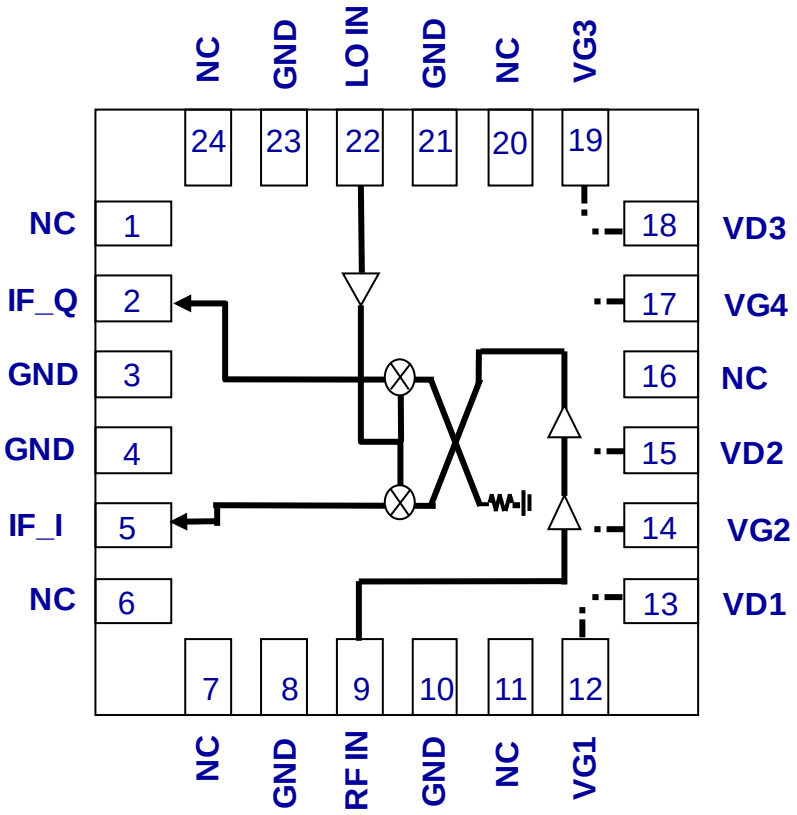
Notes



ESD protections are implemented on gate DC bias accesses and RF input.
The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (100pF + 10nF) on the PC board, as close as possible to the package.

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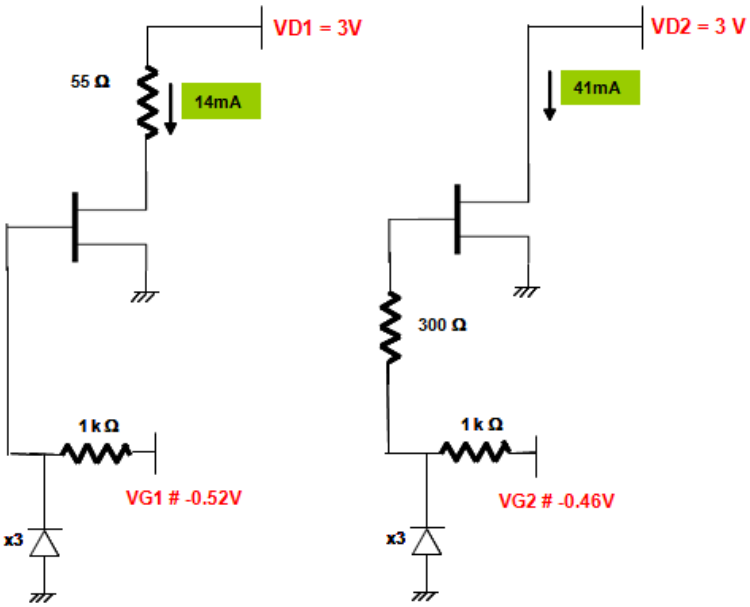
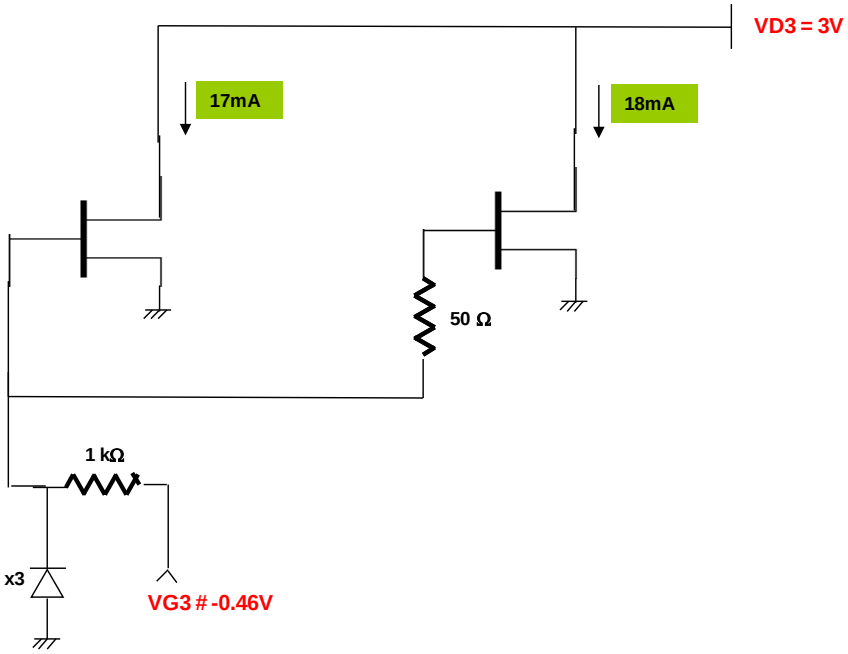
DC Schematic

LNA: 3V, 45mA



LO Buffer: 3V, 35mA



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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x4 package:	CHR3763-QDG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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