CHR3394-QEG

37-40GHz Down Converter

GaAs Monolithic Microwave IC in SMD leadless package

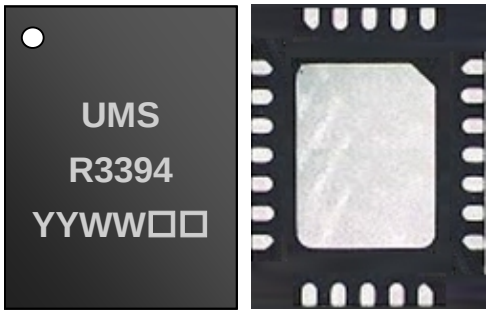
Description

The CHR3394-QEG is a multifunction monolithic receiver, which integrates a balanced cold FET mixer, a LO chain with buffers associated to a time two multiplier, and a RF Low Noise Amplifier.

It is designed for a wide range of applications, from military to commercial communication systems.

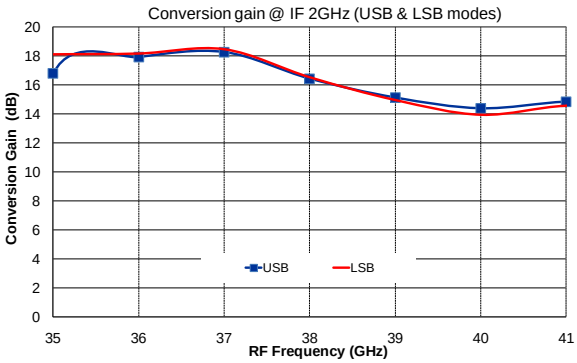
The circuit is manufactured with a pHEMT process, 0.15µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is supplied in RoHS compliant SMD package.



Main Features

- Broadband performances: 37-40.15GHz
- 13dB Conversion gain
- 15dBc Image Rejection
- 1dBm IIP3
- 3.5dB Noise Figure for IF>0.1GHz
- 0dBm LO input Power
- DC bias: Vd=4V @ Id=250mA
- 24L-QFN4x5
- MSL1



Main Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF frequency range	37		40.15	GHz
F_{LO}	LO frequency range	16.8		21.0	GHz
F_{IF}	IF frequency range	DC		3.5	GHz
G	Conversion gain	8	13		dB

United Monolithic Semiconductors S.A.S.
Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

Specifications

Tamb.= +25°C, VD = VD1 = +4V (1)

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF frequency range	37		40.15	GHz
F_{LO}	LO frequency range	16.8		21.0	GHz
F_{IF}	IF frequency range	DC		3.5	GHz
G	Conversion gain (2)	8	13		dB
NF	Noise Figure for IF>0.1GHz		3.5	6	dB
Im_rej	Image rejection (2)	12	15		dBc
P_{LO}	LO Input power		0		dBm
P1dB	RF input Power at 1 dB compression	-17	-8		dBm
IIP3	Input IP3	-6	1		dBm
LO RL	LO return loss		-12	-10	dB
RF RL	RF return loss		-6	-5	dB
VGL	LNA DC gate voltage		-0.1		V
VGX	Multiplier DC gate voltage		-0.9		V
IDt	Total Drain current (ID+ID1) (3)		250		mA

These values are representative of on-board measurements.

(1) VD: LO-chain drain bias voltage. VD1: LNA drain bias voltage.

(2) An external combiner 90° is required on I/Q.

(3) ID: LO-chain drain current, typically 125mA.
(3) ID1: LNA drain current, typically 125mA, should be tuned with VGL.

Electrostatic discharge sensitive device observe handling precautions!

“Power ON” sequence

1. Bias LNA gate voltage VGL at Vg close to Vpinch-off (Typically: Vg ≈ -1V)
2. Bias LO chain VGX at -0.9V
3. Apply 4V on VD and VD1
4. Increase slowly LNA gate voltage VGL up to quiescent bias drain current Idq =125 mA
5. Apply RF signal

“Power OFF” sequence

1. Turn off RF signal
2. Bias LNA gate voltage VGL at Vg close to Vpinch-off (Typically: Vg ≈ -1V)
3. Turn VD and VD1 bias voltage to 0V
4. Turn both LO chain VGX bias voltage and LNA gate voltage VGL to 0V

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
VD, VD1	Drain bias voltages	4.5V	V
IDt	Drain bias current	350	mA
VGL, VGX	Gate bias voltages	-2 to +0.4	V
P_RF	Maximum peak input power overdrive (2)	+15	dBm
P_LO	Maximum LO input power	+15	dBm
Tj	Junction temperature	175	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s.

Recommended Operating Range 3, 4

Symbol	Parameter	Values	Unit
VD, VD1	Drain bias voltage	3.3 to 4	V
Id	Drain bias current	200 to 250	mA
VGL, VGX	Gate bias voltage	-1 to 0	V
P_LO	LO input power	-2 to +8	dBm
P_RF	RF power	-30 to -10	dBm

(3) Electrical performances are defined for specified test conditions
(4) Electrical performances are not guaranteed over all recommended operating conditions

Temperature Range

Ta	Operating temperature range	-40 to +95	°C
Tstg	Storage temperature range	-55 to +155	°C

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad Nº	Parameter	Values	Unit
VD1, VD	10, 11	DC drain voltages (LNA and LO-chain)	4	V
ID1	10	LNA drain current controlled with VGL	125	mA
VGL	9	LNA DC gate voltage	-0.1	V
VGX	12	Multiplier DC gate voltage	-0.9	V

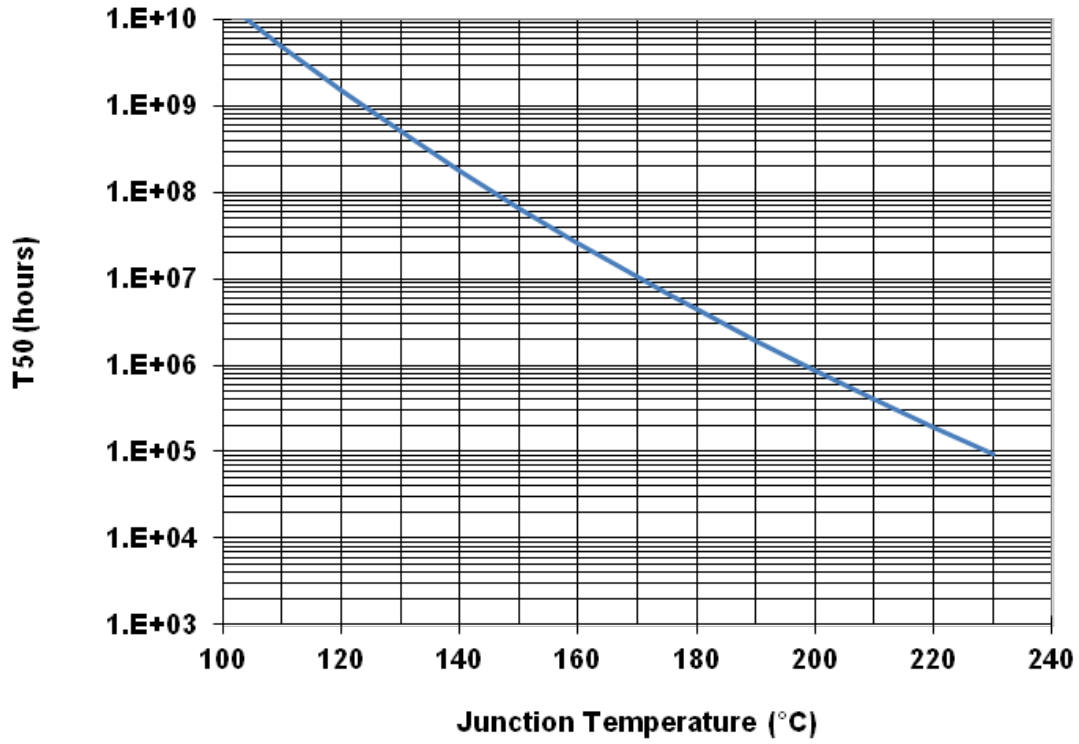
Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is only cooled down by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tcase).
The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Absolute Maximum Ratings table.
So, the system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	Tjunction (°C)	R_{TH} (°C/W)	T50 (hours)
R_{TH} (1) Thermal Resistance (Junction to Case)	Vd= 4V Id= 250mA Pdiss= 1W	147	62	8.8E+08

[1] Assuming 85°C Tcase

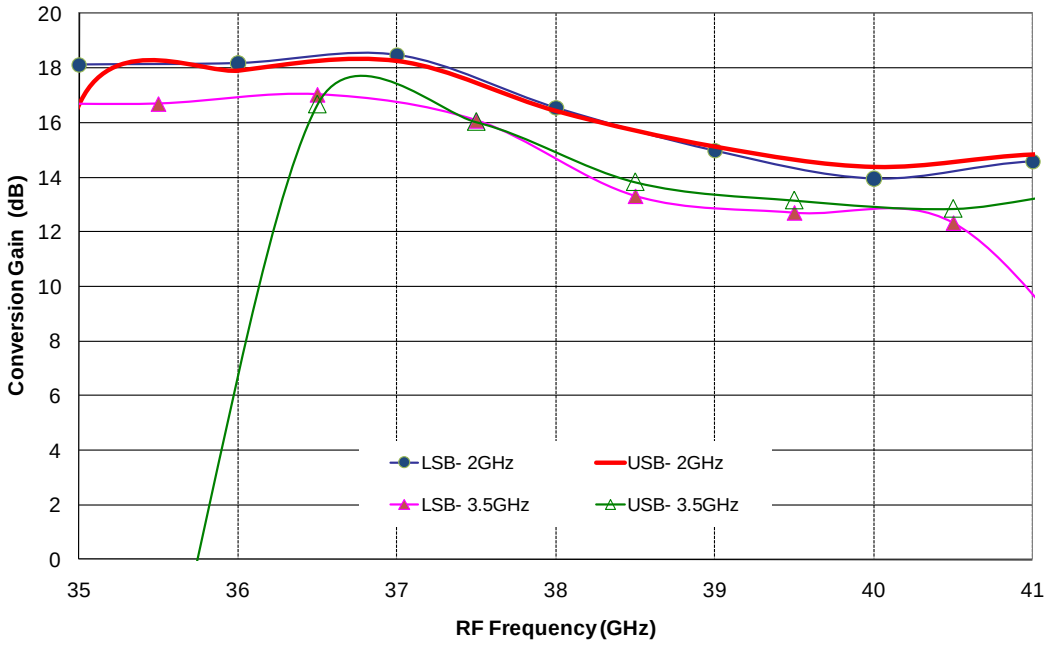


Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

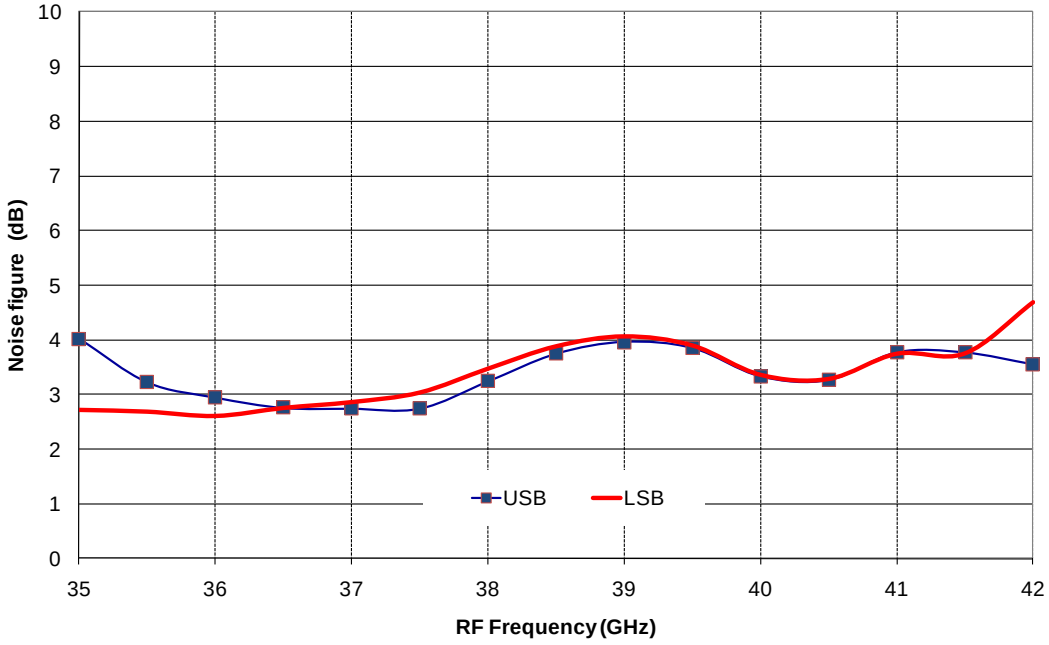
Typical Board Measurements

Tamb.= +25°C, VD = VD1 =+4V, VGL = -0.1V, VGX = -0.9V, P_LO = 0dBm (IDt = 250mA)
These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board". Data given in the package access planes.

Conversion Gain versus RF & IF frequency (USB & LSB modes)



Noise figure versus RF frequency at IF 3GHz

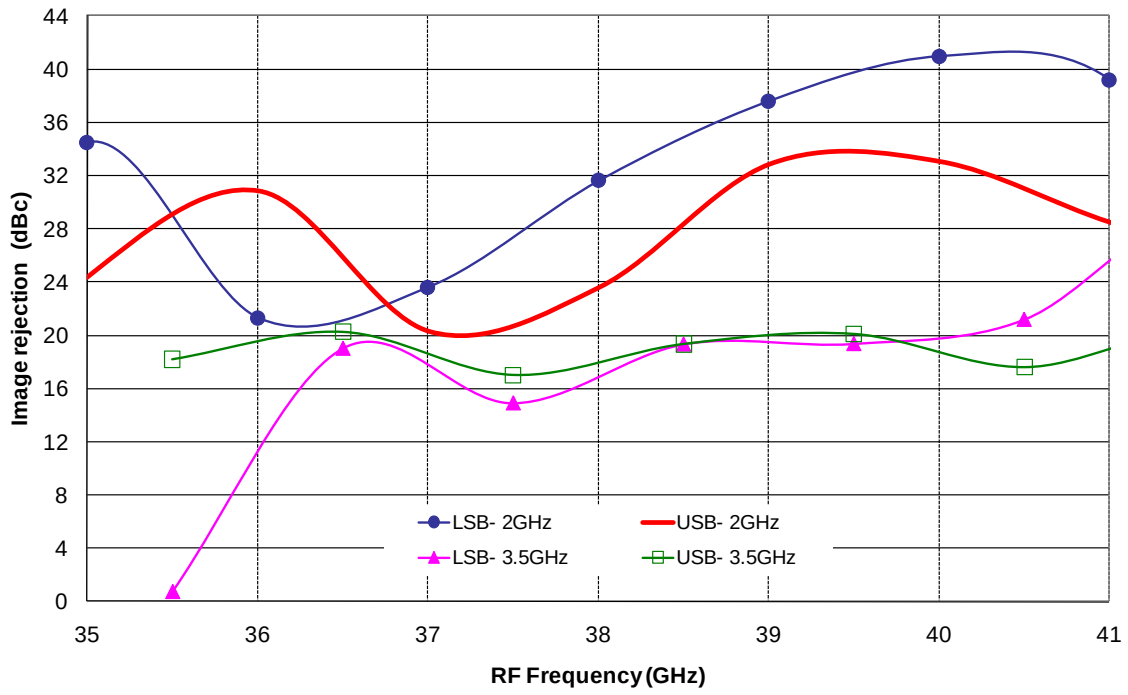


Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

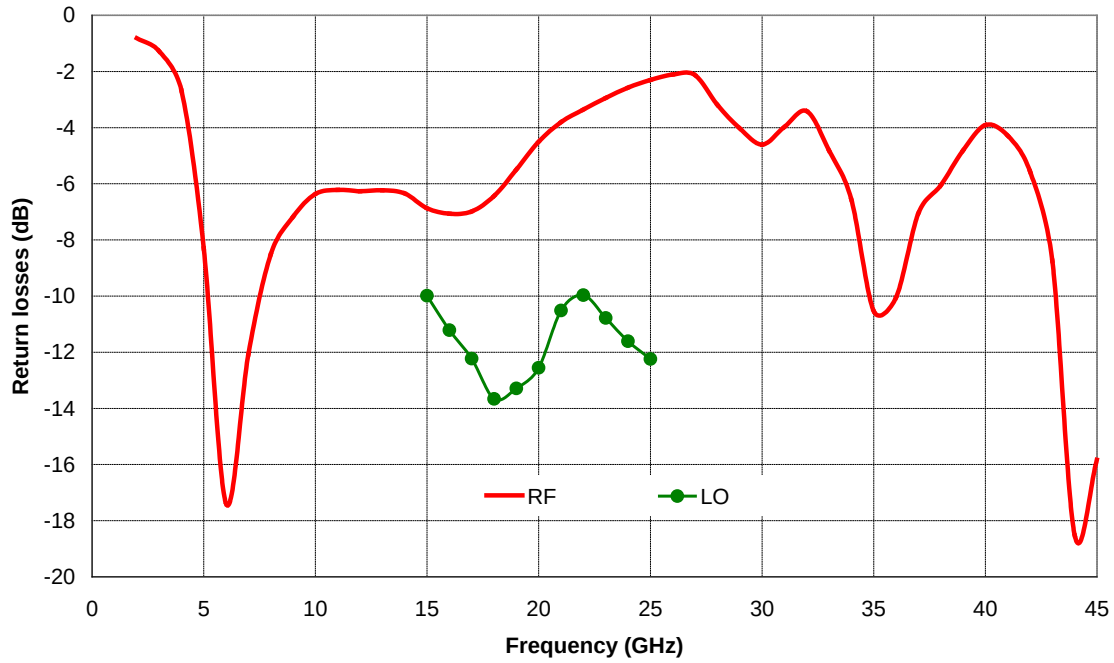
Typical Board Measurements

Tamb.= +25°C, VD = VD1 = +4V, VGL = -0.1V, VGX = -0.9V, P_LO = 0dBm (IDt = 250mA)

Image rejection versus RF & IF frequency



Return Losses (LO & RF) versus frequency

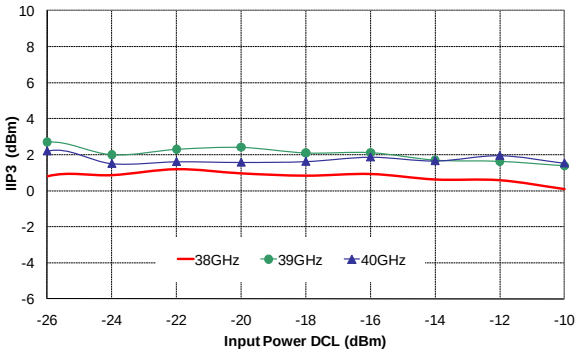


Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

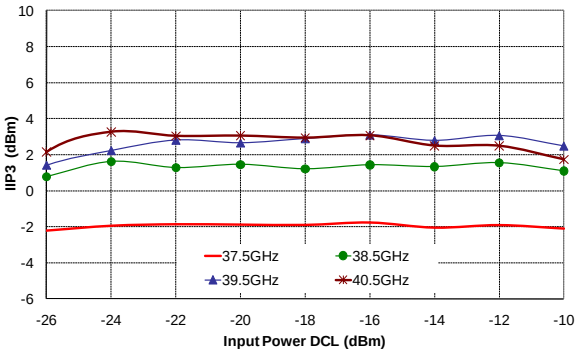
Typical Board Measurements

Tamb.= +25°C, VD = VD1 = +4V, VGL = -0.1V, VGX = -0.9V, P_LO = 0dBm (IDt = 250mA)

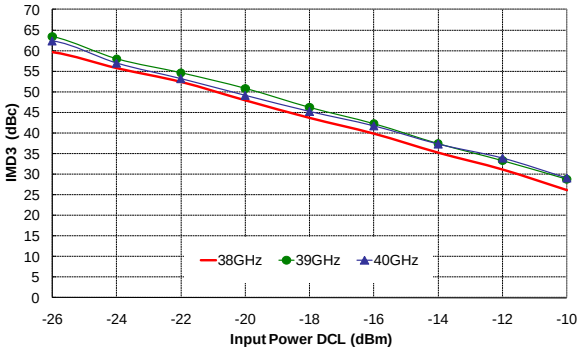
Input IP3 vs RF frequency at IF 2GHz



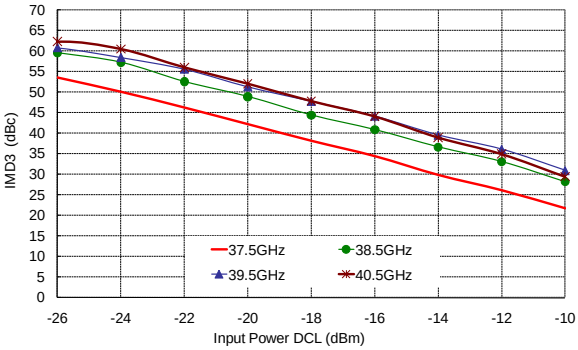
Input IP3 vs RF frequency at IF 3.5GHz



IMD3 vs RF frequency at IF 2GHz



IMD3 vs RF frequency at IF 3.5GHz

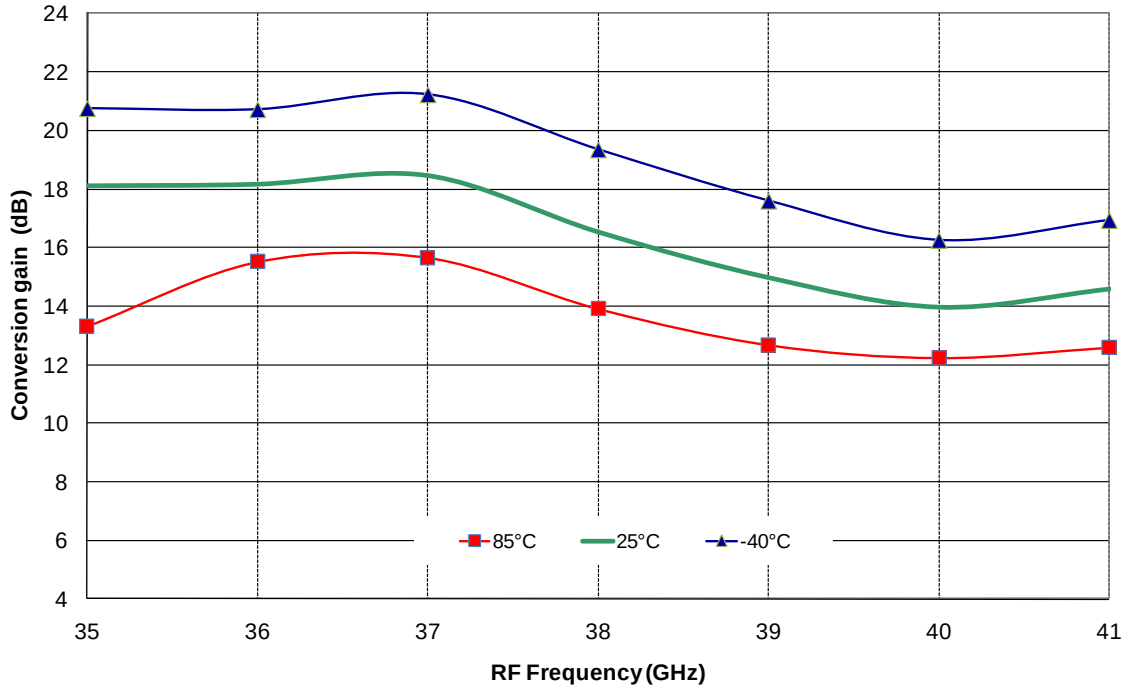


Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

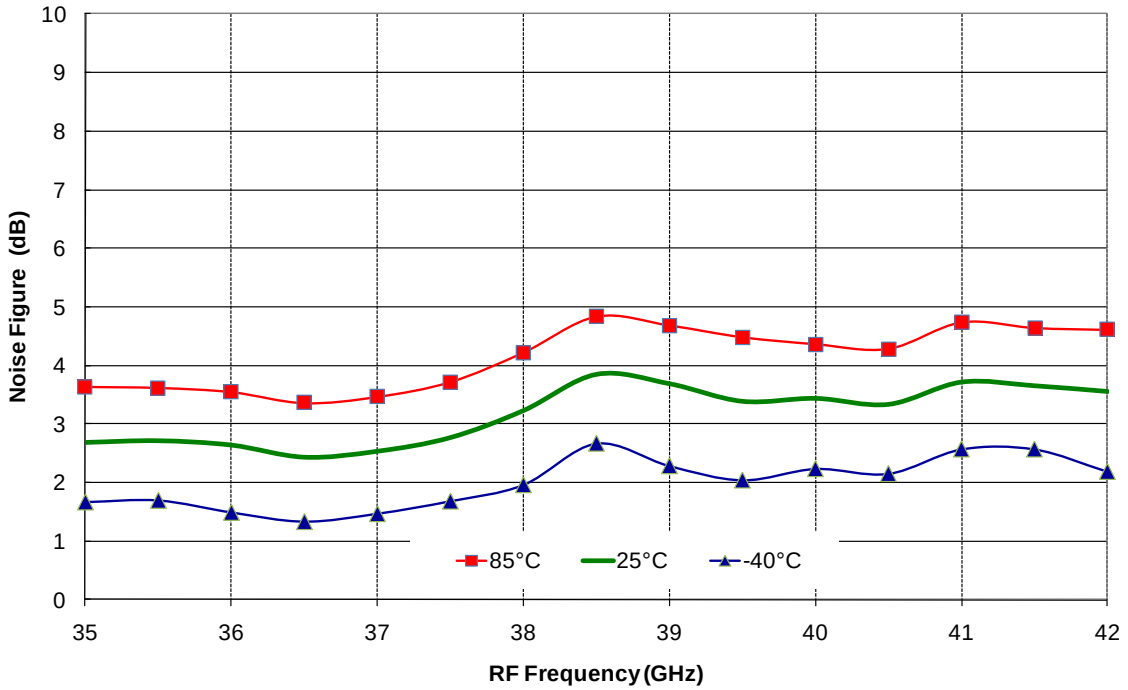
Typical Board Measurements

Tamb = +25°C, Tcold = -40°C, Thot = +85°C
VD = VD1 = +4V, VGL = -0.1V, VGX = -0.9V, P_LO = 0dBm

Conversion Gain versus temperature at IF 2 GHz (USB mode)



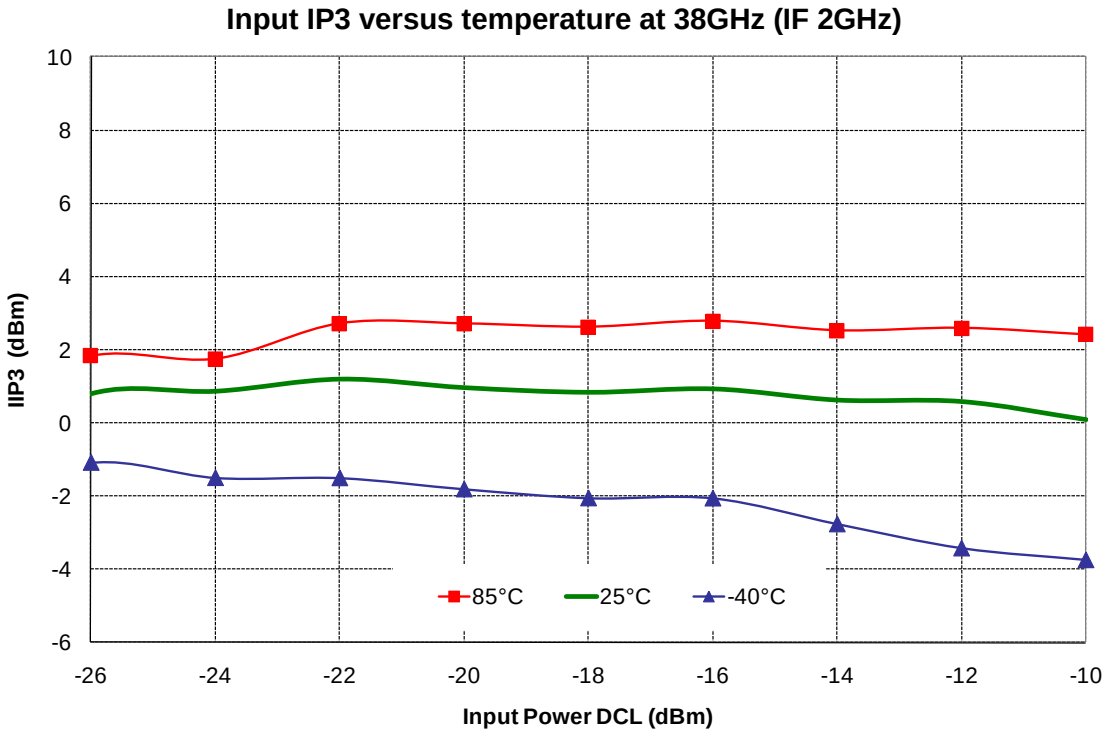
Noise figure versus temperature at IF 2GHz (USB mode)



Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

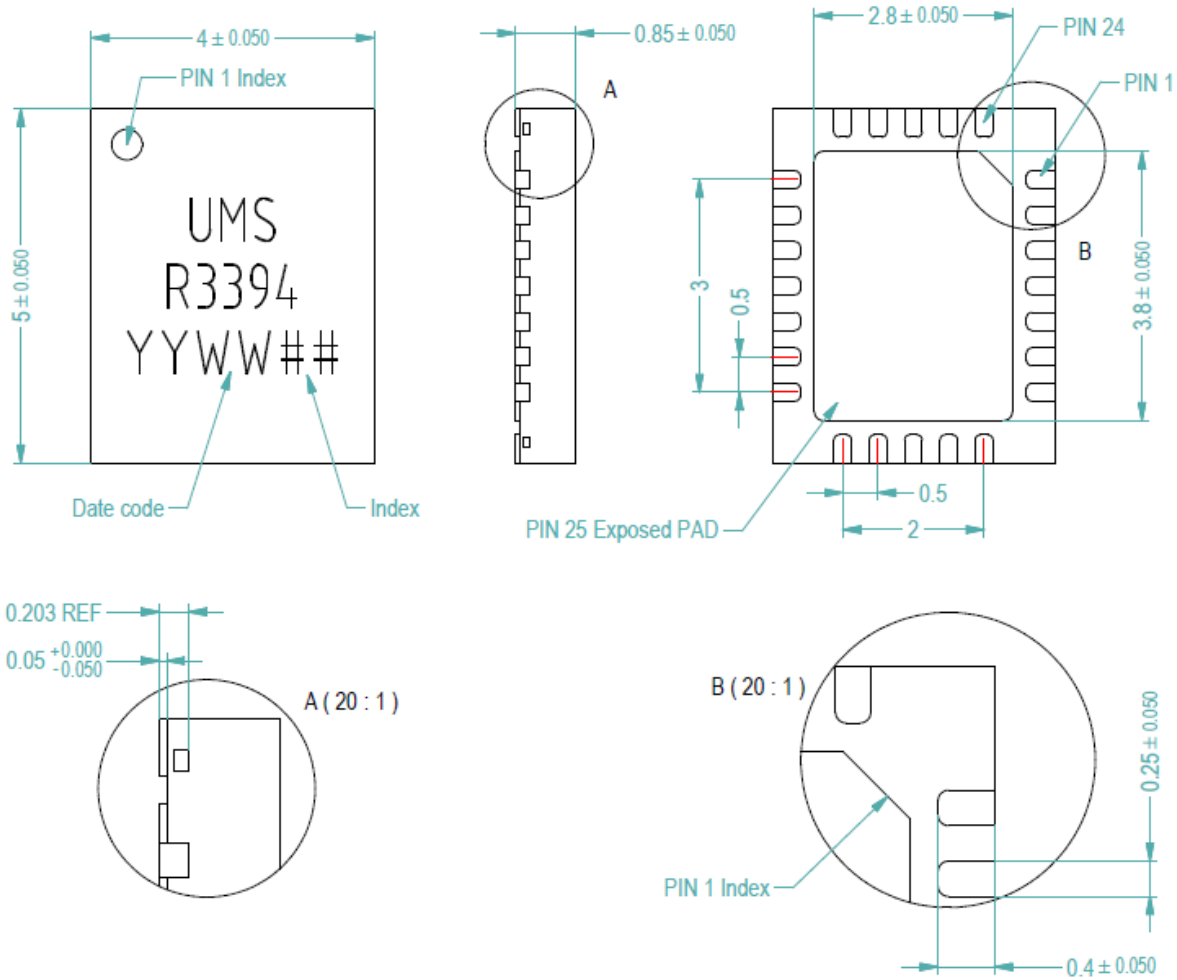
Typical Board Measurements

Tamb = +25°C, Tcold = -40°C, Thot = +85°C
VD = VD1 = +4V, VGL = -0.1V, VGX = -0.9V, P_LO = 0dBm

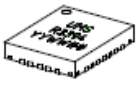


Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

Package outline (1)



Units : mm
Finish : Matt tin
Lead free (Green)



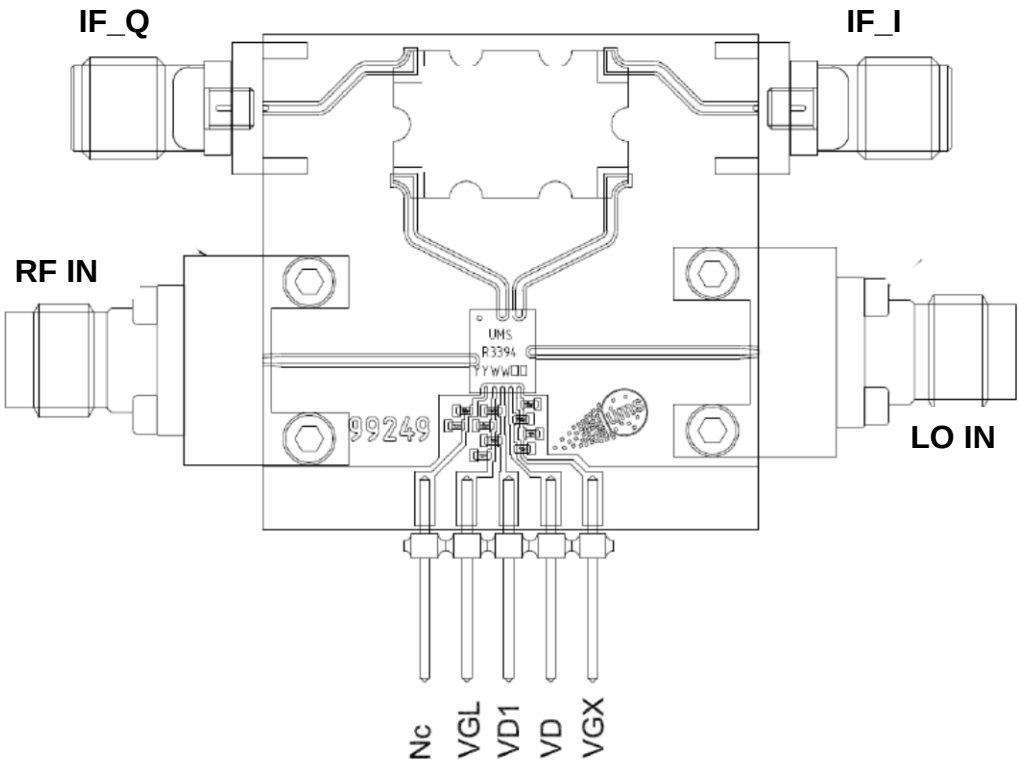
Matte tin, Lead Free (Green)	1- Nc	9- VGL	17- Gnd(2)
Units : mm	2- Nc	10- VD1	18- Nc
From the standard : JEDEC MO-220	3- Nc	11- VD	19- Nc
(VGGD)	4- Gnd(2)	12- VGX	20- IF_I
25- GND	5- RF in	13- Nc	21- Gnd(2)
	6- Gnd(2)	14- Nc	22- IF_Q
	7- Nc	15- Gnd(2)	23- Nc
	8- Nc	16- LO in	24- Nc

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (http://www.ums-gaas.com) for exact package dimensions.
(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.
- See application note AN0017 for details.
- Hybrid coupler 90° for 2-4GHz.

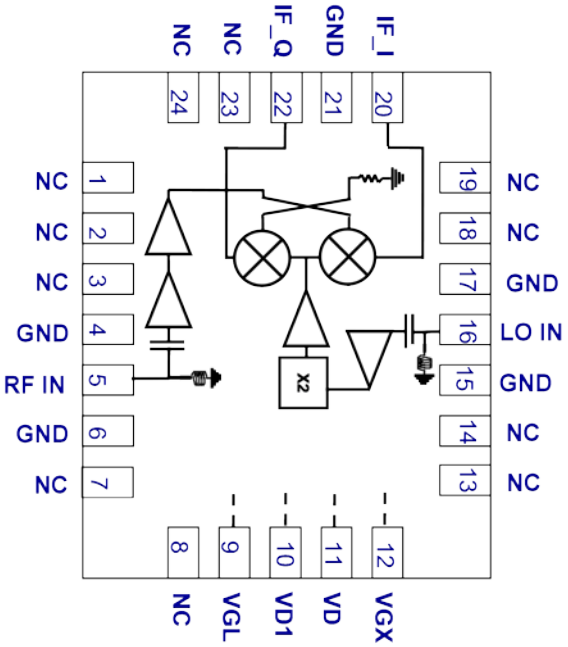


Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

Notes

Due to ESD protection circuits on RF and LO inputs, an external capacitance might be requested to isolate the product from external voltage that could be present on these accesses.

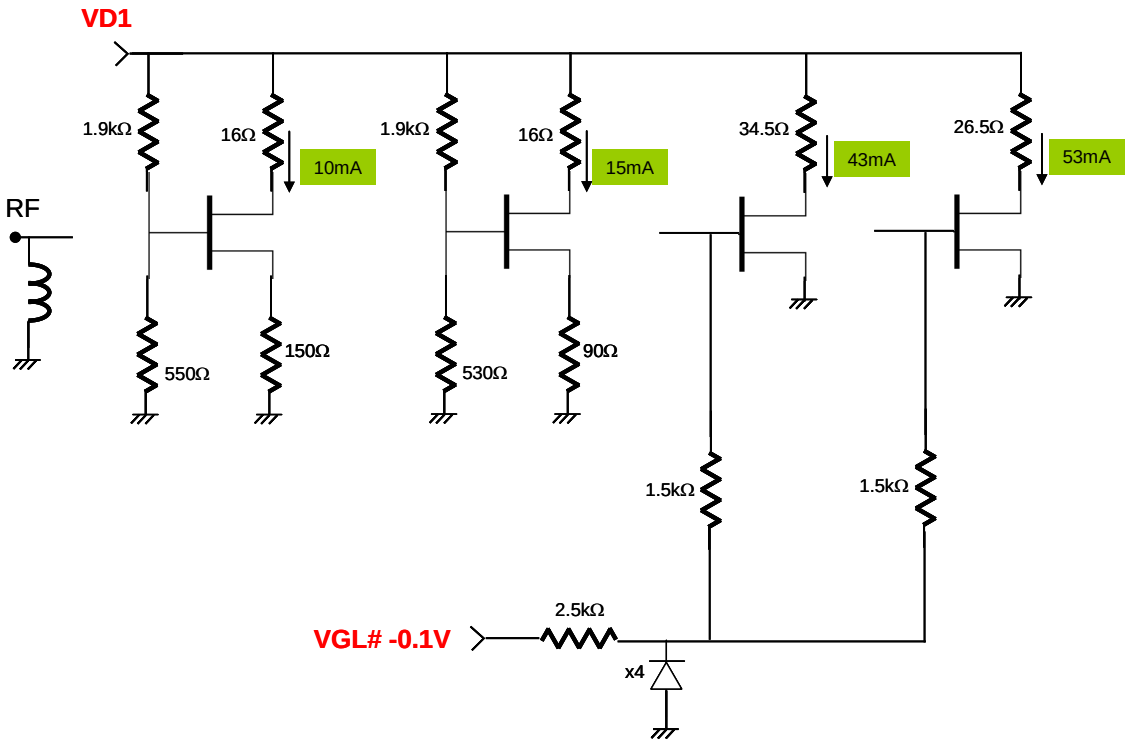


ESD protections are also implemented on gate access.
The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (10nF) on the PC board, as close as possible to the package.

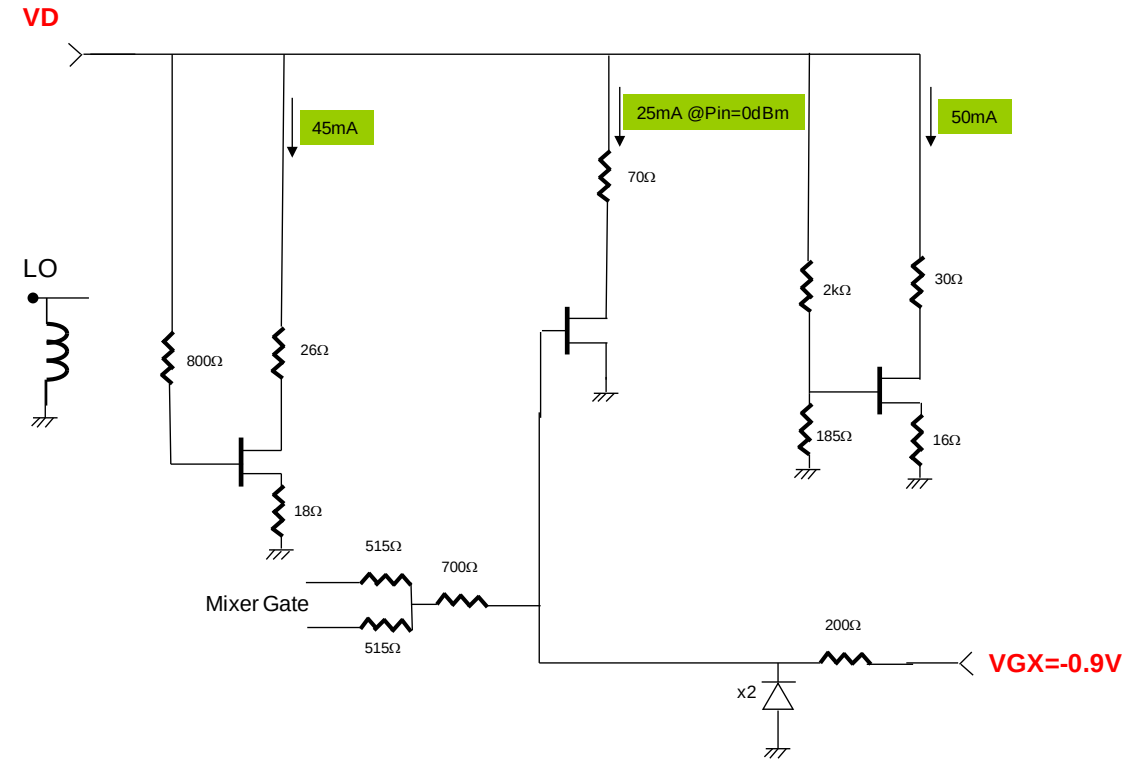
Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

DC Schematic

LNA: 4V, 125mA



LO chain: 4V, 125mA



Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x4 package:	CHR3394-QEG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com