United Monolithic Semiconductors

CHR1080a98F

71-86GHz Down-converter

GaAs Monolithic Microwave IC

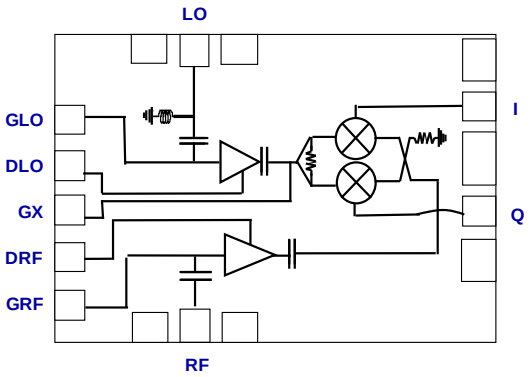
Description

The CHR1080a98F is a multifunction monolithic receiver, which integrates a balanced sub-harmonic cold FET mixer, a LO buffer, and a RF low noise amplifier.

It is designed for the E-band telecommunication application, particularly well suited for the new generation of high capacity backhaul.

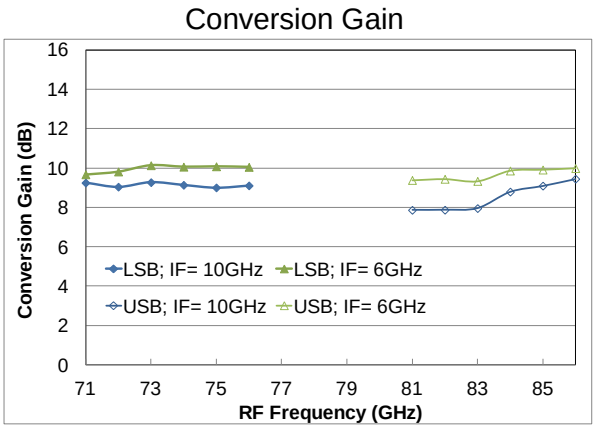
The circuit is manufactured with a pHEMT process, 0.10µm gate length.

It is available in chip form.



Main Features

- Broadband RF performances: 71-86GHz
- 8dB Conversion Gain
- 5dB Noise Figure
- -10dBm Input Power at 1dB compression
- DC bias: Vd=3.5V @Id=175mA
- Chip size 3.43x2.24x0.07mm



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF Frequency	71		86	GHz
F_{IF}	IF frequency	DC		12	GHz
G	Conversion gain		8		dB
NF	Noise Figure		5		dB

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Electrical Characteristics

Tamb.= +25°C, Vd = 3.5V

Symbol	Parameter	Min	Typ	Max	Unit
FRF	RF Frequency range	71		86	GHz
FLO	LO Frequency range	34.5		44	GHz
FIF	IF output Frequency	DC	10	12	GHz
PLO	LO input power	0	1		dBm
Gc	Conversion gain (1)		8		dB
R_LO	LO input return loss		8		dB
R_RF	RF input return loss		10		dB
NF	Noise Figure		5		dB
Im_rej	Image rejection (1)		16		dBc
2LO Leak.	2LO Leakage to RF port		-38		dBm
RFin P1dB	RF Input power @1dB compression		-10		dBm
Idt	Drain current (Id LO Buffer +Id LNA) (2)		175		mA
DLO, DRF	DC drain voltage (LO Buffer, LNA)		3.5		V
GLO, GX, GRF	LO Buffer, Mixer, LNA DC gate voltage		-2		V

(1) An external combiner 90° is required on I / Q.

(2) LO drain quiescent current 85mA, LNA drain quiescent current 90mA.

These values are representative of on-wafer measurements made without bonding wires at the RF & LO ports.
A ribbon (75 µm wide) connection at the RF and LO inputs (see chapter recommended chip assembly) could improve the results.

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4V	V
Idt	Drain bias current	240	mA
Vg	Gate bias voltage	-3.0 to -1.4	V
Pin_LO	Maximum LO peak input power overdrive (2)	+10	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s.

Typical Bias Conditions

Tamb.= +25°C

Pad name	Pad N°	Parameter	Typical Values	Unit
GRF	6	LNA DC gate voltage (1)	-2	V
DRF	7	LNA DC drain voltage (90mA)	3.5	V
GX	8	Mixer DC gate voltage	-2	V
DLO	10	LO Buffer DC drain voltage (85mA)	3.5	V
GLO	12	LO Buffer DC gate voltage	-2.2	V
	5, 9, 11	Not connected		

(1) LNA gate voltage could be adjusted between -3.0V and -1.4V to perform gain control

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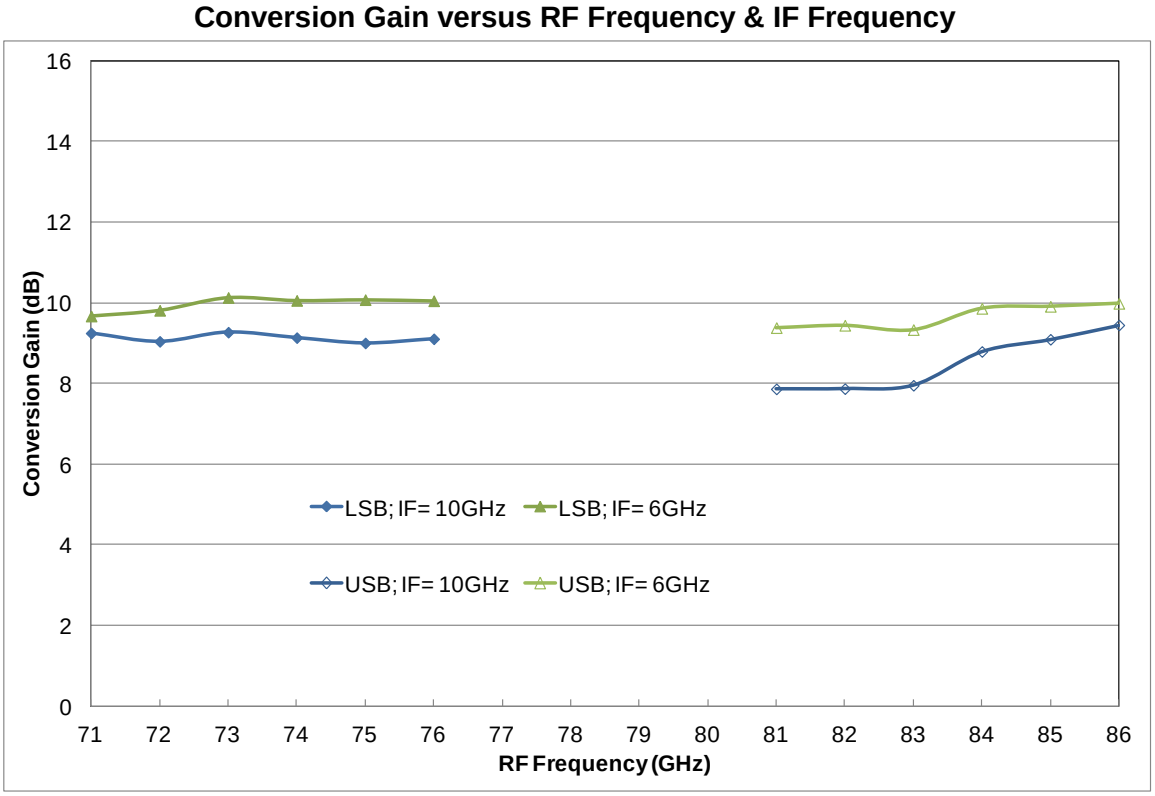
Typical on wafer Measurements

Tamb.= +25°C, Vd = +3.5V

Without specific comment:
GLO= -2.2V, GX= -2V, Pin_RF= -30dBm, Pin_LO= 1dBm, IF frequency = 10GHz
GRF to be tuned for I_DRF= 90mA (GRF close to -2V)
LSB: RF= 2LO- IF; USB: RF= 2LO+ IF



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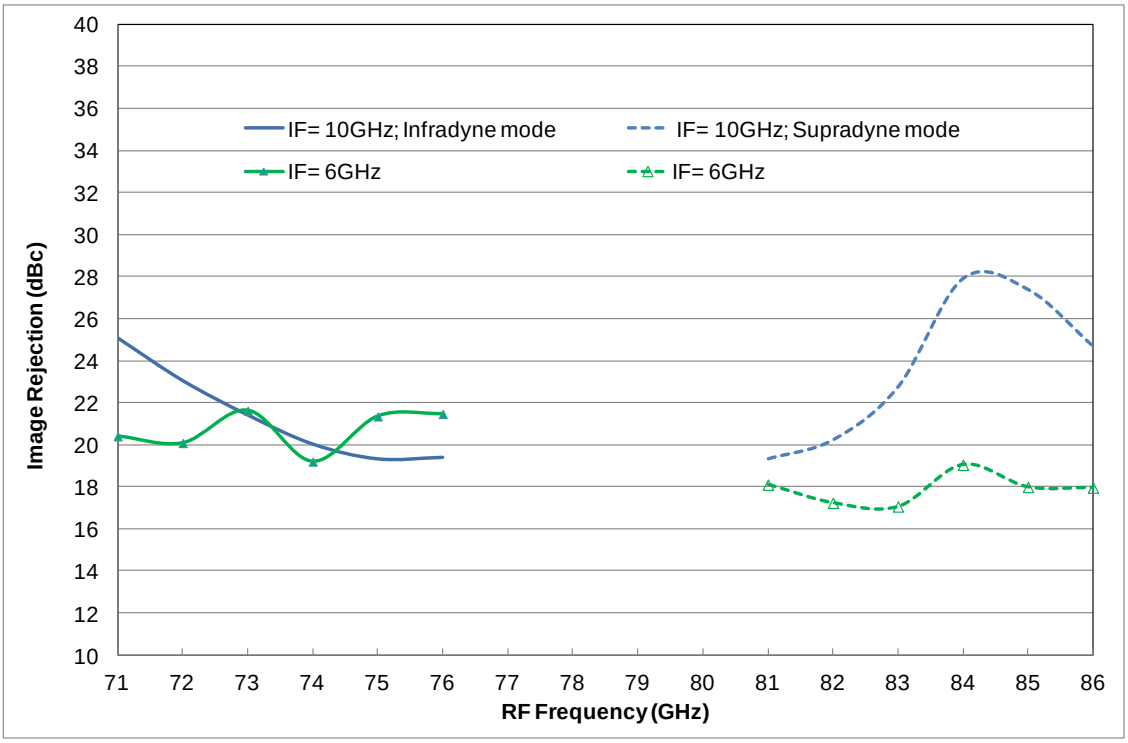
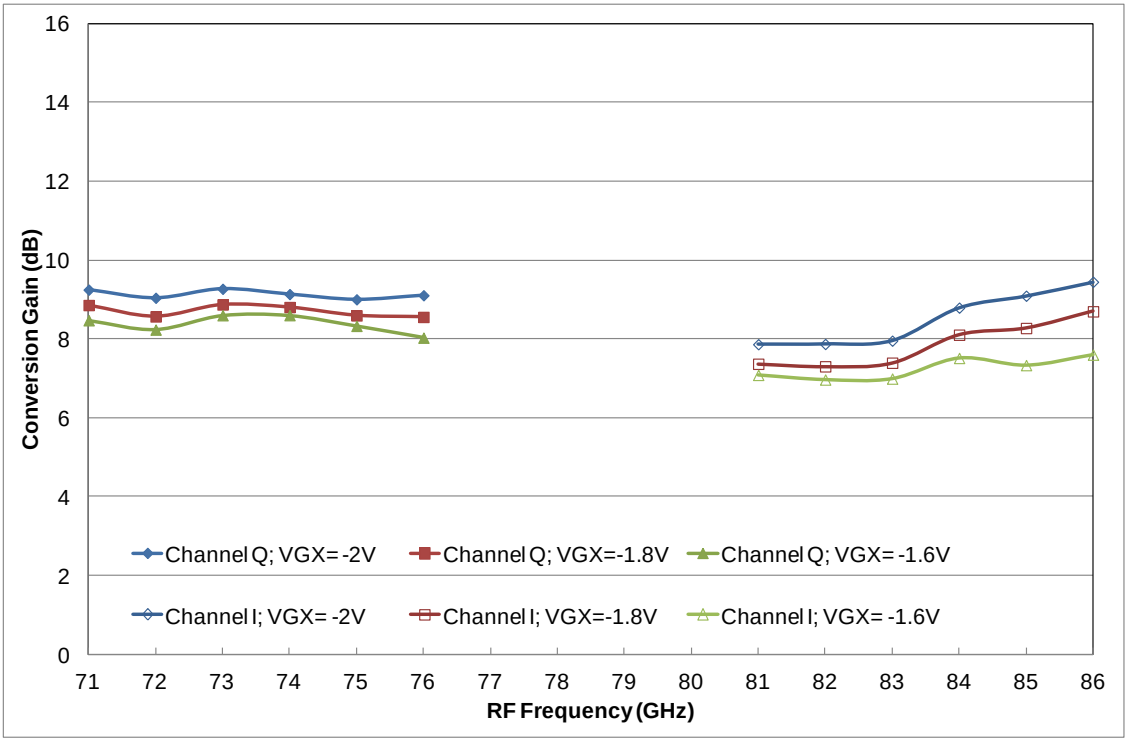
Typical on wafer Measurements

Tamb.= +25°C, Vd = +3.5V

Image rejection versus RF Frequency & IF Frequency



Conversion Gain versus RF Frequency & Mixer voltage



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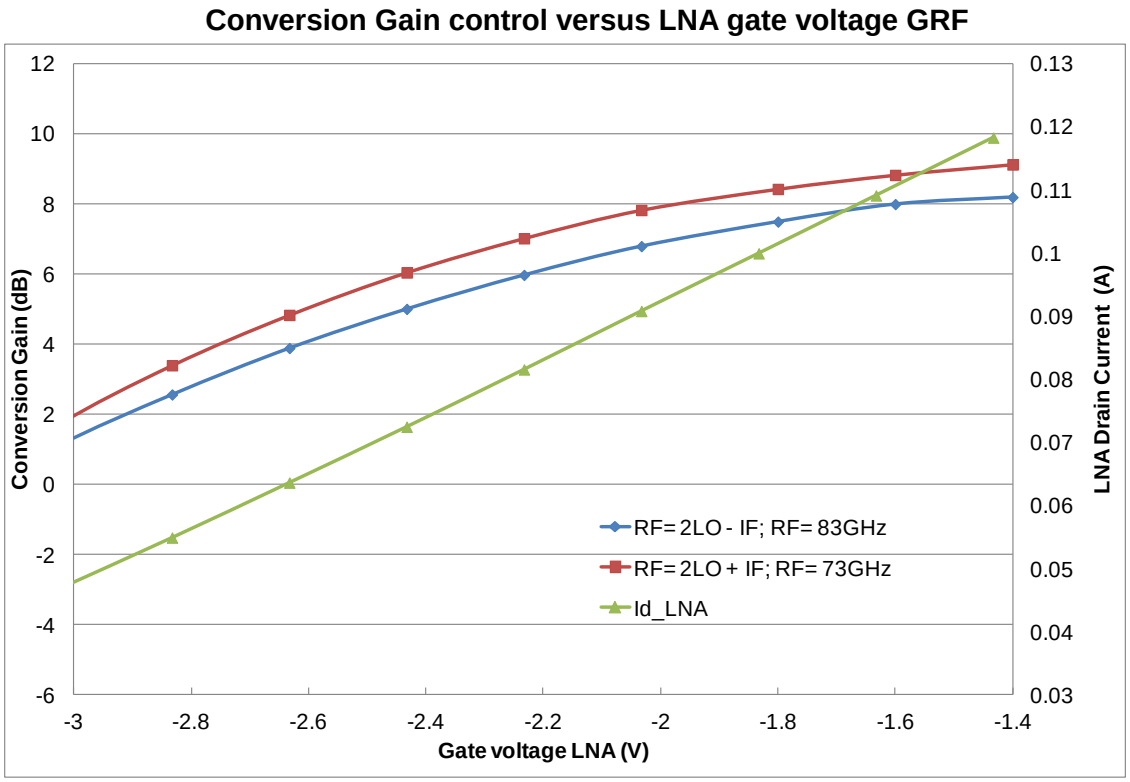
Typical on wafer Measurements

Tamb.= +25°C, Vd = +3.5V



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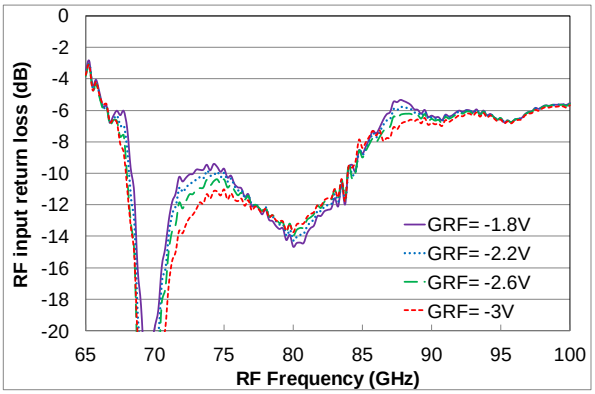
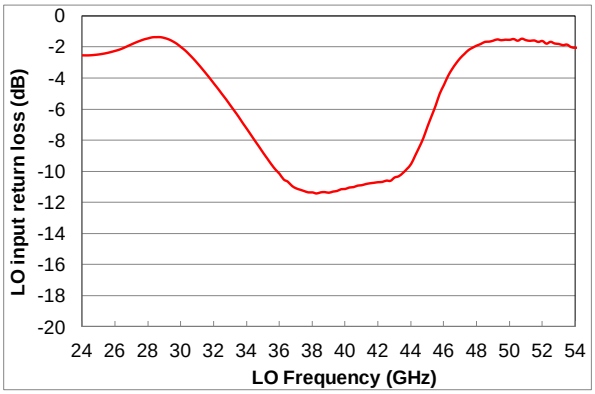
Typical on wafer Measurements

Tamb.= +25°C, Vd = +3.5V

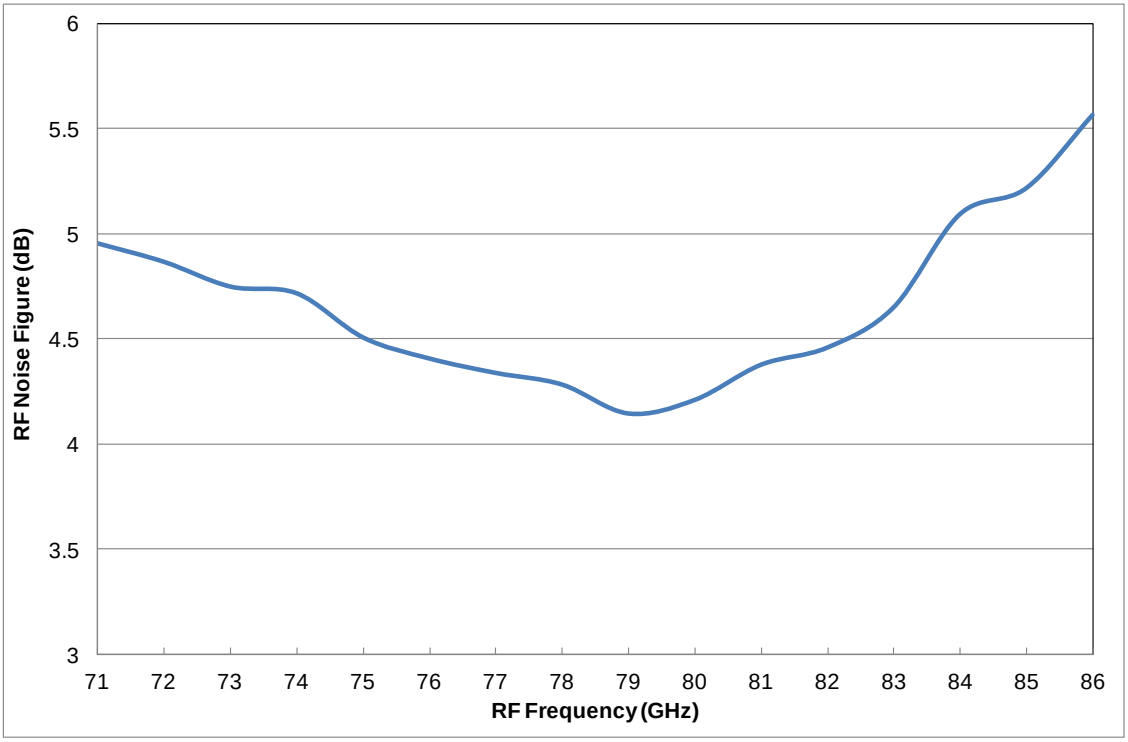
RF return loss vs gate voltage GRF



LO return loss versus Frequency



Noise figure versus Frequency



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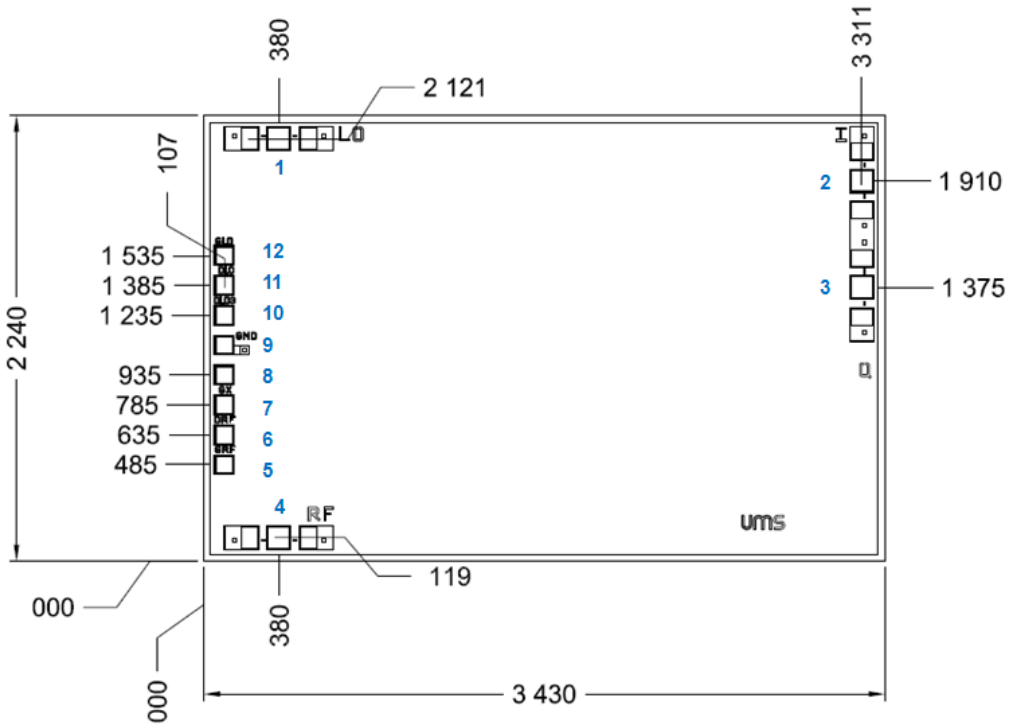
Mechanical data



Chip thickness: 70µm.
Chip size: 3430x2240 ±35µm
All dimensions are in micrometers

RF Pads = 108 x 106 (BCB opening)
DC Pads = 86 x 83 (BCB opening)

Recommended circuit bonding table

Pin number	Pin name	Description	Decoupling
1	**LO**	LO in	
2	**I**	IF (I)	
3	**Q**	IF (Q)	
4	**RF**	RF in	
6	**GRF**	DC LNA Gate Voltage (-2V)	120pF, 10nF
7	**DRF**	DC LNA drain Voltage (3.5V)	120pF, 10nF
8	**GX**	DC Mixer Gate Voltage (-2V)	120pF, 10nF
11	**DLO3**	DC LO Buffer drain Voltage (3.5V)	120pF, 10nF
12	**GLO**	DC LO buffer Gate Voltage (-2.2V)	120pF, 10nF
5, 9, 10		Not connected	

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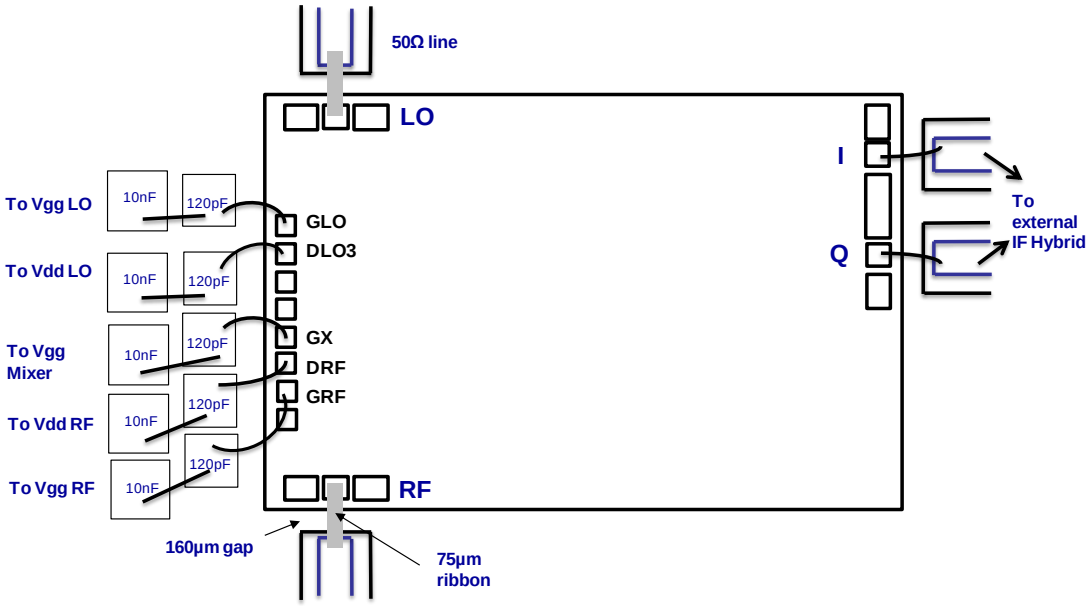
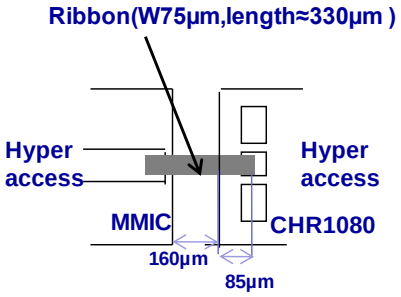
Recommended assembly plan



The design integrates a half ribbon (75µm wide) connection at the RF and LO input of the MMIC amplifier compliant with a 50Ohm line on GaAs MMIC.
Circuits having to be as close as possible to each other, the ribbon length must be reduced to the achievable minimum (160µm gap between two chips is considered) and the loop height must also be the smallest realizable (80µm).



A second solution is the use of double wires (Ø 25µm). In this case, a minimum of two wires and the same chip to chip distance as ribbon solution is necessary to reduce the inductance effect. Nevertheless, simulations have demonstrated an improvement of RF performance for E-band frequency range with the use of ribbon connection instead of wire.

Regarding the connection of the DC pads, a 25µm wedge bonding is preferred.

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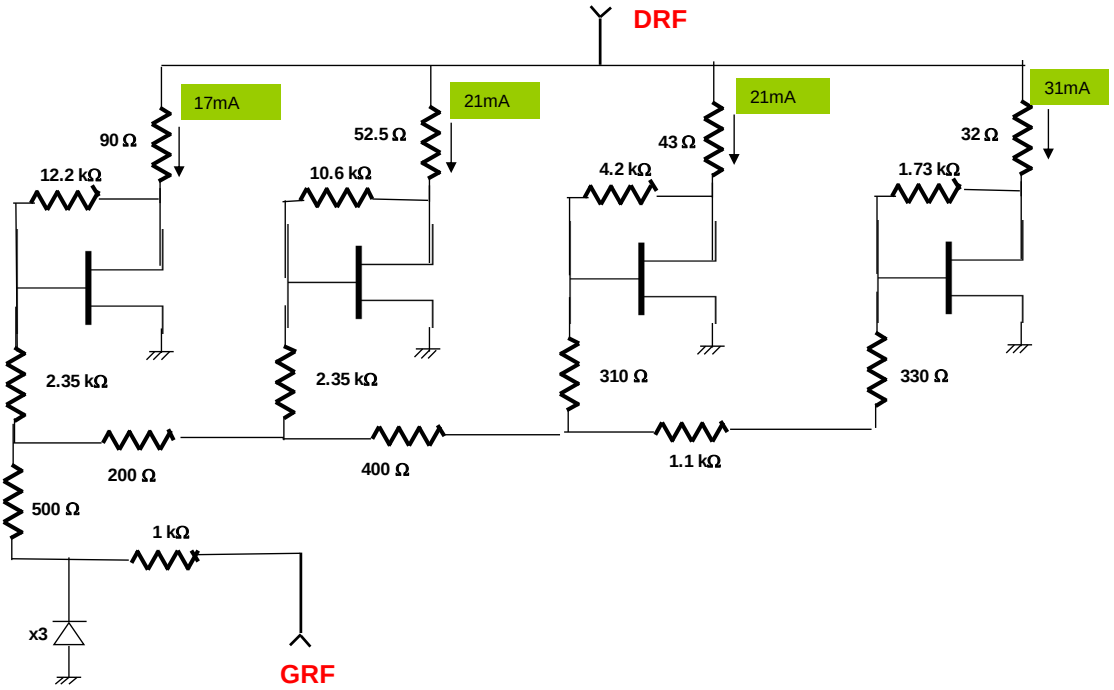
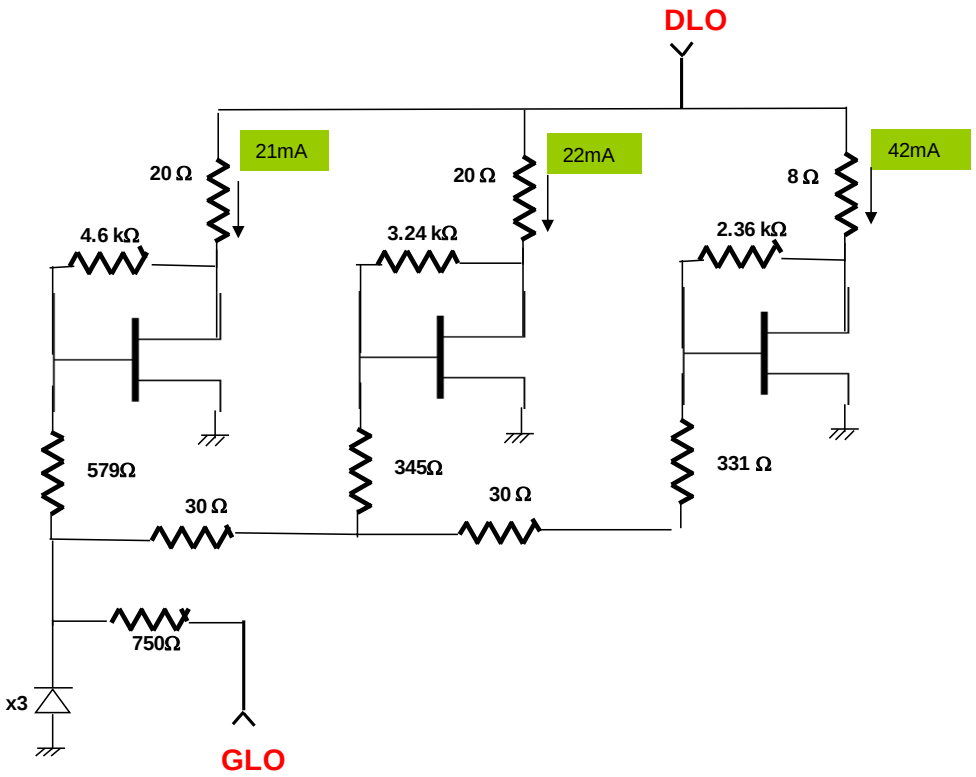
DC Schematic

LNA: 3.5V, 90mA



LO Buffer: 3.5V, 85mA



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Notes

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Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Ordering Information

Chip form:	CHR1080a98F/00

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