United Monolithic Semiconductors

CHKA011aSXA

130W Power Packaged Transistor

GaN HEMT on SiC packaged

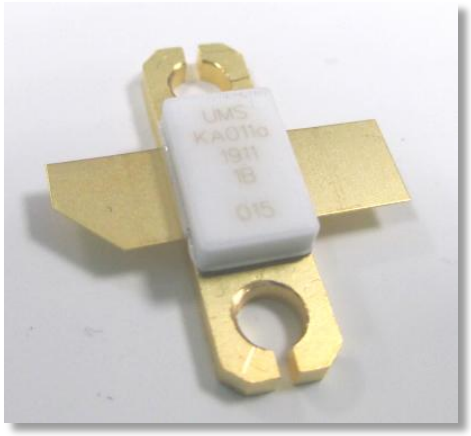
Description

The CHKA011aSXA is an unmatched packaged Gallium Nitride High Electron Mobility Transistor.

It offers general purpose and broadband solutions for a variety of RF power applications. It is well suited for multi-purpose applications such as radar and telecommunication.

The CHKA011aSXA is developed on a 0.5µm gate length GaN HEMT process. It requires an external matching circuitry.

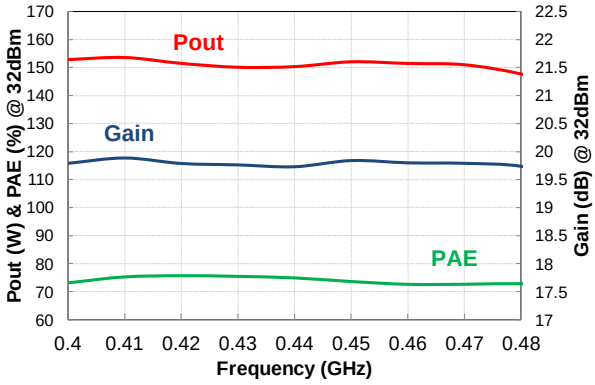
It is proposed in ceramic-metal flange power package, compliant with the RoHs N°2011/65 and REACH N°1907/2006 directives.



Main Features

- Wide band capability: up to 1.5GHz
- Pulsed and CW operating modes
- High power: > 130W
- High Efficiency: > 70%
- DC bias: Vd = 50Volt @ Id = 640mA
- Package: Ceramic-Metal
- MTTF > 10^6 hours @ Tj = 200°C

V_{DS} = 50V, I_{D_Q} = 640mA, Pin=32dBm
Pulsed mode (25µs, 10%)



Main Electrical Characteristics

Tcase= +25°C, Pulsed mode, V_{DS}=50V, I_{D_Q}=640mA, Freq=440MHz

Symbol	Parameter	Min	Typ	Max	Unit
G_{ss}	Small signal Gain	21	23.5		dB
P_{sat}	Saturated Output Power	130	150		W
G_{PAE_MAX}	Associated Gain at Max PAE		19.5		dB
$PAE_{\_MAX}$	Max Power Added Efficiency	70	75		%
I_{D_SAT}	Saturated Drain Current		4		A

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Recommended DC Operating Ratings

Tcase= +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{DS}	Drain to Source Voltage			50	V	
V_{GS_Q}	Gate to Source Voltage		-1.8		V	V_D=50V, I_{D_Q}=640mA
I_{D_Q}	Quiescent Drain Current		0.640	1.3	A	V_D=50V
I_{D_MAX}	Drain Current		4	(1)	A	V_D=50V, compressed mode
I_{G_MAX}	Gate Current (forward mode)		0	100	mA	Compressed mode
T_{j_MAX}	Junction temperature(1)			200	°C	

(1) Power dissipation must be considered

DC Characteristics

Tcase= +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_P	Pinch-Off Voltage	-2.7	-2	-1.5	V	V_D=50V, I_D= I_{DSS} /100
I_{D_SAT}	Saturated Drain Current		15.4 (1)		A	V_{DS}=10V, V_{GS}=1V
I_{G_leak}	Gate Leakage Current (reverse mode)	-2.6			mA	V_D=50V, V_G=-7V
V_{BDS}	Drain-Source Break-down Voltage		180		V	V_G=-7V, I_D=20mA

(1) For information, limited by I_{D_MAX}. see on Absolute Maximum Ratings

RF Characteristics

Tcase= +25°C, Pulsed mode, F = 440MHz

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
G_{ss}	Small signal Gain	21	23.5		dB	V_D=50V, I_{D_Q}=640mA
P_{sat}	Saturated Output Power	130	150		W	V_D=50V, I_{D_Q}=640mA
G_{PAE_MAX}	Associated Gain at Max PAE		19.5		dB	
$PAE_{\_MAX}$	Max Power Added Efficiency	70	75		%	V_D=50V, I_{D_Q}=640mA
I_{D_SAT}	Saturated Drain Current		4		A	V_D=50V, I_{D_Q}=640mA

These values are deduced from measurements and simulations. They are considered in the reference plane defined by the leads of the package, at the connection interface with the PCB.

The typical performance achievable in more than 10% frequency band around 0.44GHz was demonstrated using the reference board 61504318a presented hereafter.

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Absolute Maximum Ratings

Tcase= +25°C[(1) (2) (3)]

Symbol	Parameter	Rating	Unit	Note
V_{DS}	Drain-Source Biasing Voltage	60	V	
V_{GS_Q}	Gate-Source Biasing Voltage	-10, +2	V	
I_{G_MAX}	Maximum Gate Current (forward mode)	200	mA	
I_{G_MIN}	Minimum Gate Current (reverse mode)	-10	mA	
I_{D_MAX}	Maximum Drain Current	12	A	(4)
P_{IN}	Maximum Input Power			(5)
T_j	Junction Temperature	230	°C	
T_{STG}	Storage Temperature	-55 to +150	°C	
T_{Case}	Case Operating Temperature	See note	°C	(4)

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s.
(3) The given values must not be exceeded at the same time even momentarily for any parameter, since each parameter is independent from each other. Otherwise deterioration or destruction of the device may take place.
(4) Max junction temperature must be considered
(5) Linked to and limited by I_{G_MAX} & I_{G_MIN} values. Maximum input power depends on frequency and should not exceed 2dB above PAE_max.

Biasing procedure

1. Bias power bar gate voltage at V_{GS} close to V_p (Typically: $V_{GS} \approx$ -5V)
2. Apply V_{DS} bias voltage (Typically: V_{DS} = 50V)
3. Increase V_{GS} up to quiescent bias drain current I_{D_Q}

The quiescent current steady state must be carefully controlled as it is influenced by the operating mode, the temperature and the overall thermal resistance.
A drain current control is recommended on the biasing network.

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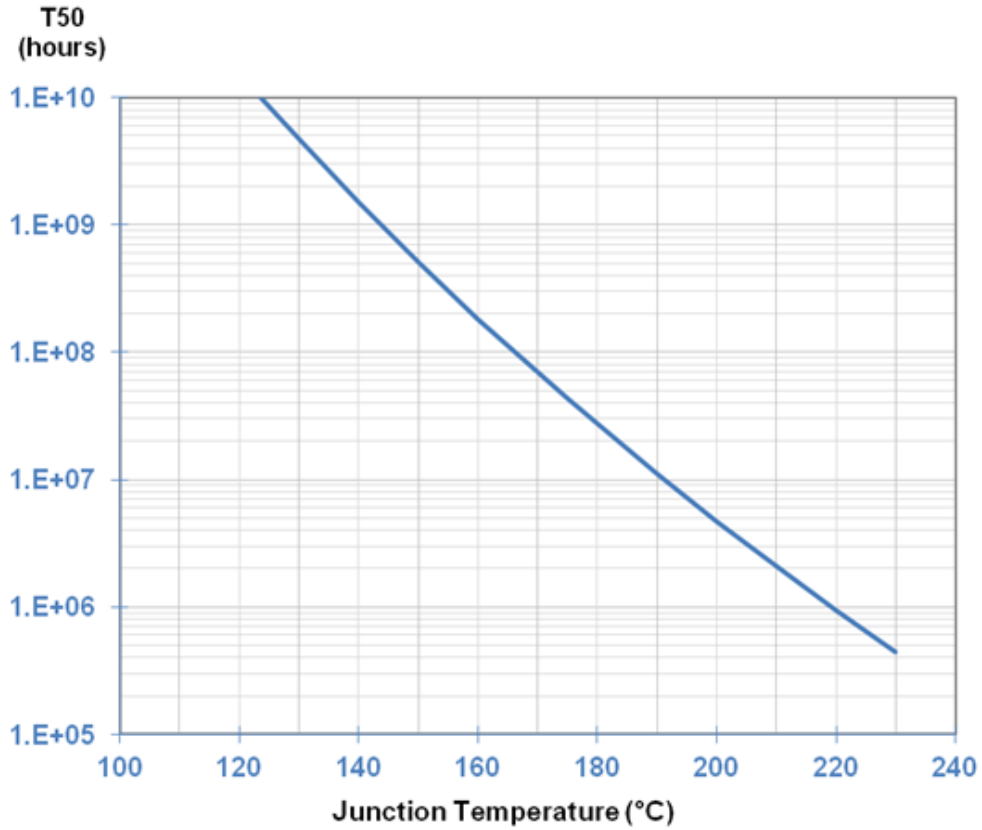
Device thermal information

The thermal performances of the device are based on UMS rules to evaluate the junction temperature (Tj). This temperature is defined as the peak temperature in the channel area.
This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHKA012a99F is fabricated (GaN Power HEMT 0.5µm).
The temperature Tcase is defined as the package back side temperature
The thermal resistance (Rth) is given in CW operating mode. The device assembly must be adapted to the operating mode. Thermal analysis is recommended. More information is available on request.

Typical Thermal Resistance	Rth	Packaged device Characteristic Tcase = 85°C Pdiss = 85W CW	1.36	°C/W
Junction Temperature	Tj		200	°C

The package back side temperature is considered uniform.

Median Life Time versus Junction Temperature



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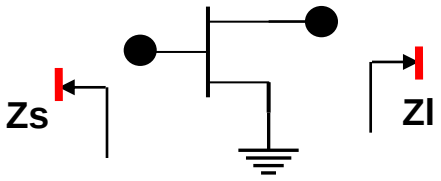
Simulated Source and Load Impedances

V_{DS} = 50V, I_{D_Q} = 640mA, Tcase= +25°C



The impedances are chosen as a trade-off between Output Power, PAE and Stability of the device.
These values are given in the reference plane defined by the connection between the transistor leads and the PCB. A gap of 200µm is considered between the edge of the package and the PCB.

Frequency (MHz)	Zs	Zl	Pout (W)	PAE (%)
500	3.03 + j1.14	6.43 + j3.7	180	76
1000	1.92 – j0.35	3.75 + j2.04	172	72.5
1500	1.46 – j1.9	2.96 - j0.1	161	69

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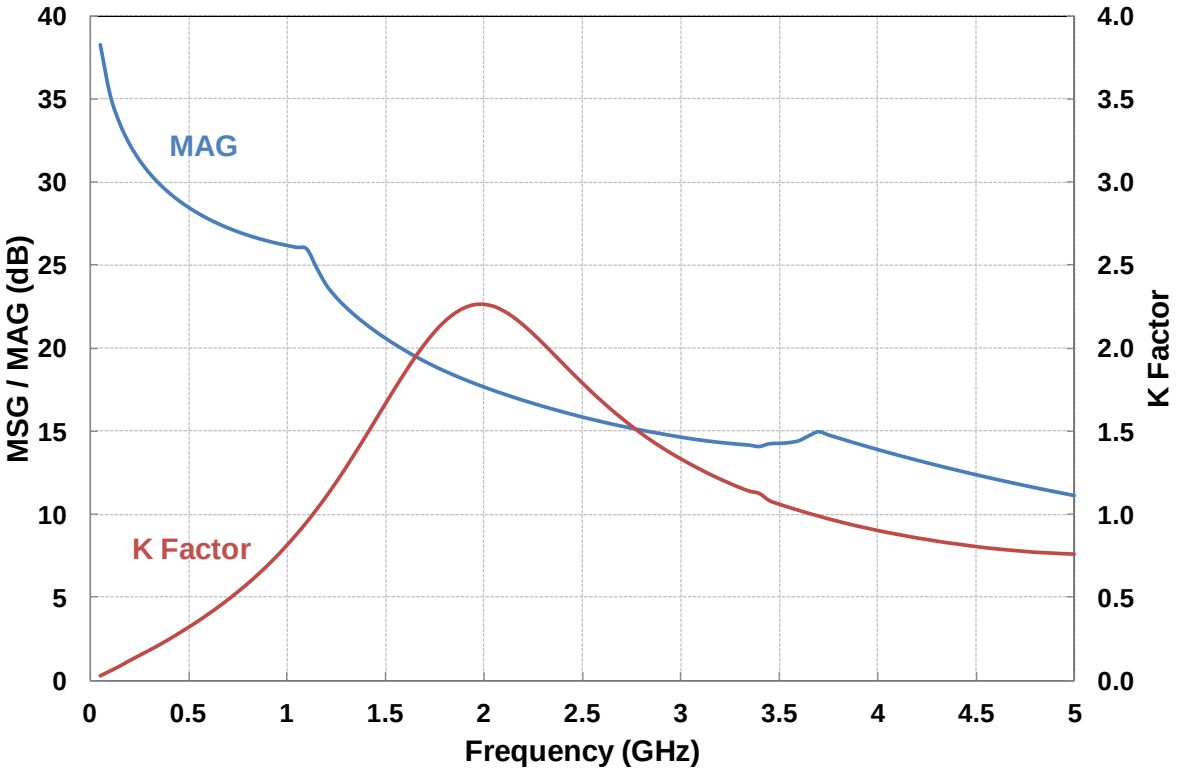
Simulated Maximum Gain & Stability Characteristics

Tcase= +25°C, V_{DS} = 50V, I_{D_Q} = 640mA



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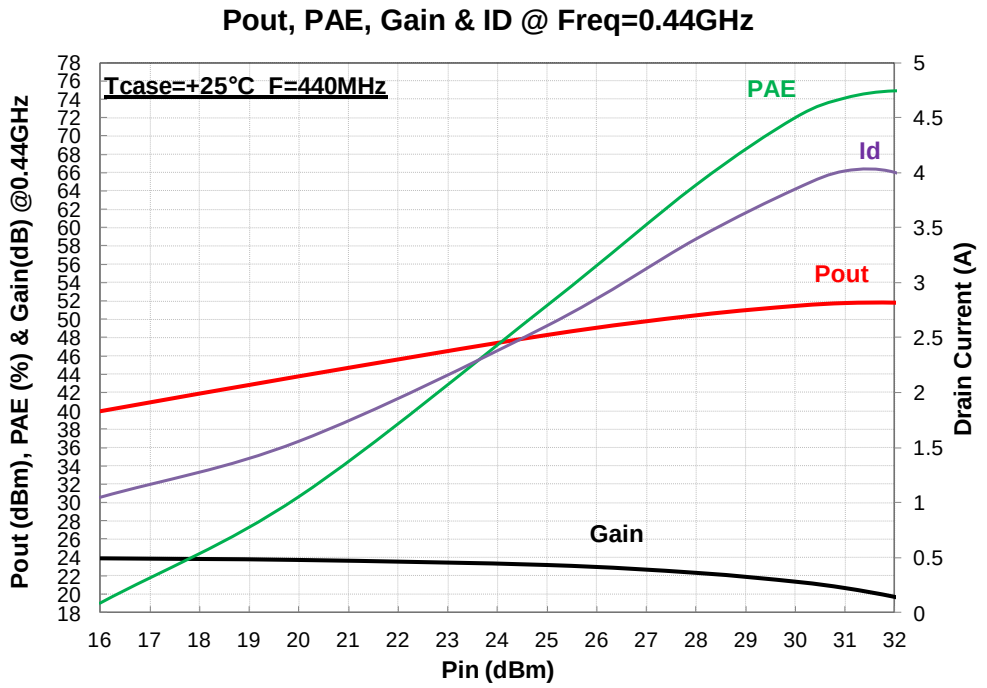
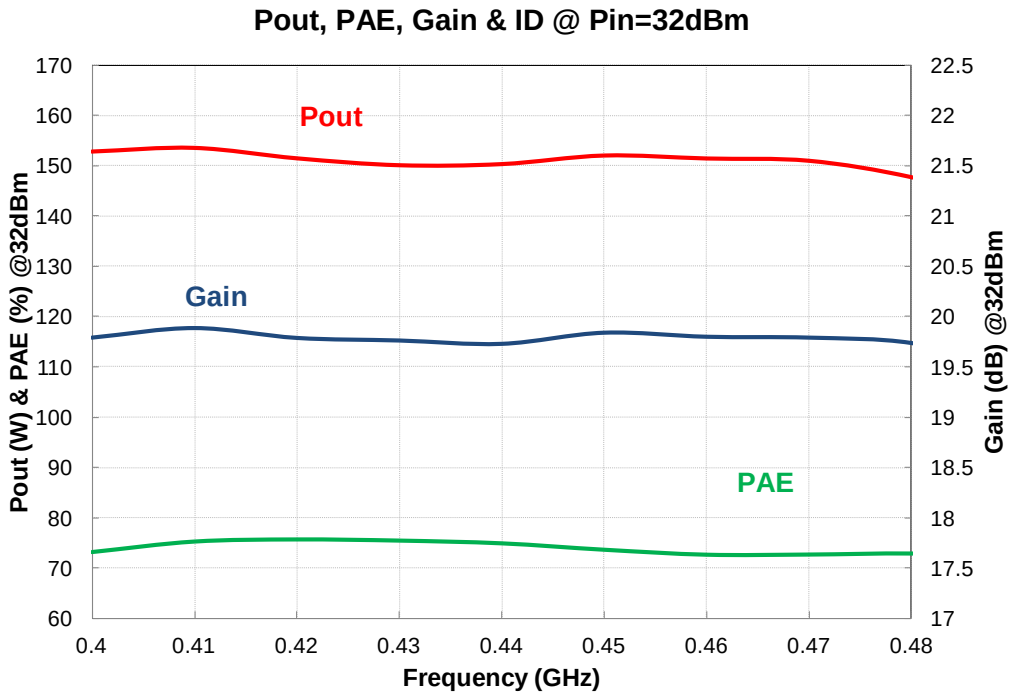
Typical Performance on Evaluation Board (ref 61504318)

Calibration and measurements are done on the connector access planes of the evaluation boards.
Tcase = +25°C, Pulsed Mode [1], V_{DS} = 50V, I_{D_Q} = 640mA





[1] Input RF and gate voltage are pulsed. Conditions are 25µs width. 10% duty cycle and 1µs offset between DC and RF pulse.

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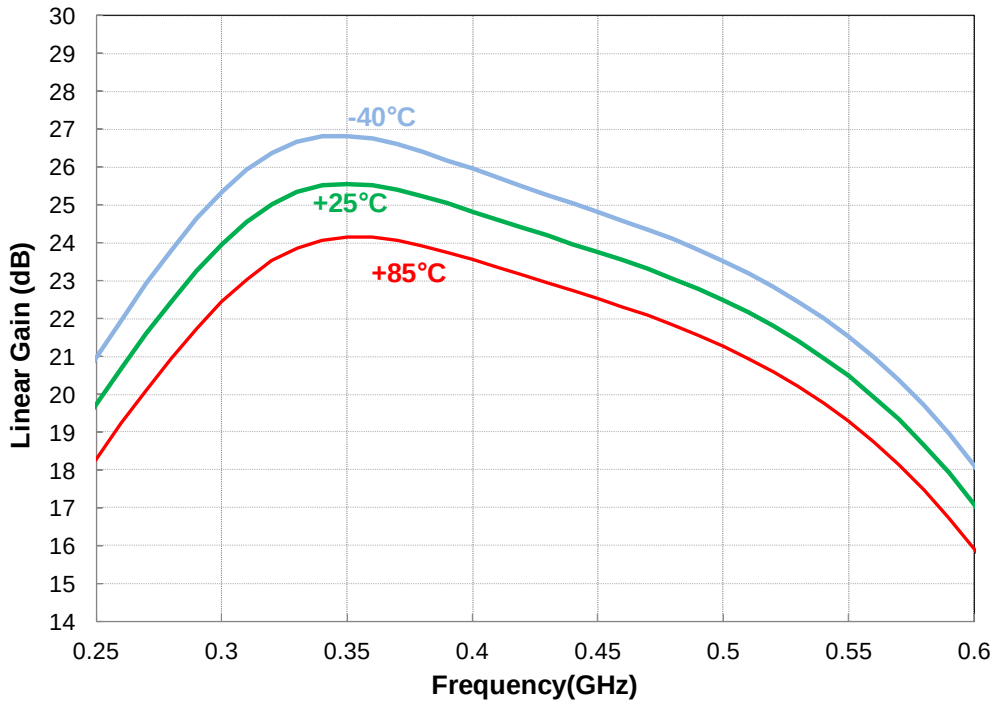
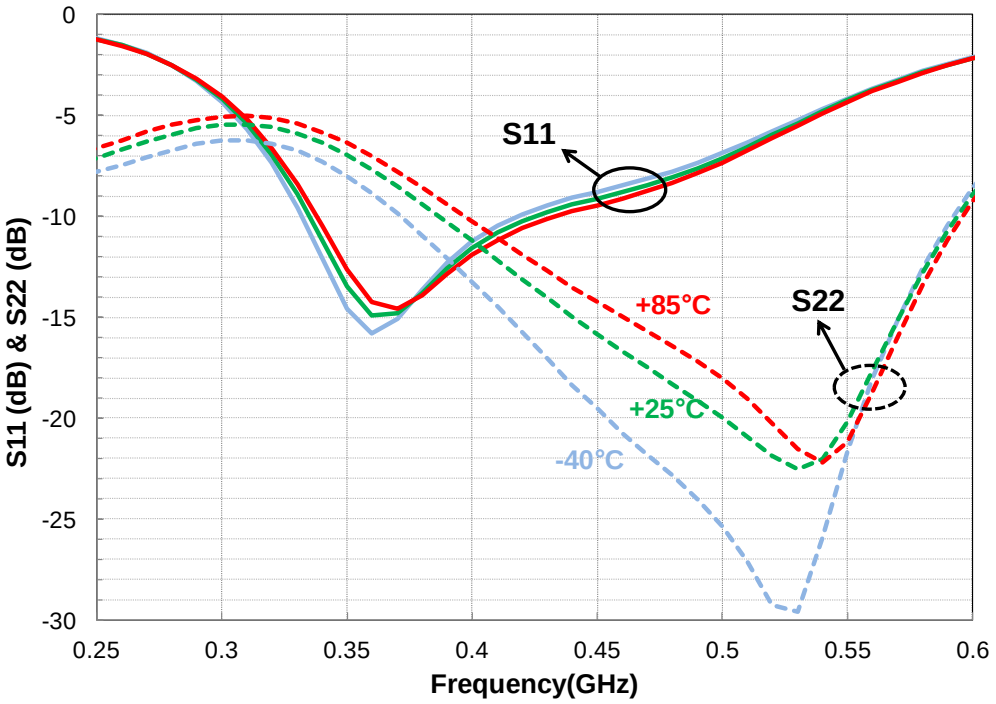
Typical Performance in Temperature (Evaluation Board)

Calibration and measurements are done on the connector access planes of the evaluation boards.
Tcase = -40°C, +25°C, +85°C, CW mode, V_{DS} = 50V, I_{D_Q} = 640mA (fixed @ +25°C)

Linear Gain versus temperature with I_{D_Q} fixed at 25°C



Input and Output Return Loss versus temperature with I_{D_Q} fixed at 25°C



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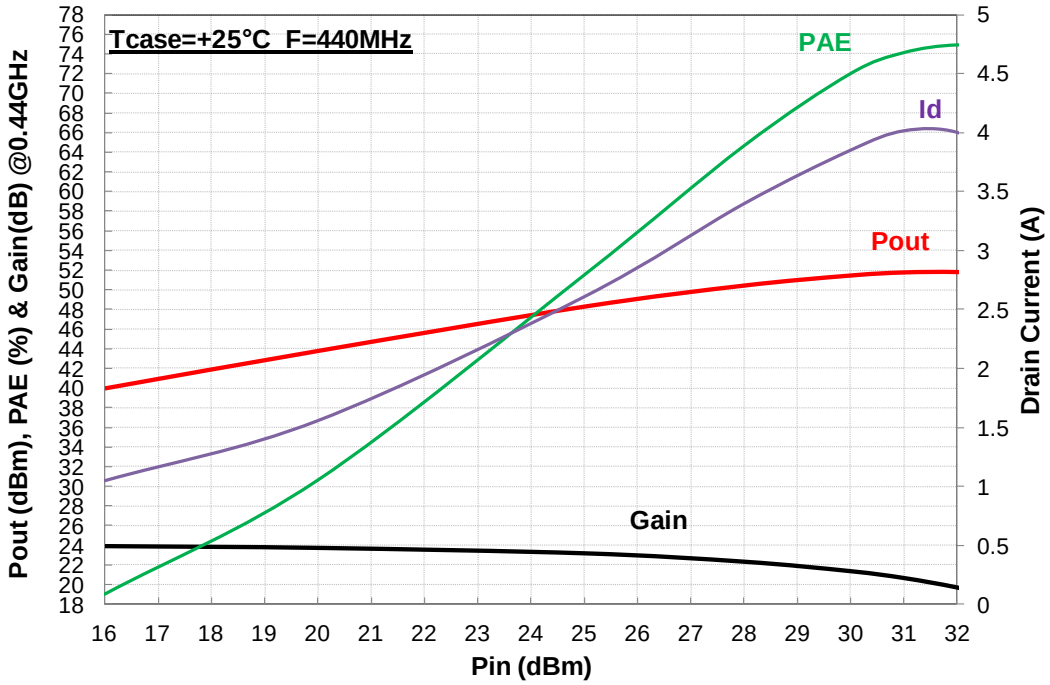
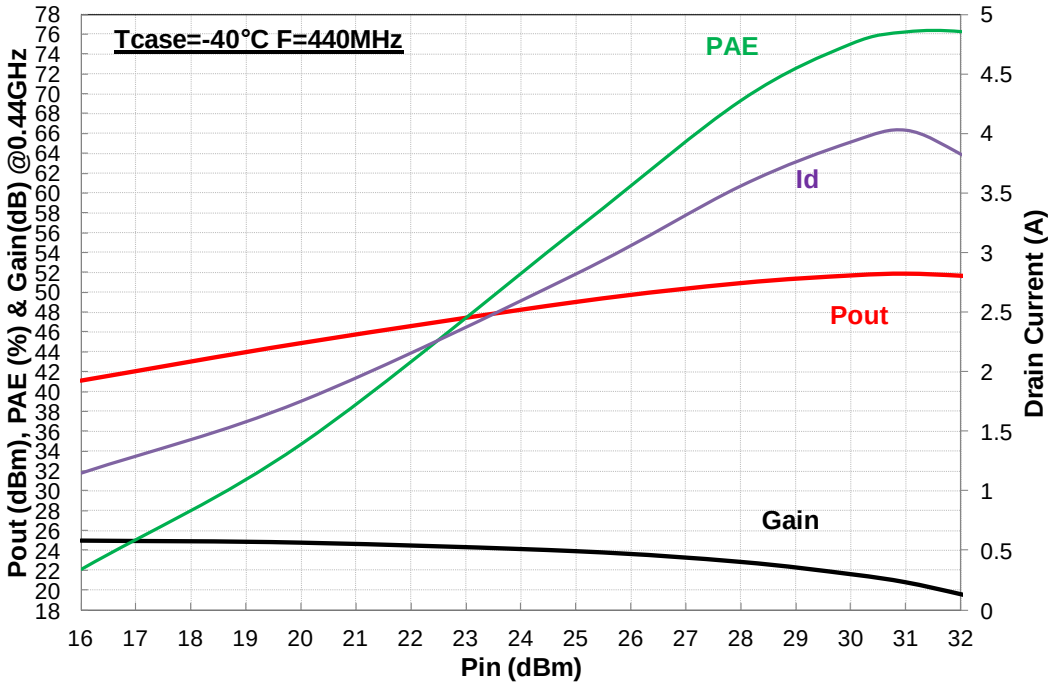
Typical Performance in Temperature (Evaluation Board)

Calibration and measurements are done on the connector access planes of the evaluation boards.
Tcase = -40°C, +25°C, +85°C;
Pulsed mode (25µs,10%), V_{DS} = 50V, I_{D_Q} = 640mA (fixed @ +25°C)

Pout, PAE, Gain & Id @ Freq = 440MHz & Tc = +25°C



Pout, PAE, Gain & Id @ Freq = 440MHz & Tc = -40°C



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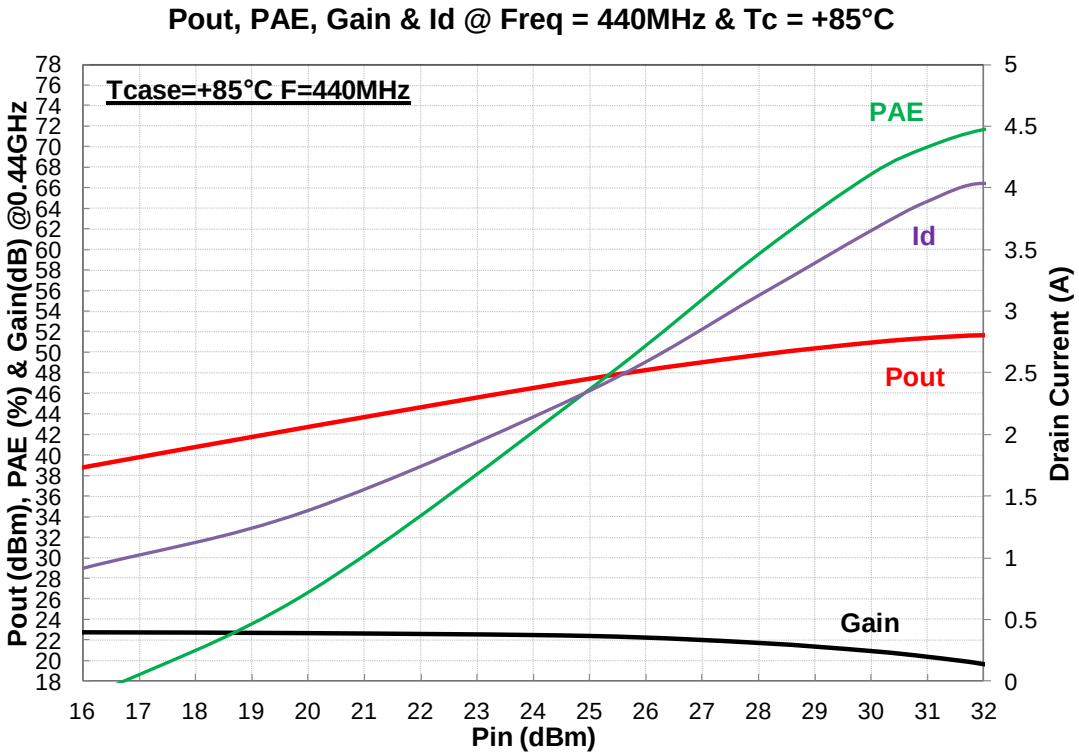
Typical Performance in Temperature (Evaluation Board)

Calibration and measurements are done on the connector access planes of the evaluation boards.
Tcase = -40°C, +25°C, +85°C;
Pulsed mode (25µs,10%), V_{DS} = 50V, I_{D_Q} = 640mA (fixed @ +25°C)



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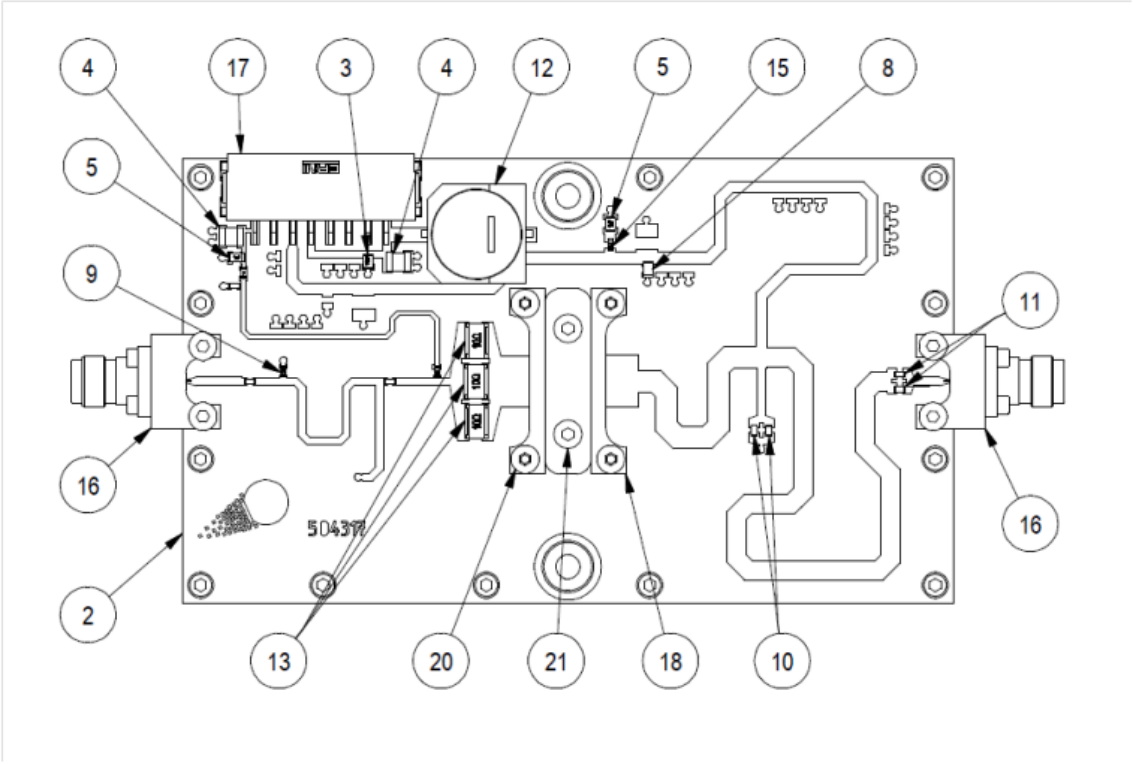
Demonstration Amplifier Circuit Outline (Ref. 61504318a)



Demonstration Amplifier / Bill of Materials (Ref. 61504318a)

Designator	Description	Qty
1	Base / Heat-sink	1
2	PCB RF35P, Er=3.5, h=508µm	1
3	Capacitor 10nF +/- 10% 0805 100V	1
4*	Capacitor 1µF +/- 10% 1210 100V	2
5	Capacitor 1nF +/- 5% 0805 100V	2
6	Capacitor 100pF +/- 5% 0603 250V	1
7	Capacitor 27pF +/- 5% 0603 250V	2
8	Capacitor 240pF +/- 5% 0805 250V	1
9	Capacitor 8.2pF +/- 5% 0603 250V	1
10	Capacitor 6.8pF +/- 5% 0603 250V	2
11	Capacitor 18pF +/- 5% 0603 250V	2
12	Capacitor 150µF +/- 20% H13 80V	1
13	Resistor 10Ω +/- 1% 1218 1W	3
14	Resistor 10Ω +/- 1% 0603 0.1W	2
15	Resistor 5.1Ω +/- 1% 0603 0.1W	1
16	RF SMA Connector	2
17	DC ERNI Connector 8cts	1
18	Pressor elements	2

* Have to be removed on Gate accesses in case of Gate pulsed measurement

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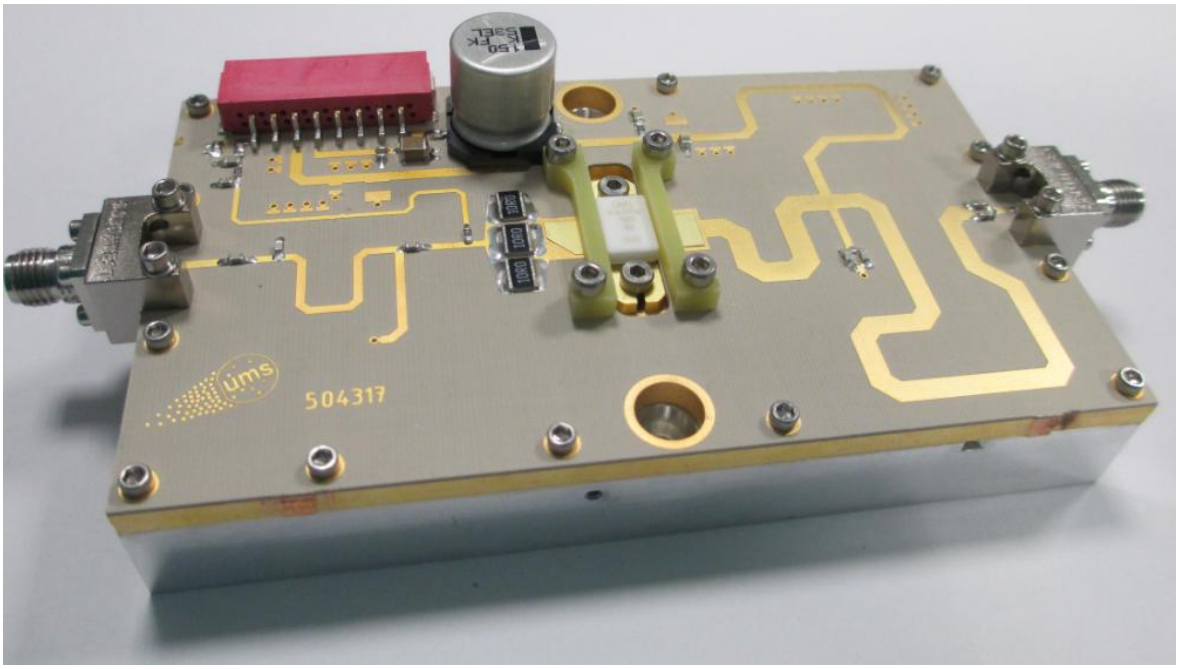

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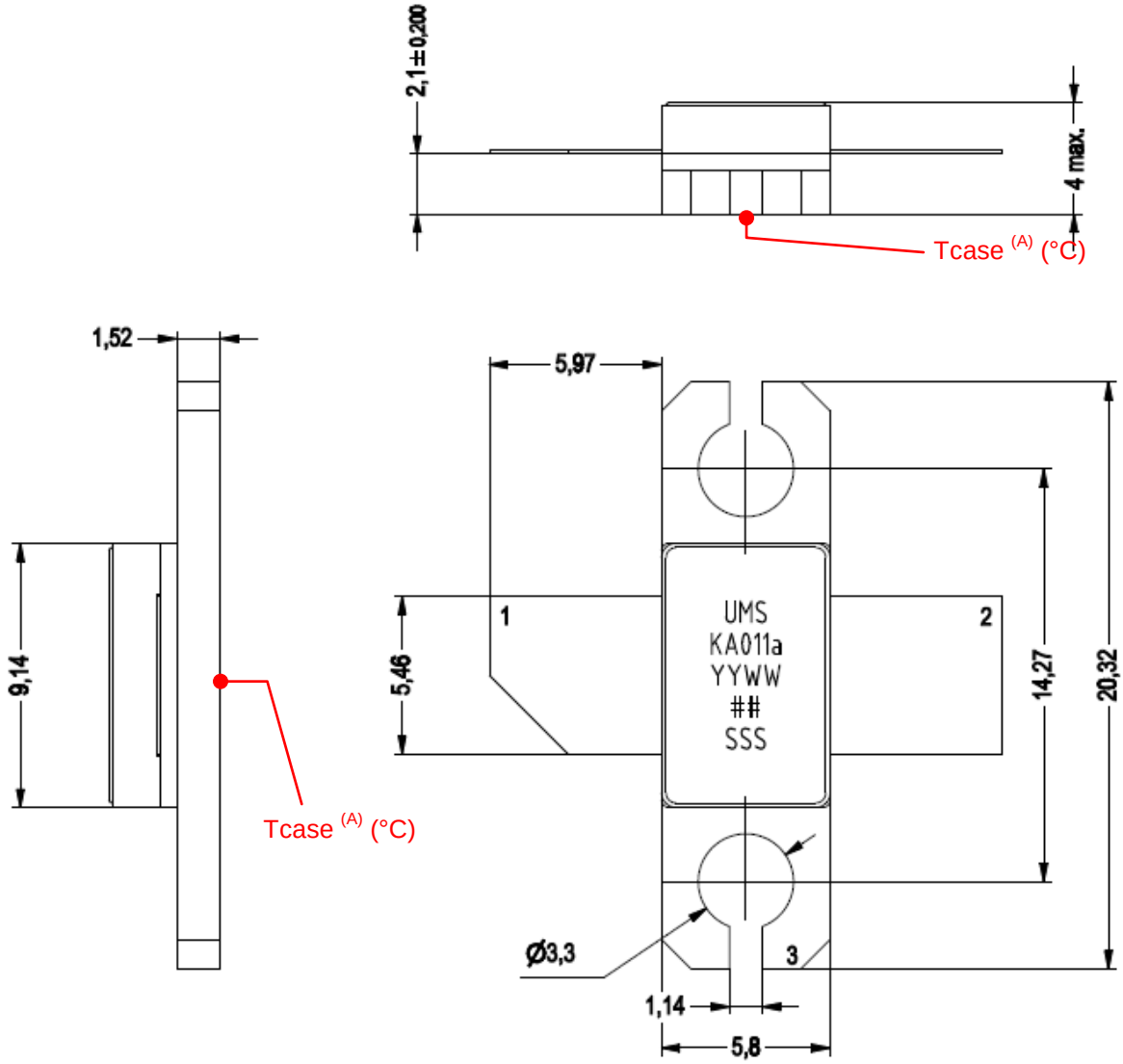
Package outline



PINOUT: 1- GRILLE
2- DRAIN
3- SOURCE (GND)

(A) Tcase locates the reference point used to monitor the device temperature. This point has been taken at the device / system interface to ease system thermal design.
Chamfer on leads indicates the gate access of the transistor.

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Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Qualification domain

The CHKA011aSXA is qualified according to UMS rules, excluding humid environment as it is in non hermetic package

Ordering Information

Ceramic metal package:	CHKA011aSXA/XY Stick: XY = 26

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