

45W GaN packaged power bar

GaN HEMT Microwave Transistor in flange package

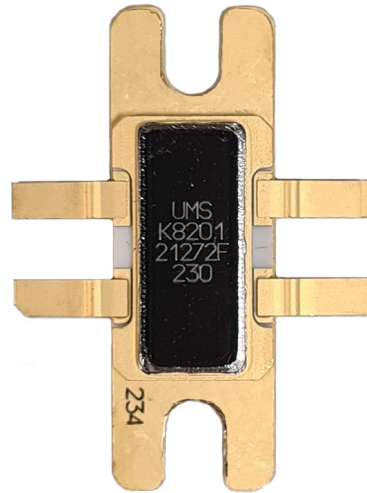
Description

The CHK8201-SYA is an unmatched power bar microwave transistor, which integrates two CHK8101a99F power bars packaged together with individual access possible, that produces 45W of combined output power.

It is designed for a wide range of RF power applications up to 4 GHz. It is well suited for multi-purpose applications such as radar and telecommunication.

The applied GaN on SiC technology is a space evaluated HEMT process with 0.50 μm gate length. It requires an external matching circuitry.

It is supplied in a hermetic ceramic-metal flange power package, compliant with the RoHs N°2011/65 and REACH N°1907/2006 directives.



Main Features

- Broadband performances: DC-4GHz
- 45W Pout for +29dBm input power
- 22dB of linear gain at 0dBm input power
- DC bias: $V_{DS}=50V@I_{D,Q}=200mA$

Main Electrical Characteristics

Tamb.= +25°C, $V_{DS}=+50V$, freq. = 1.3 GHz, $I_{D,Q} = 200 \text{ mA}$, Pulsed Mode (25 μs -10%)

Symbol	Parameter	Min	Typ	Max	Unit
G_{SS}	Small signal gain		22		dB
P_{SAT}	Saturated output power		45		W
PAE	Power Added Efficiency		55		%
G_{PAE_MAX}	Associated Gain at Max PAE		17		dB

These values are representative of board measurements made in the connector's access planes.

Specifications

Tamb. = +25°C, V_{DS} = +50V, I_{D_Q} = 200mA, Pulsed Mode (25µs-10%), freq. = 1.3GHz

Symbol	Parameter	Min	Typ	Max	Unit
G _{SS}	Small signal gain		22		dB
P _{SAT}	Saturated output power		45		W
PAE	Power Added Efficiency		55		%
G _{PAE_MAX}	Associated Gain at Max PAE		17		dB
I _D	Drain current in saturation			1.8	A

These values are representative of board measurements made in the board connector's access planes.

Recommended Operating Ratings (ROR)

Tamb. = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range			4	GHz
V _{DS}	Drain source voltage		50	50	V
V _{GS}	Gate source voltage ⁽²⁾		-1.9		V
I _{D_Q}	Quiescent drain current		200	640	mA
I _{G_MAX}	Gate Current (forward mode) ⁽³⁾		0	32	mA
T _{OP_CASE}	Case operating temperature range ⁽¹⁾	-40		85	°C
T _{J_MAX}	Junction temperature			200	°C

⁽¹⁾ Max junction temperature must be considered

⁽²⁾ Typical value for I_{D_Q} = 200 mA

⁽³⁾ Currents are provided at saturation (with RF signal)

Absolute Maximum Ratings ⁽¹⁾ (AMR)

Tamb. = +25°C

Symbol	Parameter	Values	Unit
V _{DS}	Drain source biasing voltage	60	V
V _{GS}	Gate source biasing voltage ⁽²⁾	-10 to +2	V
I _{G_MAX}	Maximum Gate Current (forward mode) ⁽⁴⁾	+64	mA
I _{G_MIN}	Maximum Gate Current (reverse mode) ⁽⁴⁾	-4	mA
I _{D_MAX}	Maximum drain current	See note (3)	mA
T _J	Junction temperature	230	°C
T _a	Operating temperature range	See note (3)	°C
T _{stg}	Storage temperature range	-55 to +150	°C

⁽¹⁾ Operation of this device above anyone of these parameters may cause permanent damage

⁽²⁾ Linked to and limited by I_{G_MAX} and I_{G_MIN} values. Maximum input power depends on frequency and should not exceed 2dB above PAE_{MAX}

⁽³⁾ Max junction temperature must be considered

⁽⁴⁾ Currents are provided at saturation (with RF signal)

Bias-up procedure

1. Bias power bar gate voltage at V_{GS} close to V_p (Typically: $V_{GS} \approx -5V$)
2. Apply V_{DS} bias voltage (Typically: $V_{DS} = 50V$)
3. Increase V_{GS} up to quiescent bias drain current I_{D_Q}

Bias-down procedure

1. Turn off RF signal
2. Bias power bar gate voltage at V_{GS} close to V_p (Typically: $V_{GS} \approx -5V$)
3. Turn V_{DS} bias voltage down to 0V
4. Turn V_{GS} bias voltage down to 0V

Device thermal information

All the figures given in this section are obtained assuming that the package is cooled down by conduction through the package baseplate (no convection mode considered).

The thermal performances of the device are based on UMS rules to evaluate the junction temperature (T_j). This temperature is defined as the peak temperature in the channel area.

This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the power bar is fabricated (GaN Power HEMT 0.5 μ m).

The temperature T_c is monitored, and defined, at the package backside interface.

The thermal resistance (R_{th}) is given for the full power bar, in “equivalent” CW operating mode.

The system maximum temperature must be adjusted in order to guarantee that $T_{junction}$ remains below the maximum value specified in the Absolute Maximum Ratings table.

So, the system PCB must be designed to comply with this requirement.

Thermal analysis is recommended. More information is available on request.

Parameters	Symbol	Conditions	Value	Unit
Typical Thermal Resistance	R_{th}	Bare die on carrier characteristic	3	$^{\circ}C/W$
Junction Temperature ⁽¹⁾	T_j	$T_c = 95^{\circ}C$, $P_{diss}^* = 35W$, CW	200	$^{\circ}C$

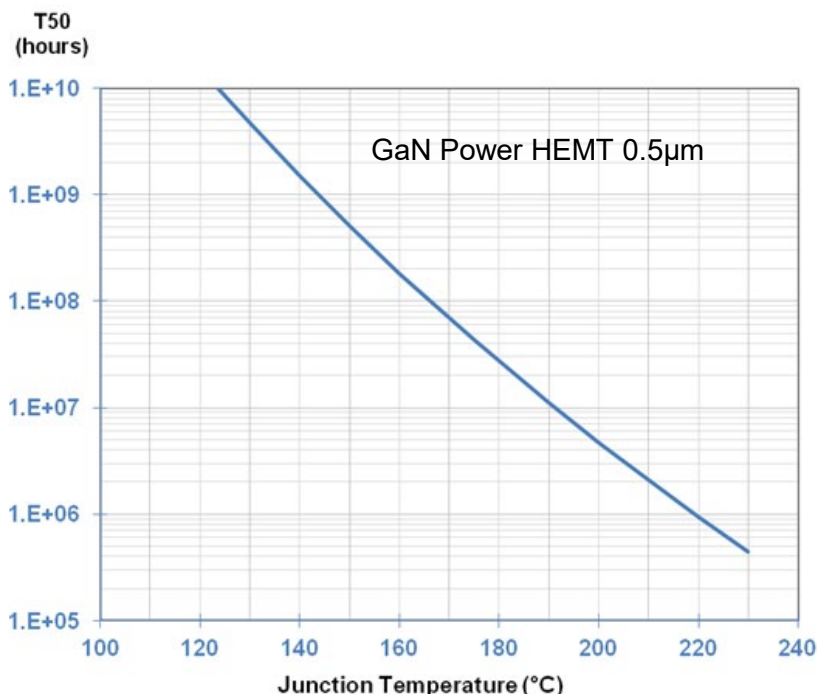
The reference temperature (T_c) is defined at the package backside.

The package carrier plate is made up of 1.5mm Cu/Mo/Cu.

* $P_{diss}=35W$; $P_{out}=46.75dBm$; $I_d=1.63A$

(1) Assuming that the same power is dissipated in each power bar : P_{diss} is the total dissipated power

Median Life Time versus Junction Temperature

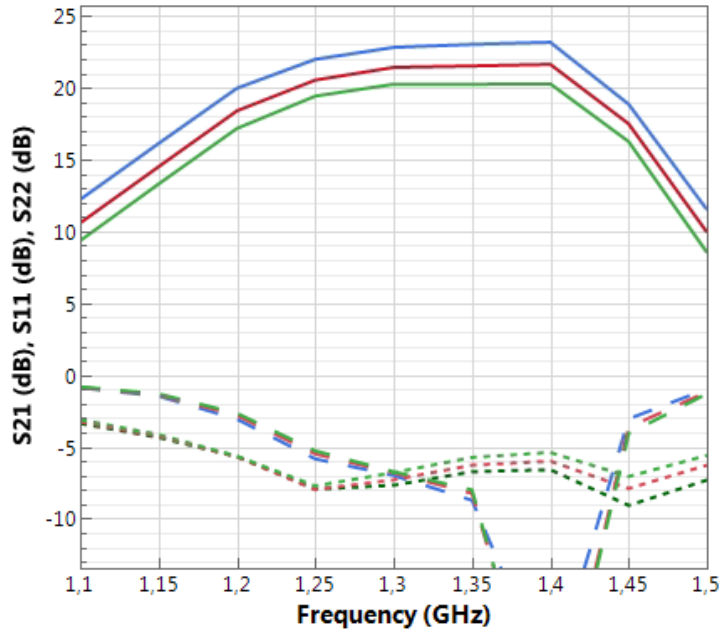


Typical Board Measurements

Vd = +50V, I_{D_Q} = 200mA

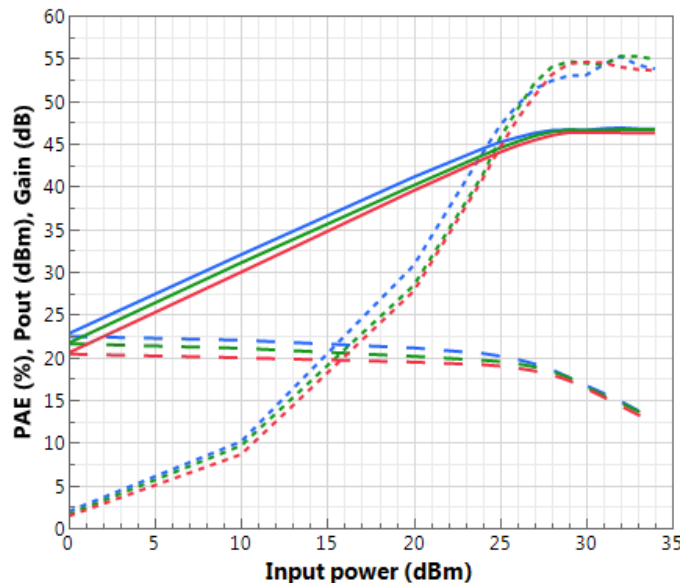
Gain (dB, - S₂₁), input (dB, -- S₁₁) & output (dB, - - S₂₂) return losses against frequency

(I_{D_Q} = 200 mA at Tc=25°C)



Tcase ≈ -40°, +25; +85°C

PAE (%), Pout (dBm), and Gain (dB, --) against input power (f = 1.3GHz, I_{D_Q} = 200mA at Tc=25°C)

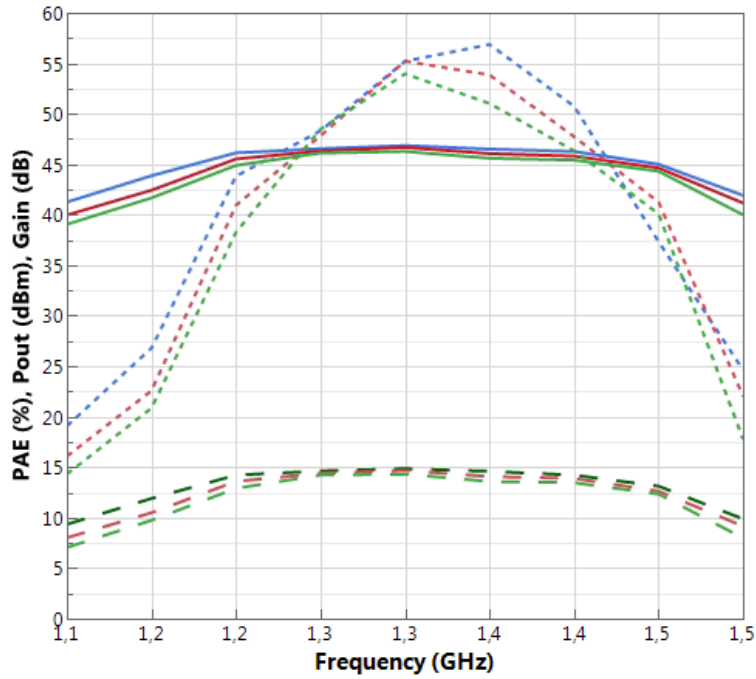


Tcase ≈ -40°, +25; +85°C

Typical Board Measurements

Vd = +50V, I_{D_Q} = 200mA

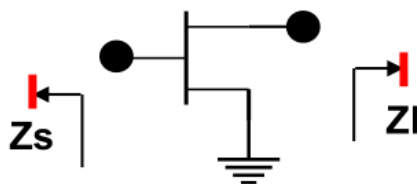
PAE (%), Pout (dBm, -), and Gain (dB, --) against frequency
(Pin = 32 dBm, I_{D_Q} = 200 mA at Tc=25°C)



Tcase ≈ -40°, +25°, +85°C

Simulated Source and Load Impedances

$V_{DS} = +50V$, $I_{D_Q} = 200\text{ mA}$, $T_{case} = +25^{\circ}C$

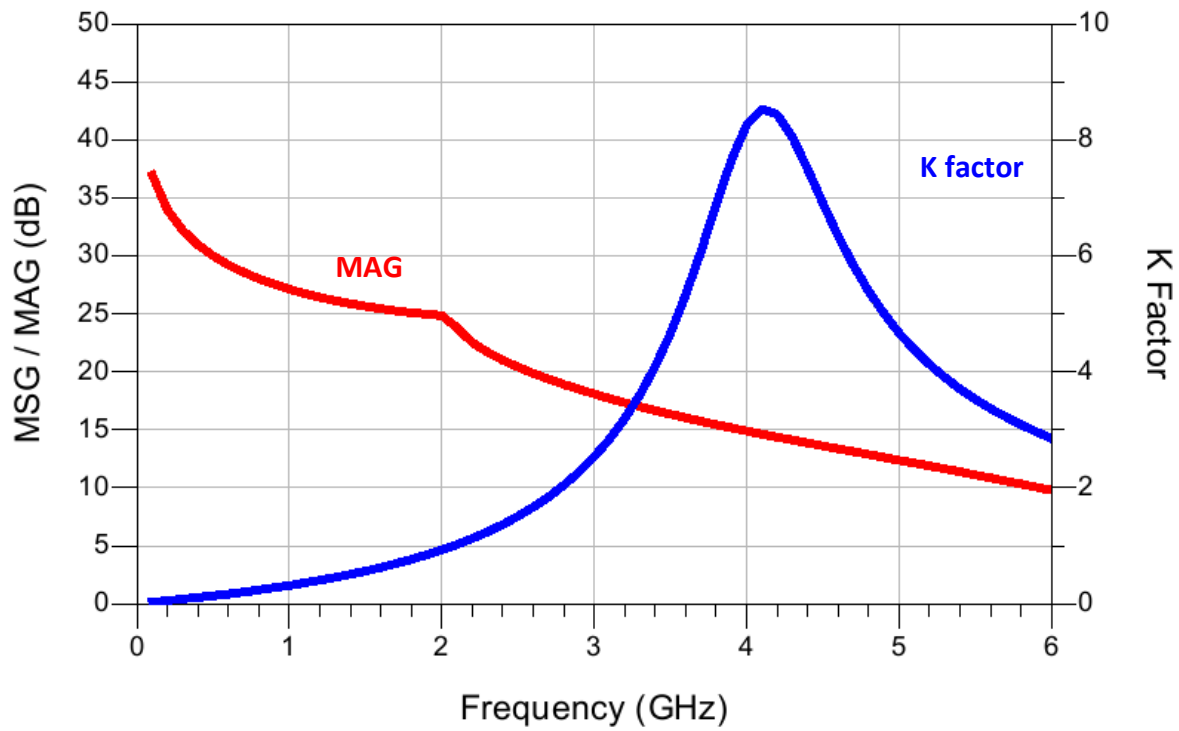


These values are given in the reference plane defined by the connection between the transistor leads and the PCB. The impedances are simulated in the package access planes, the two flanges of each package side being connected. A gap of $200\mu\text{m}$ is considered between the edge of the package and the PCB.

Frequency (MHz)	Zs (Ω)	ZI (Ω)	Pout (dBm)	PAE (%)
1000	$2-j$	$6.4+j*15$	46	72
2500	$1.3-j*6.8$	$2.6+j*2.6$	46	62.6
4000	$5-j*16$	$1.5-j*3.2$	45.9	38

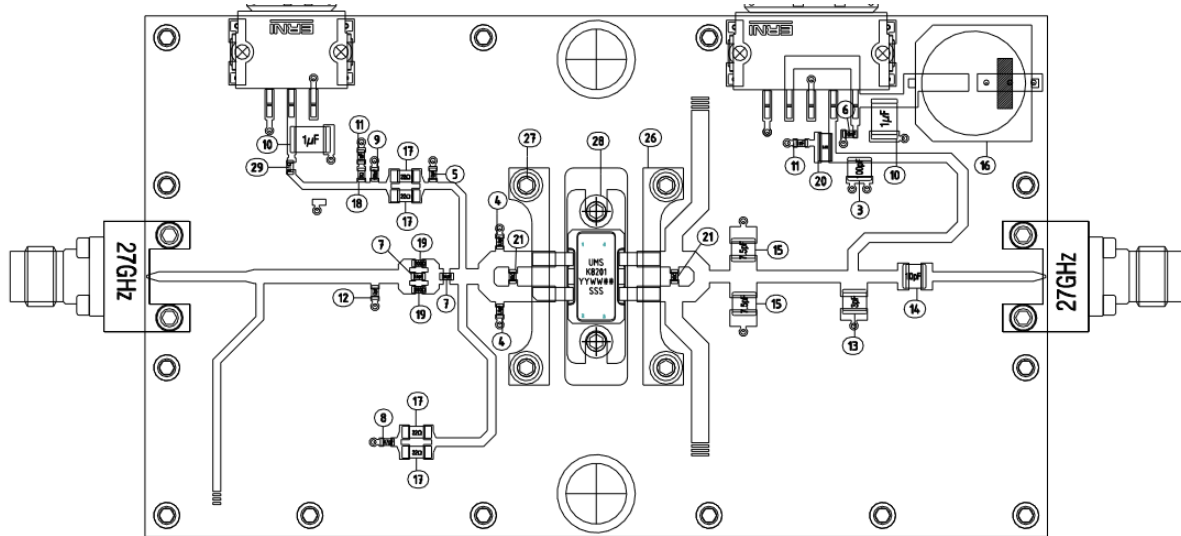
Simulated Maximum Gain & Stability Characteristics

$V_{DS} = +50V$, $I_{D,Q} = 200mA$, $T_{case} = +25^{\circ}C$



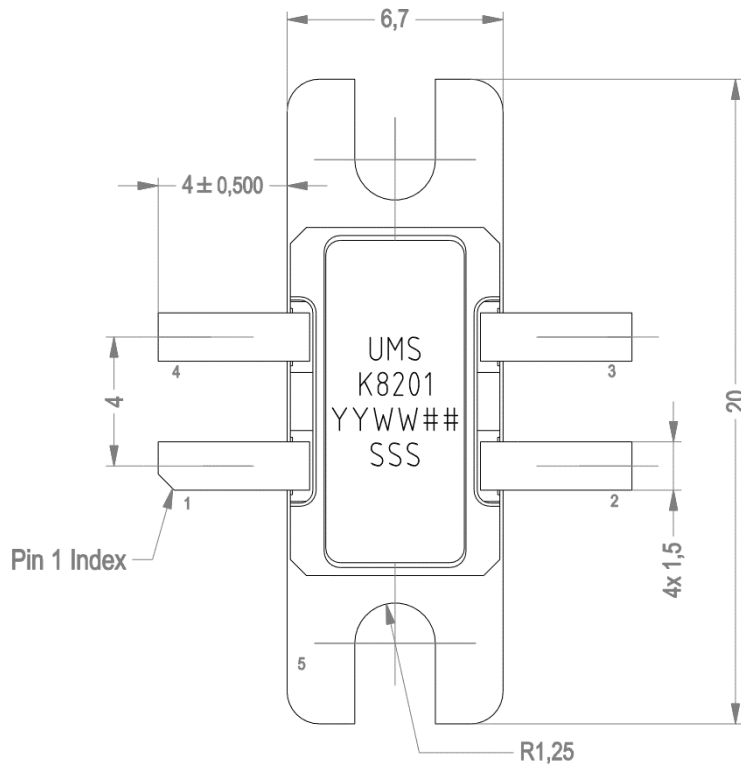
Demonstration board

The measurements of the component are performed on an evaluation board whose description can be found below. It is optimized for operation around 1.3 GHz.

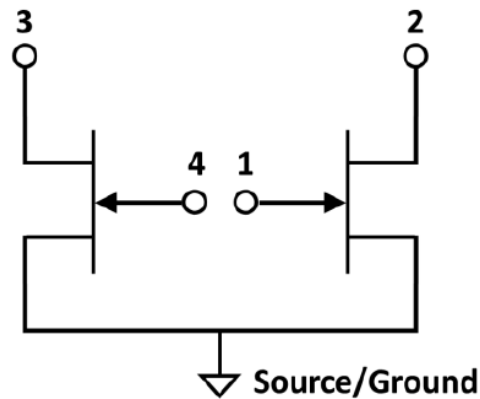


Drawing reference	Quantity	SAP reference	Designation
1	1	61503717	Heatsink Alu 104X60X7
2	1	61505027	PCB for CHK8201-SYA design
3	1	47003098	Capacitor ATC100B 100pF 1111 500V 175°C
4	2	47002069	Capacitor 0603 3.9pF± 0.25pF 250V
5	1	47002075	Capacitor 0603 10pF± 5% 250V
6	1	47002501	Capacitor 0603 X7R 10nF ±10% 100V
7	2	47002077	Capacitor 0603 15pF± 5% 250V
8	1	47002086	Capacitor 0603 47pF± 5% 250V
9	1	47002090	Capacitor 0603 100pF± 5% 250V
10	2	47002101	Capacitor 1812 1µF±10% 100V
11	2	47002500	Capacitor 0603 COG 1nF ±5% 100V
12	1	47002076	Capacitor 0603 12pF± 5% 250V
13	1	47003102	Capacitor 1111 3pF± 10% 500V
14	1	47003096	Capacitor ATC100B 10pF 1111 500V 175°C
15	2	47003094	Capacitor ATC100B 7.5pF 1111 500V 175°C
16	1	47002274	Capacitor H13 68µF±20% 100V
17	4	47002246	Resistor MMA0204 22ohms ±1% 250mW
18	1	47002115	Resistor 0603 3 Ohms±1% 0.1W
19	2	47002349	Resistor 0603 200ohms ±1% 0.1W
20	1	47003035	Resistor 0612 3.3Ω ±1% 1W
21	2	47002119	Resistor 0603 10 Ohms±1% 0.1W
22	1	47000882	DC ERNI connector 3 cts
23	1	47000884	DC ERNI connector 5 cts
24	2	47000875	RF SMA connector
25	13	47000895	Screw CHc M1.6X6 A2
26	2	61498873	Mechanical holder
27	4	47002329	Screw CHc M2x10 A2
28	2	47000926	Screw CHc M2x6 A2
29	1	47002117	Resistor 0603 5.1ohm ±1% 100mW

Package outline



Ni/Au finish on leads		1- Gate
Units :	mm	2- Drain
		3- Drain
Ni/Au finish on leads		4- Gate
Ni/Au finish on Cu/Mo/Cu package		5- Gnd



Component schematic



Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <https://www.ums-rf.com>.

Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

Metal-ceramic package

CHK8201-SYA/XY

Tray: XY = 26

Information furnished is believed to be accurate and reliable. However **United Monolithic Semiconductors S.A.S.** assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of **United Monolithic Semiconductors S.A.S.**. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. **United Monolithic Semiconductors S.A.S.** products are not authorised for use as critical components in life support devices or systems without express written approval from **United Monolithic Semiconductors S.A.S.**