United Monolithic Semiconductors

CHKA012a99F

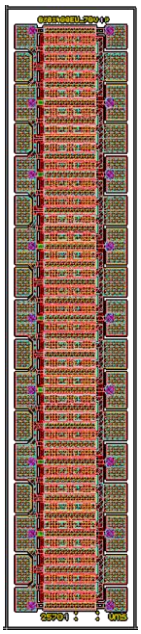
140W Power Bar

GaN HEMT on SiC

Description

The CHKA012a99F is a 140W Gallium Nitride High Electron Mobility Transistor.

This product offers a general purpose and broadband solution for a variety of RF power applications such as radar and telecommunication.
It is developed on a 0.5µm gate length GaN HEMT technology on SiC substrate and is compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006
It is proposed in a bare die form and requires an external matching circuitry.



Main Features

- Wide band capability up to 4GHz
- Pulsed and CW operating modes
- GaN technology: High Pout & High PAE
- DC bias: V_{DS} up to 50V
- Chip size: 1x4.84x0.1mm
- RoHS N°2011/65
- REACh N°1907/2006

Main Electrical Characteristics

T_{ref} = +25°C, CW mode, Freq = 3GHz, V_{DS} = 50V, I_{D_Q} = 640mA

Symbol	Parameter	Min	Typ	Max	Unit
G_{SS}	Small Signal Gain		19		dB
P_{SAT}	Saturated Output Power		140		W
P_{AE}	Max Power Added Efficiency		76		%
G_{PAE_MAX}	Associated Gain at Max PAE		14		dB

These values are deduced from elementary power cell performances

United Monolithic Semiconductors S.A.S.
Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

Recommended Operating Ratings (ROR)

T_{ref} = +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{DS}	Drain to Source Voltage			50	V	
V_{GS}	Gate to Source Voltage		-1.9		V	V_{DS}=50V, I_{D_Q}=640mA
I_{D_Q}	Quiescent Drain Current		0.64	2.05	A	V_{DS}=50V
I_{D_MAX}	Drain Current		4.1	(1)	A	V_{DS}=50V, compressed mode
I_{G_MAX}	Gate Current in forward mode		0	100	mA	DC or Compressed mode
T_{j_MAX}	Junction temperature			200	°C	(1)

(1) Power dissipation and T_{ref} (back side temperature) must be considered

DC Characteristics

T_{ref} = +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_P	Pinch-Off Voltage	-2.7	-2	-1.5	V	V_{DS}=10V, I_{DS}= I_{DSS} /100
I_{D_SAT}	Saturated Drain Current		15.4		A	(1), V_{DS}=10V, V_{GS}=1V
I_{G_leak}	Gate Leakage Current	-2.6			mA	V_{DS}=50V, V_{GS}=-7V
V_{BDS}	Drain-Source Breakdown Voltage		180		V	V_{GS}=-7V, I_{DS}=20mA

(1) For information, limited by I_{D_MAX} and T_{j_MAX}, see on ROR & AMR

RF Characteristics

T_{ref} = +25°C, CW mode, Freq = 3GHz, V_{DS} = 50V, I_{D_Q} = 640mA

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
G_{SS}	Small Signal Gain		19		dB	
P_{SAT}	Saturated Output Power		140		W	
P_{AE}	Max Power Added Efficiency		76		%	
G_{PAE_MAX}	Associated Gain at Max PAE		14		dB	

These values are deduced from elementary power cell performances.

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

Absolute Maximum Ratings (AMR)

Tref = +25°C [1] [2] [3]

Symbol	Parameter	Rating	Unit	Note
V_{DS_Q}	Drain-Source Biasing Voltage	60	V	
V_{GS_Q}	Gate-Source Biasing Voltage	-10, +2	V	[4], [5]
I_{G_MAX}	Maximum Gate Current in forward mode	200	mA	
I_{G_MIN}	Maximum Gate Current in reverse mode	-13	mA	
I_{D_MAX}	Maximum Drain Current	See note		[4]
P_{IN}	Maximum Input Power	See note		[5]
T_{j_MAX}	Maximum Junction Temperature	230	°C	
T_{STG}	Storage Temperature	-55 to +150	°C	
T_{ref}	Back Side Operating Temperature	See note	°C	[4]

[1] Operation of this device above anyone of these parameters may cause permanent damage.
[2] Duration < 1s.
[3] The given values must not be exceeded at the same time even momentarily for any parameter, since each parameter is independent from each other, otherwise deterioration or destruction of the device may take place.
[4] T_{ref} = back side temperature. Max junction temperature must be considered
[5] Linked to and limited by I_{G_MAX} & I_{G_MIN} values. Maximum input power depends on frequency and should not exceed 2dB above PAE_max.

Biasing procedure

1. Bias power bar gate voltage at V_{GS} close to V_p (Typically: $V_{GS} \approx -5V$)
2. Apply V_{DS} bias voltage (Typically: $V_{DS} = 50V$)
3. Increase V_{GS} up to quiescent bias drain current I_{D_Q}

The quiescent current steady state must be carefully controlled as it is influenced by the operating mode, the temperature and the overall thermal resistance.
A drain current control is recommended on the biasing network.

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

Device thermal information

The thermal performances of the device are based on UMS rules to evaluate the junction temperature (Tj). This temperature is defined as the peak temperature in the channel area.
This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHKA012a99F is fabricated (GaN Power HEMT 0.5µm).
The temperature Tb is defined as the chip back side temperature
The thermal resistance (Rth) is given for the full power bar, in “equivalent” CW operating mode and in two different configurations as given in the table. The device assembly must be adapted to the operating mode. Thermal analysis is recommended. More information is available on request.

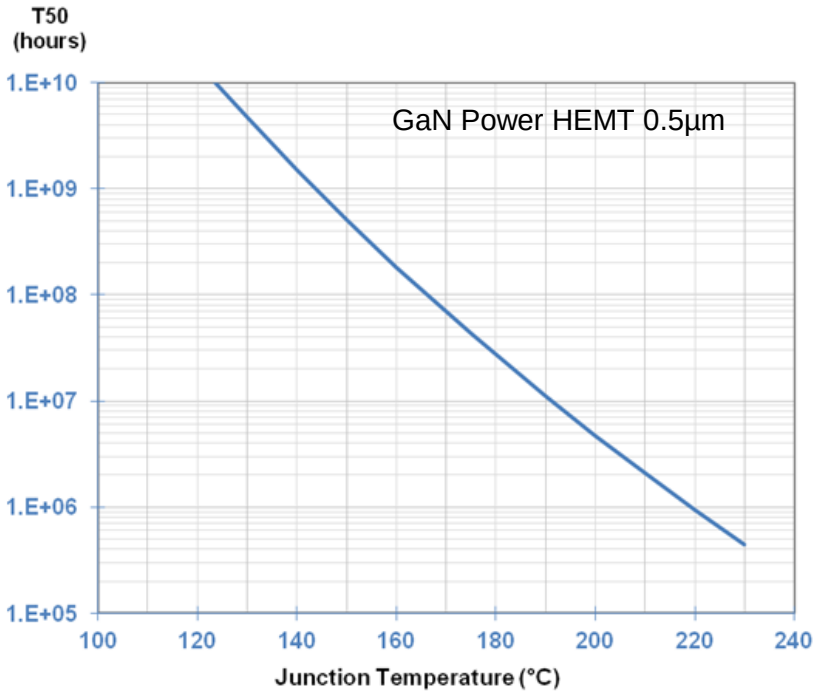
Parameters	Symbol	Conditions	Value	Unit
Typical Thermal Resistance	Rth	Bare die characteristic Tb = 100°C Pdiss = 100W CW	0.55	°C/W
Junction Temperature	Tj		155	°C

The back side temperature (Tb) is considered uniform on all the surface

Typical Thermal Resistance	Rth	Bare die on carrier characteristic Tc = 85°C Pdiss = 95W CW	1.2	°C/W
Junction Temperature	Tj		200	°C

The reference temperature (Tc) is defined on the carrier back side. The power bar is mounted on carrier plate (20µm Au/Sn soldering + 1.5mm Cu/Mo/Cu).

Median Life Time versus Junction Temperature

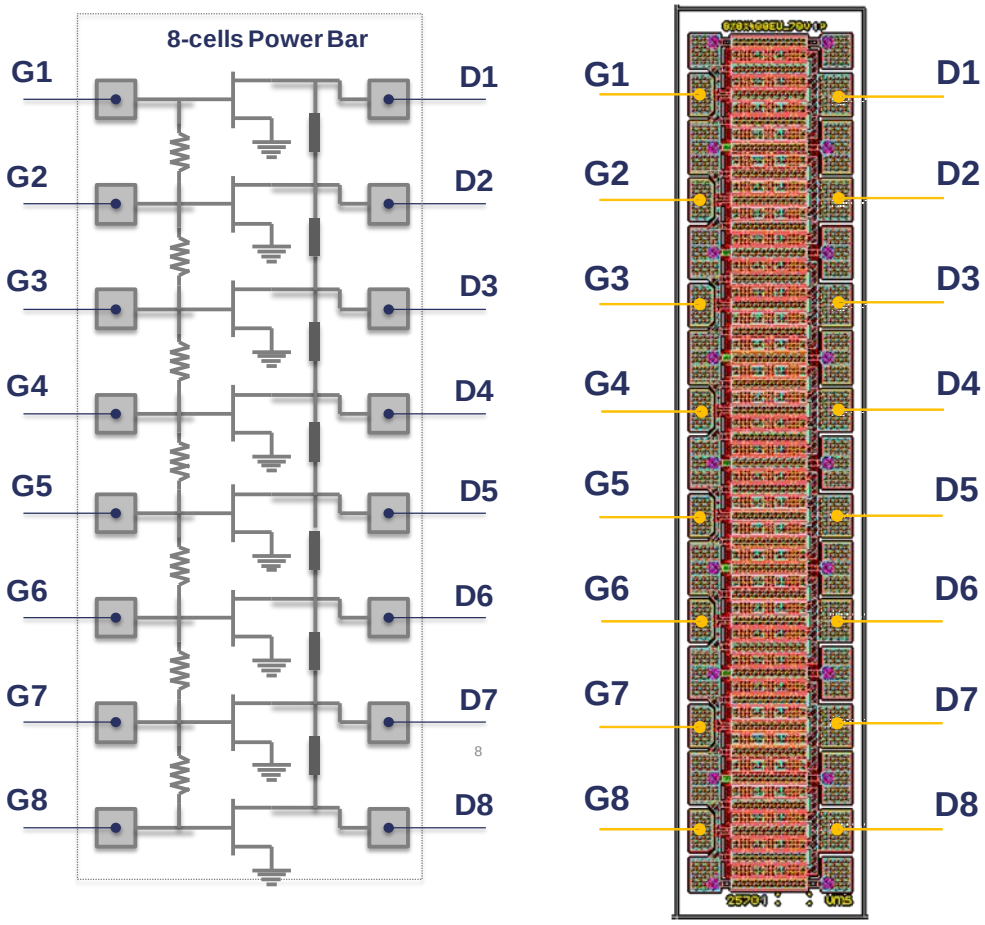


Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

Power Bar Description

The CHKA012a99F is composed of 8 elementary 17W cells. These cells are connected together with a specific network providing a good compromise between performance and stability (resistance between gates and short circuit on drains). The reference planes are at the center of the bonding pads.

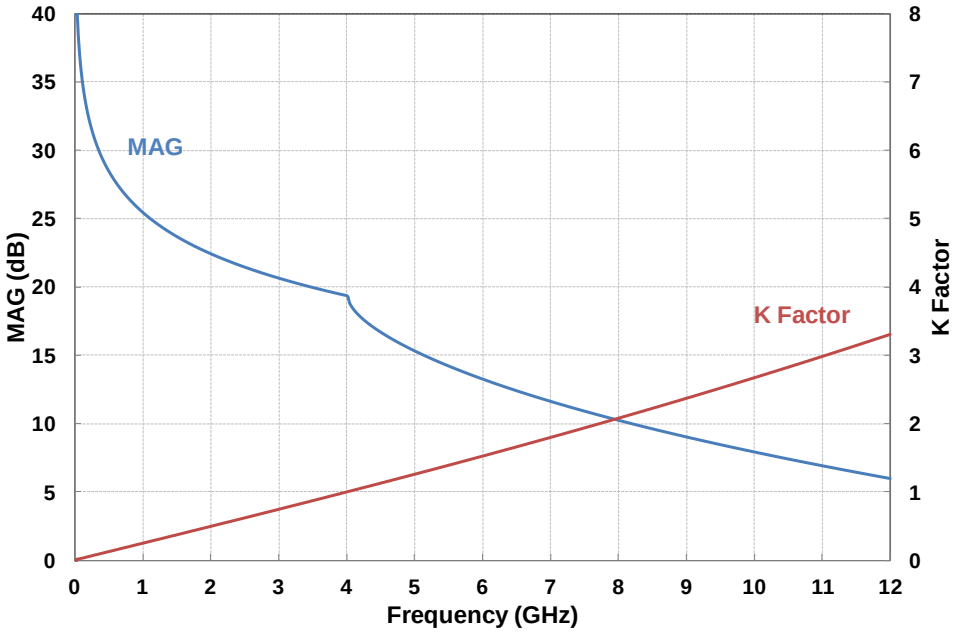
A multiport non-linear model is available on request.



Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

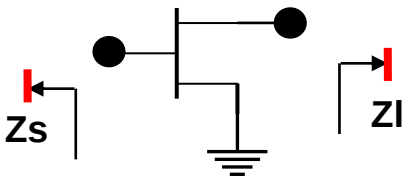
Elementary Cell Maximum Gain & Stability Characteristics

T_{ref} = +25°C, V_{DS} = +50V, I_{D_Q} = 80mA, simulated results



Elementary Cell Load Pull Performances

T_{ref} = +25°C, V_{DS} = +50V, I_{D_Q} = 80mA, simulated results



The impedances are chosen as a compromise between Output Power, PAE and Stability of the device. Second harmonic of output load and input load has been tuned.
These values are given in the bonding pads reference planes.

Frequency (GHz)	Zs	Zl	Gain (dB) @PAE_{max}	Pout (W) @PAE_{max}	PAE_{max} (%)
1	17.4 + j7.2	53.7 + j58	17	21	81
2	5.2 + j8.7	19 + j40.6	15	21	79
3	3.36 + j5.95	9.2 + j28.2	14.3	21	76
4	2.9 + j3.14	5.8 + j20.5	12.3	21	70

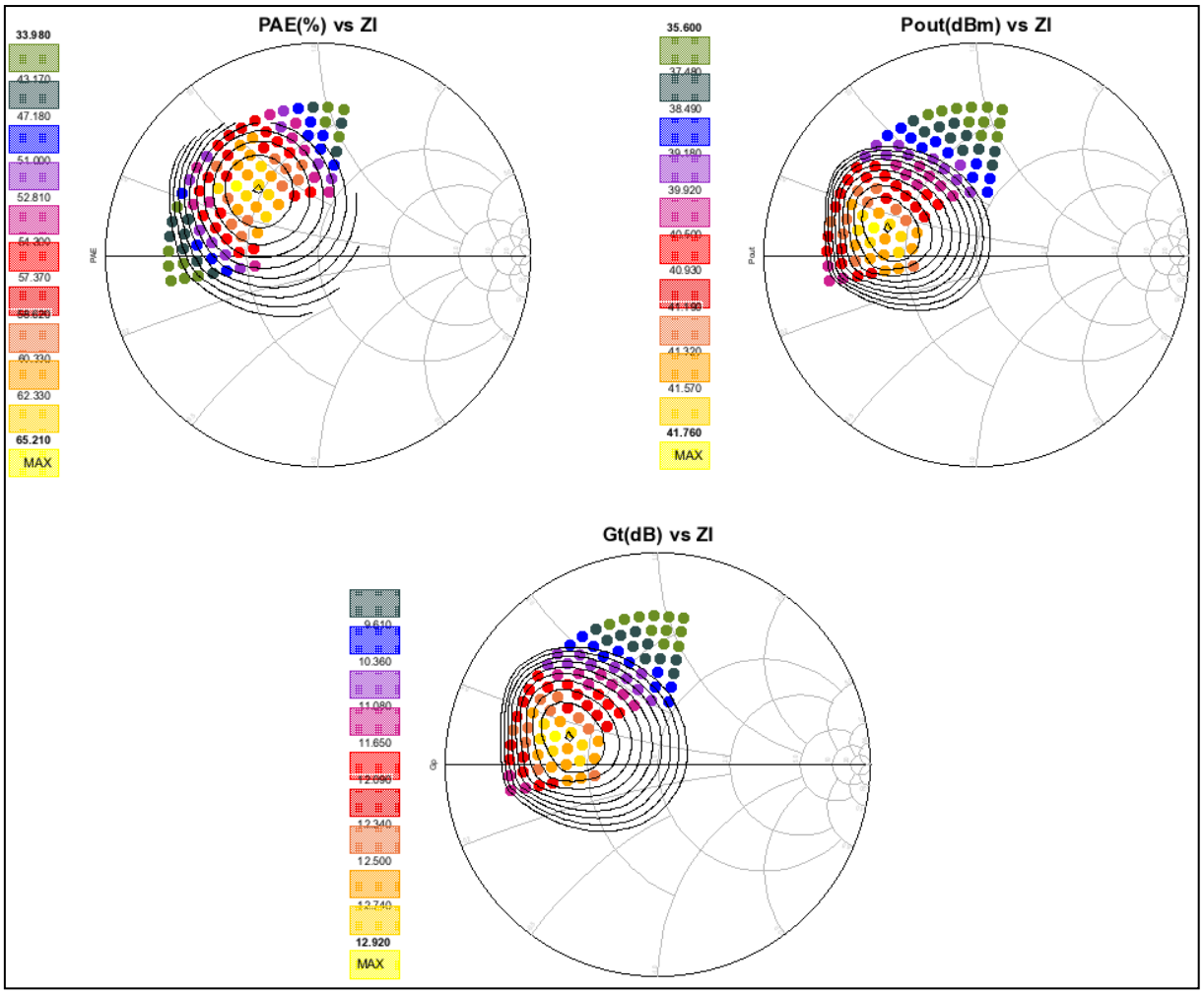
Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

Comparison Simulation versus Measurement of Elementary Cell Load Pull Performances

T_{ref} = +25°C, V_{GS} pulsed mode 10µs - 10%, RF Pulsed width: 8µs (inside V_{GS} pulsed), Freq = 3GHz, V_D = 50V, I_{D_Q} = 25mA/mm (Class AB)

- ZloadH2 = ZloadH3 = 50Ω
- Zsource matched for maximum gain
- On wafer measurement
- Measurement are given in the transistor plan at 5dB of compression
- Simulation in CW conditions

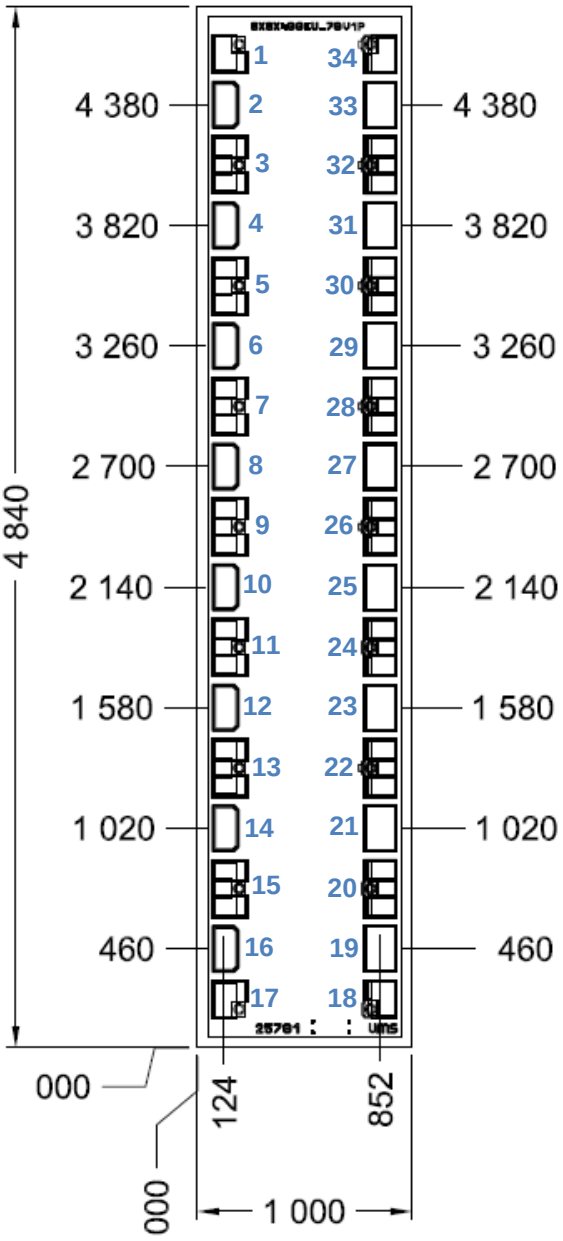
PAE(%), Output Power (dBm) and transducer gain (dB) vs the load impedance



Measurements are represented by multicolour dots and model by black contours.

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

Mechanical data



Chip thickness: 100µm +/- 10 µm

GND pads (3, 5, 7, 9, 11, 13, 15, 20, 22, 24, 26, 28, 30, 32) = 266x150µm²
GND pads (1, 17, 18, 34) = 173x150µm²
DC Gate pads (2, 4, 6, 8, 10, 12, 14, 16) = 212 x 118µm²
DC Drain pads (19, 21, 23, 25, 27, 29, 31, 33) = 212 x 118µm²

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

Notes

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

Qualification domain

This part is qualified according to UMS standards, excluding humid environment.

User guide for MMIC storage, pick & place, die attach, wire bonding

Refer to the application note AN0001 available at http://www.ums-gaas.com for general recommendations on chip handling.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS products.

User guide GaN Power Bars Assembly guide lines

Refer to the application note AN0026 available at http://www.ums-gaas.com for general recommendations on GaN-on-SiC Transistor handling and assembly.

Ordering Information

Chip form:	CHKA012a99F/00

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com