United Monolithic Semiconductors

CHK015AaQIA

15W Power Packaged Transistor

GaN HEMT on SiC in SMD leadless package

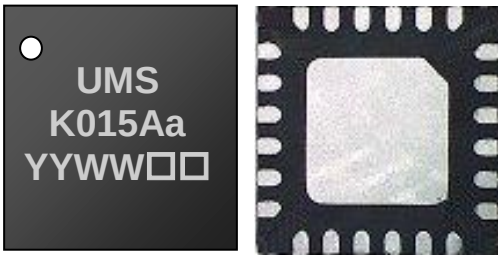
Description

The CHK015AaQIA is an unmatched packaged Gallium Nitride High Electron Mobility Transistor.

It offers general purpose and broadband solutions for a variety of RF power applications. It is well suited for multi-purpose applications such as radar and telecommunication.

The CHK015AaQIA is developed on a 0.5µm gate length GaN HEMT process. It requires an external matching circuitry.

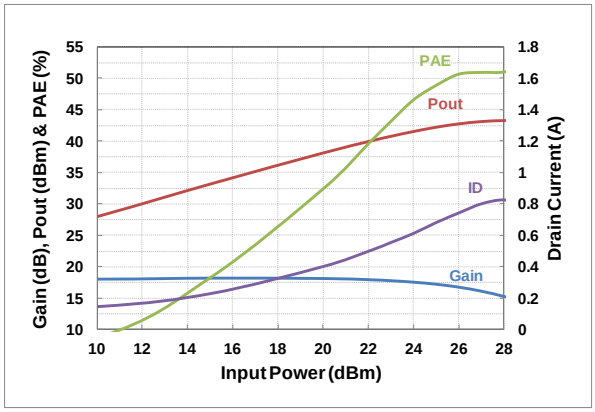
It is proposed in low cost plastic package providing low parasitic and low thermal resistance.



Main Features

- Wide band capability: up to 4GHz
- Pulsed and CW operating modes
- GaN technology: High Pout & High PAE
- DC bias: V_{DS} up to 50V
- Low cost package: 14L-DFN3x4
- MTTF > 10^6 hours @ Tj = 200°C
- RoHS N°2011/65
- REACh N°1907/2006

V_{DS} = 50V, I_{D_Q} = 75mA, Freq = 2.9GHz
Pulsed mode (1ms, 10%)



Main Electrical Characteristics[(1)]

Tamb.= +25°C, **Pulsed mode**, F = 2.9GHz, V_{DS} = 50V, I_{D_Q} = 75mA

Symbol	Parameter	Min	Typ	Max	Unit
G_{SS}	Small Signal Gain	16	18		dB
P_{SAT}	Saturated Output Power	15	20		W
PAE	Max Power Added Efficiency		55		%
I_{D_SAT}	Saturated Drain Current		800		mA

(1) : These values are the intrinsic performance of the packaged device.

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Recommended DC Operating Ratings

Tcase= +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{DS}	Drain to Source Voltage			50	V	
V_{GS_Q}	Gate to Source Voltage		-1.9		V	V_D=50V. I_{D_Q}=75mA
I_{D_Q}	Quiescent Drain Current		75	320	mA	V_D=50V
I_{D_MAX}	Drain Current		800	(1)	mA	V_D=50V. compressed mode
I_{G_MAX}	Gate Current (forward mode)		0	16	mA	DC or Compressed mode
T_{op}	Operating temperature range	-40		+85	°C	
T_{j_MAX}	Junction temperature(1)			200	°C	

(1) Power dissipation must be considered

DC Characteristics

Tcase= +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_P	Pinch-Off Voltage	-2.7	-2	-1.5	V	V_D=10V. I_D= I_{DSS} /100
I_{D_SAT}	Saturated Drain Current		2.4 (1)		A	V_D=10V. V_G=1V
I_{G_leak}	Gate Leakage Current (reverse mode)	-0.8			mA	V_D=50V. V_G=-7V
V_{BDS}	Drain-Source Break-down Voltage		180		V	V_G=-7V. I_D=20mA

(1) For information, limited by I_{D_MAX}. see on Absolute Maximum Ratings

RF Characteristics

Tcase= +25°C. Pulsed mode

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
G_{SS}	Small Signal Gain @ 2.9GHz	16	18		dB	V_D=50V. I_{D_Q}=75mA
P_{SAT}	Saturated Output Power	15	20		W	V_D=50V. I_{D_Q}=75mA
PAE	Max PAE @ 2.9GHz		55		%	V_D=50V. I_{D_Q}=75mA
G_{PAE_MAX}	Associated Gain at Max PAE @ 2.9GHz		15		dB	V_D=50V. I_{D_Q}=75mA

These values are the intrinsic performance of the packaged device. They are deduced from measurements and simulations. They are considered in the reference plane defined by the leads of the package, at the connection interface with the PCB.

The typical performance achievable in more than 10% frequency band around 3GHz was demonstrated using the reference board 61502522 presented hereafter.

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Absolute Maximum Ratings

Tcase= +25°C[1] [2] [3]

Symbol	Parameter	Rating	Unit	Note
V_{DS}	Drain-Source Biasing Voltage	60	V	
V_{GS_Q}	Gate-Source Biasing Voltage	-10. +2	V	
I_{G_MAX}	Maximum Gate Current in forward mode	32	mA	
I_{G_MIN}	Maximum Gate Current in reverse mode	-2	mA	
I_{D_MAX}	Maximum Drain Current	3	A	[4]
P_{IN}	Maximum Input Power	30	dBm	[5]
T_j	Junction Temperature	230	°C	
T_{STG}	Storage Temperature	-55 to +150	°C	
T_{Case}	Case Operating Temperature	-40 to +100	°C	[4]

[1] Operation of this device above anyone of these parameters may cause permanent damage.
[2] Duration < 1s.
[3] The given values must not be exceeded at the same time even momentarily for any parameter, since each parameter is independent from each other. Otherwise deterioration or destruction of the device may take place.
[4] Max junction temperature must be considered
[5] Linked to and limited by I_{G_MAX} & I_{G_MIN} values. Maximum input power depends on frequency and should not exceed 2dB above PAE_max.

Biasing procedure

1. Bias power bar gate voltage at V_{GS} close to V_p (Typically: $V_{GS} \approx$ -5V)
2. Apply V_{DS} bias voltage (Typically: V_{DS} = 50V)
3. Increase V_{GS} up to quiescent bias drain current I_{D_Q}

The quiescent current steady state must be carefully controlled as it is influenced by the operating mode, the temperature and the overall thermal resistance.
A drain current control is recommended on the biasing network.

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Device thermal information

The thermal performances of the device are based on UMS rules to evaluate the junction temperature (Tj). This temperature is defined as the peak temperature in the channel area. This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime (see graph below) and activation energy for the particular technology on which the CHK015AaQIA is fabricated (GaN Power HEMT 0.5µm).

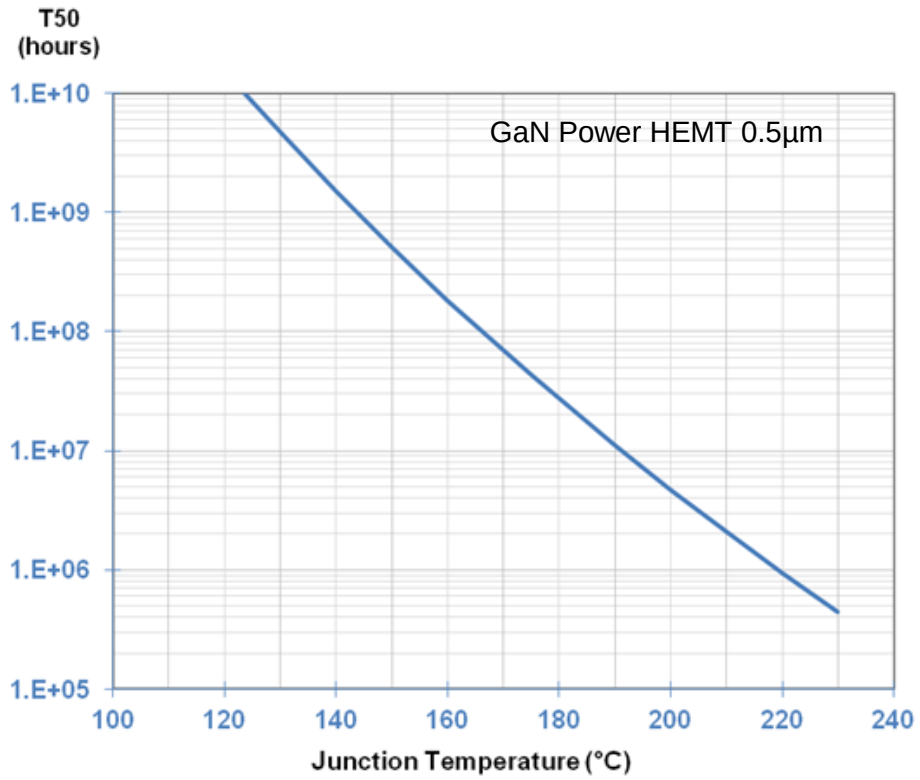
The temperature Tcase is defined as the package back side temperature.

The thermal resistance (Rth) is given in “equivalent” CW operating mode between junction and Tcase.

Parameters	Symbol	Conditions	Value	Unit
Typical Thermal Resistance	Rth	Packaged Device characteristic Tcase = 85°C Pdiss = 20W CW	5	°C/W
Junction Temperature	Tj		185	°C

The package back side temperature is considered uniform.

Median Life Time versus Junction Temperature



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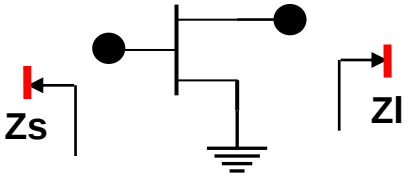
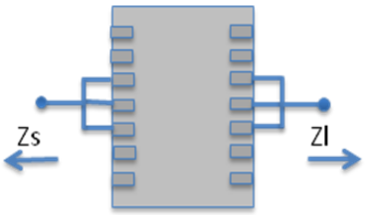
Simulated Source and Load Impedances

V_{DS} = 50V, I_{D_Q} = 75mA





Frequency (MHz)	Zs	Zl	Pout (W)	PAE (%)
1000	2.4 + j12.3	30 + j25	22	66
2000	1.5 + j3.5	14.7 + j19.7	21	64
3000	1.5 - j0.8	11 + j12.8	20.5	60
4000	1.2 - j4.3	6.2 + j8.3	20	59

The impedances are chosen as a trade-off between Output Power, PAE and Stability of the device. These values are given in the reference plane defined by the connection between the transistor leads and the PCB according to the footprint above mentioned.

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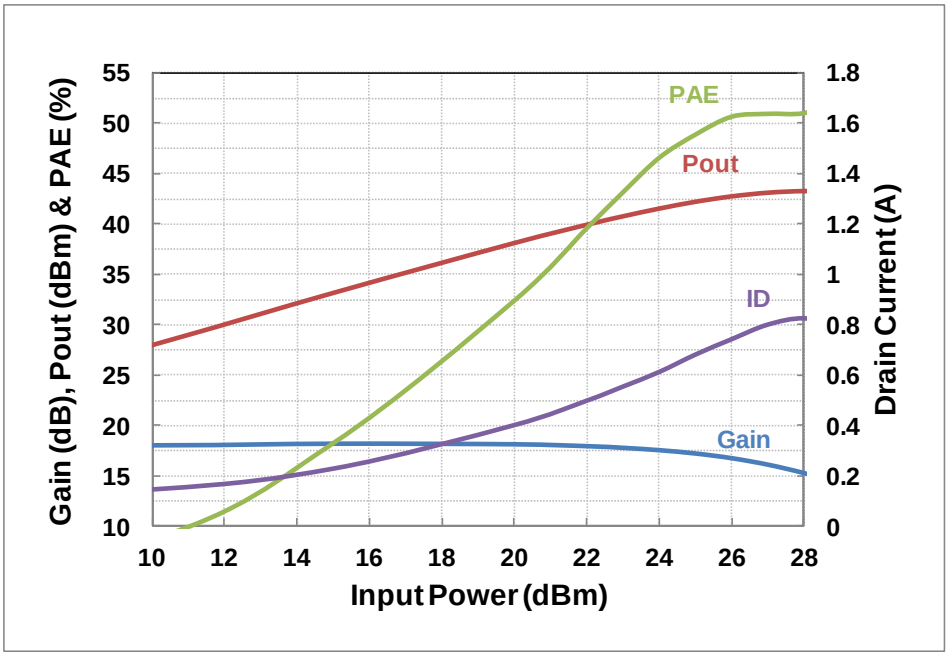
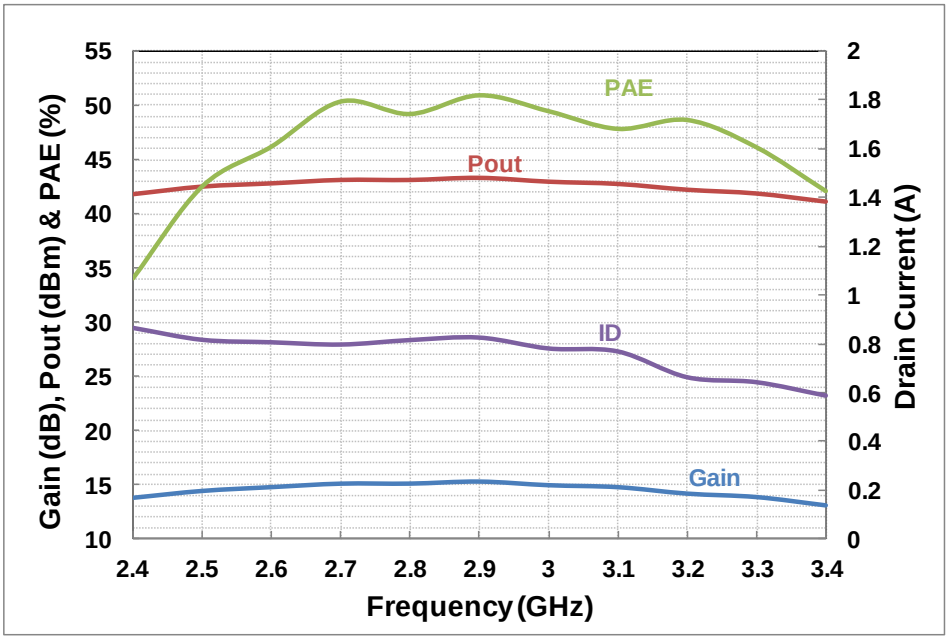
Typical Measured Performance on Evaluation Board (ref 61502522)

Calibration and measurements are done on the connector access planes of the evaluation boards.
Tamb. = +25°C, Pulsed Mode [(1)], V_{DS} = 50V, I_{D_Q} = 75mA

Pout. PAE. Gain & ID @ Freq = 2.9GHz



Pout. PAE. Gain & ID @ Pin = 28dBm



[(1)] Input RF and gate voltage are pulsed. Conditions are 1ms width. 10% duty cycle and 1µs offset between DC and RF pulse.

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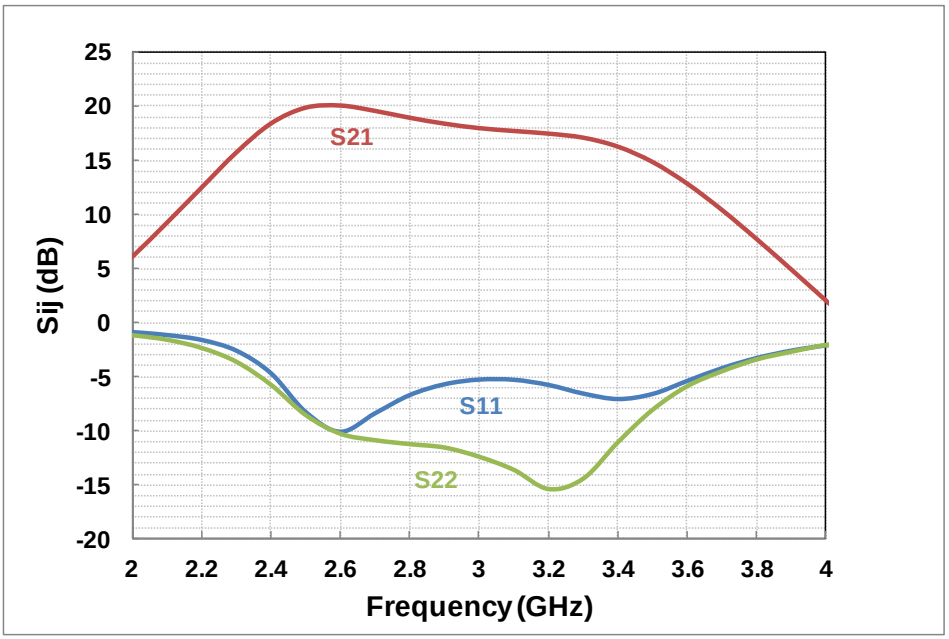
Typical Measured Performance on Evaluation Board (ref 61502522)

Calibration and measurements are done on the connector access planes of the evaluation boards.
Tamb. = +25°C, CW mode, V_{DS} = 50V, I_{D_Q} = 75mA

S parameters versus frequency



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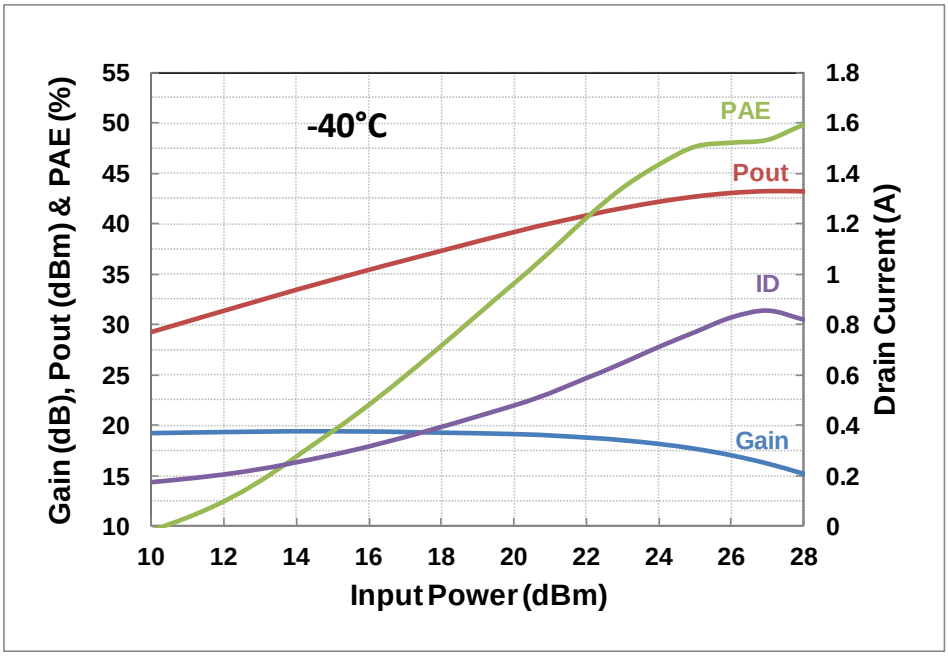
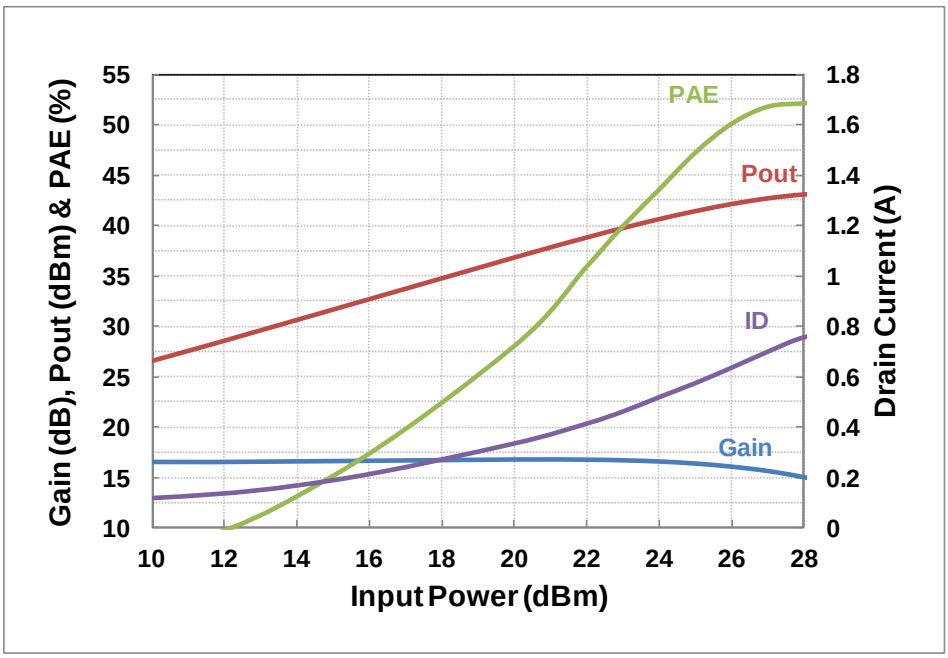
Typical Measured Performance in Temperature (Evaluation Board)

Calibration and measurements are done on the connector access planes of the evaluation boards.
Tamb. = -40°C & +85°C, Pulsed Mode [(1)], V_{DS} = 50V, I_{D_Q} = 75mA

Pout, PAE, Gain & Id @ 2.9GHz & -40°C



Pout, PAE, Gain & Id @ 2.9GHz & +85°C



[(1)] Input RF and gate voltage are pulsed. Conditions are 1ms width, 10% duty cycle and 1µs offset between DC and RF pulse.

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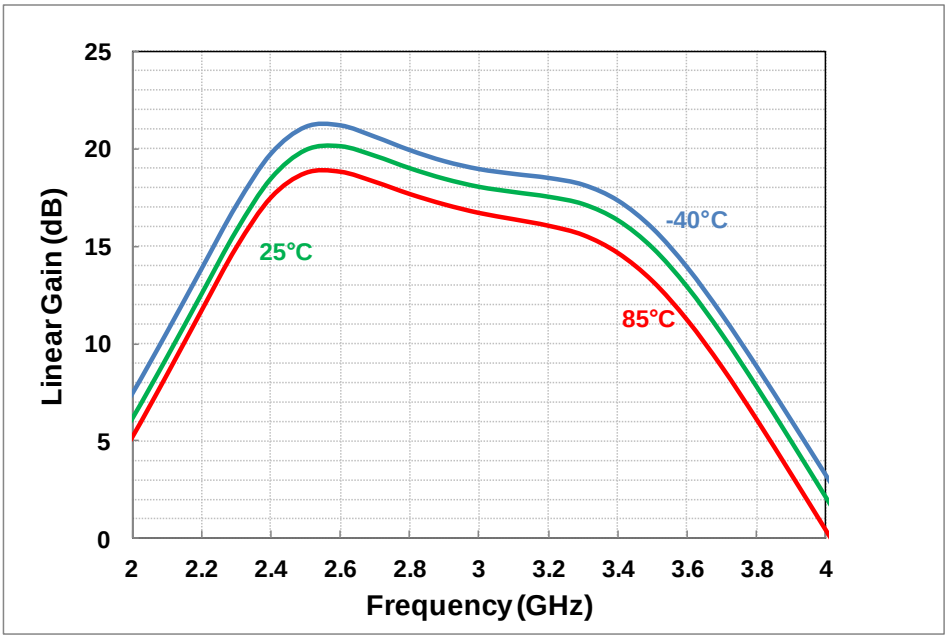
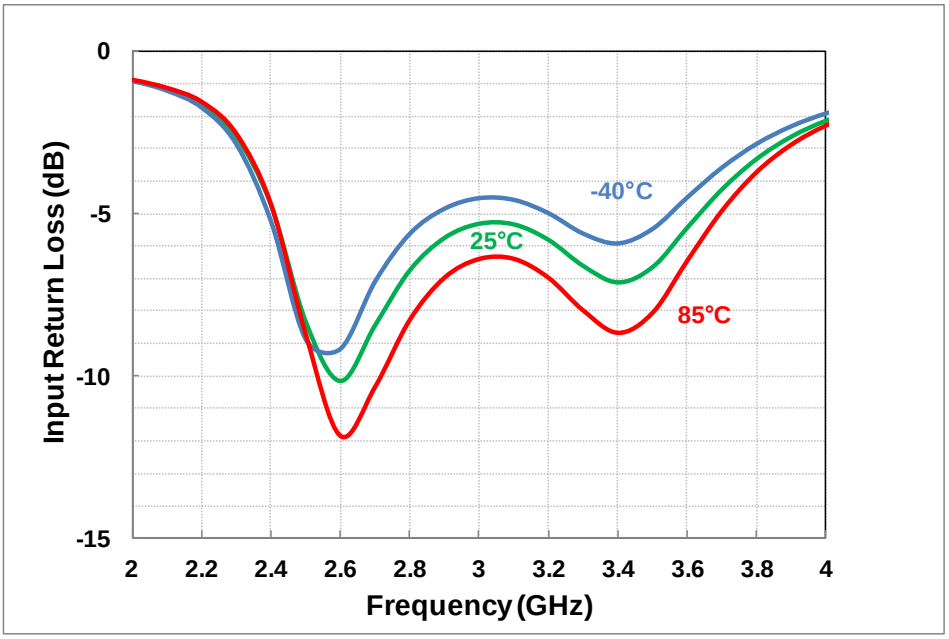
Typical Measured Performance in Temperature (Evaluation Board)

Calibration and measurements are done on the connector access planes of the evaluation boards.
Tamb. = -40°C, +25°C, +85°C, CW mode, V_{DS} = 50V, I_{D_Q} = 75mA (fixed @ +25°C)

Linear Gain versus temperature with ID_Q fixed @ each temperature (75mA)



Input Return Loss versus temperature with I_{D_Q} fixed @ each temperature (75mA)



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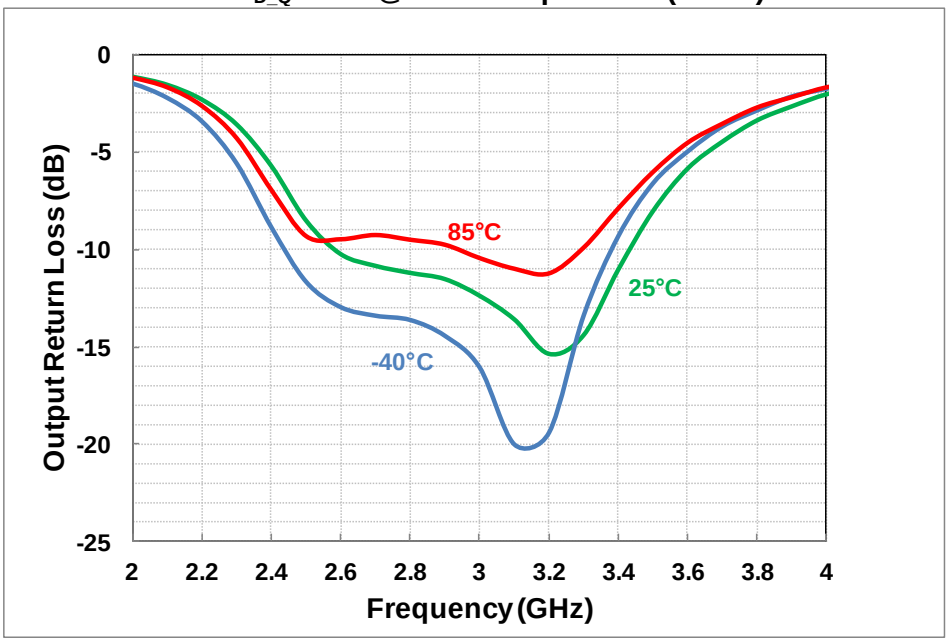
Typical Measured Performance in Temperature (Evaluation Board)

Calibration and measurements are done on the connector access planes of the evaluation boards.
Tamb. = -40°C, +25°C, +85°C, CW mode. V_{DS} = 50V, I_{D_Q} = 75mA (fixed @ +25°C)

Output Return Loss versus temperature with I_{D_Q} fixed @ each temperature (75mA)



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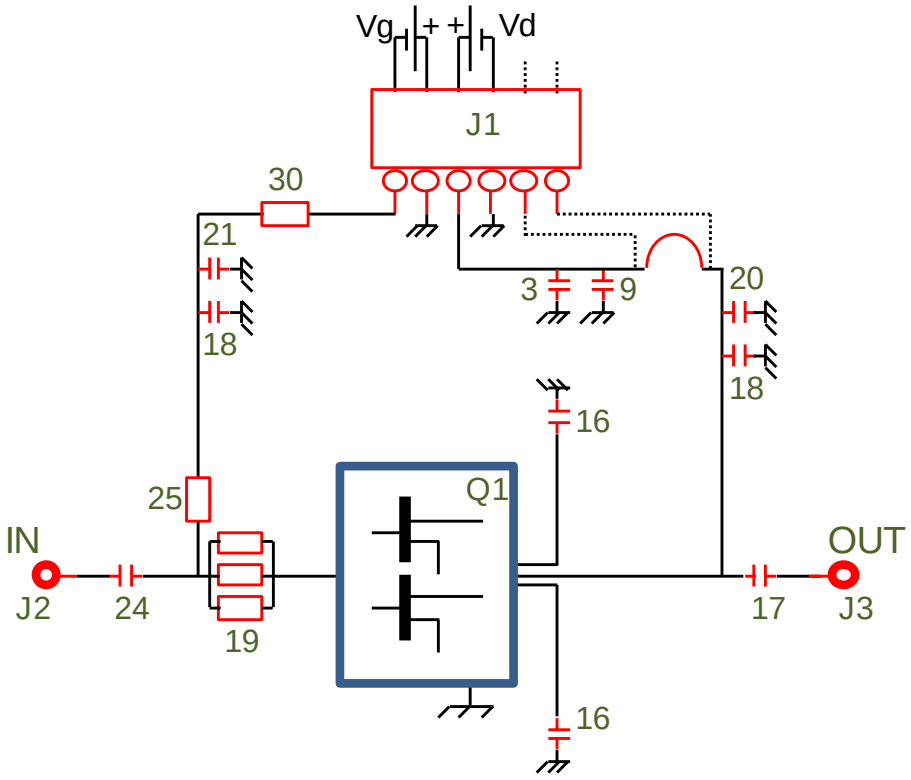
Demonstration Amplifier Low Frequency Equivalent Schematic (Ref. 61502522)



Demonstration Amplifier Bill of Materials (Ref. 61502522)

Designator	Type	Value - Description	Qty
24	Capacitor	1pF. +/- 0.1pF. 0603	1
16	Capacitor	4.7pF. +/- 0.25pF. 0603	1
17	Capacitor	3.9pF. +/- 0.25pF. 0603	1
18	Capacitor	20pF. +/- 5%. 0603	2
20	Capacitor	100pF. +/- 5%. 0603	1
21	Capacitor	1nF. +/- 5%. 0805	1
9	Capacitor	1µF. +/- 10%. 1210	1
3	Capacitor	68µF. +/- 20%	1
25	Resistor	49.9Ω. +/- 1%. 0603	1
19	Resistor	3Ω +/- 1%. 0603	3
30	Resistor	100Ω +/- 1%. 0603	1
J1	Connector	CMS 6cts	1
J2. J3	Connector	SMA	2
Q1	Packaged Transistor	CHK015A-QIA	1
-	PCB	TACONIC RF35P h=0.203mm	-

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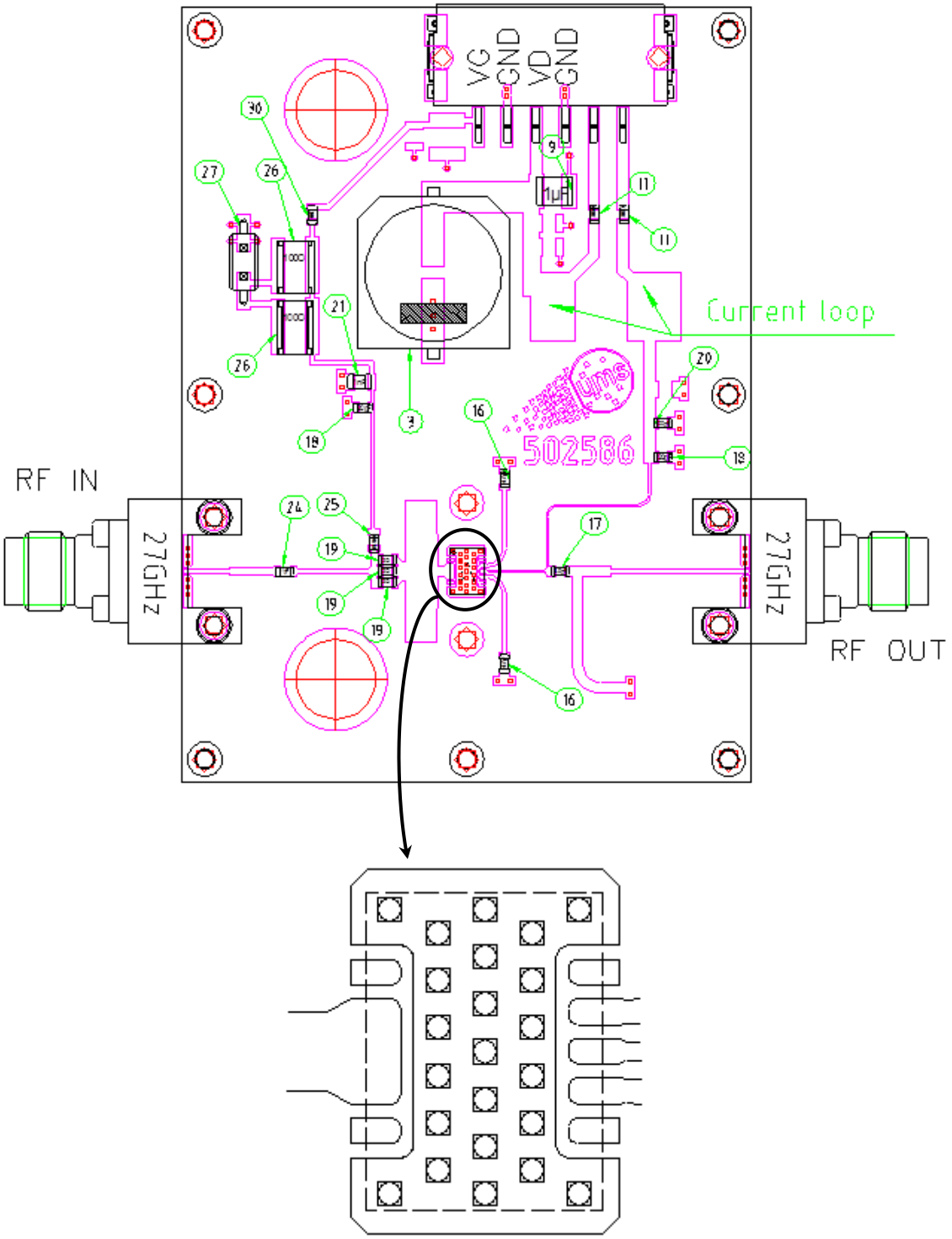
Demonstration Amplifier Circuit Outline (Ref. 61502522)



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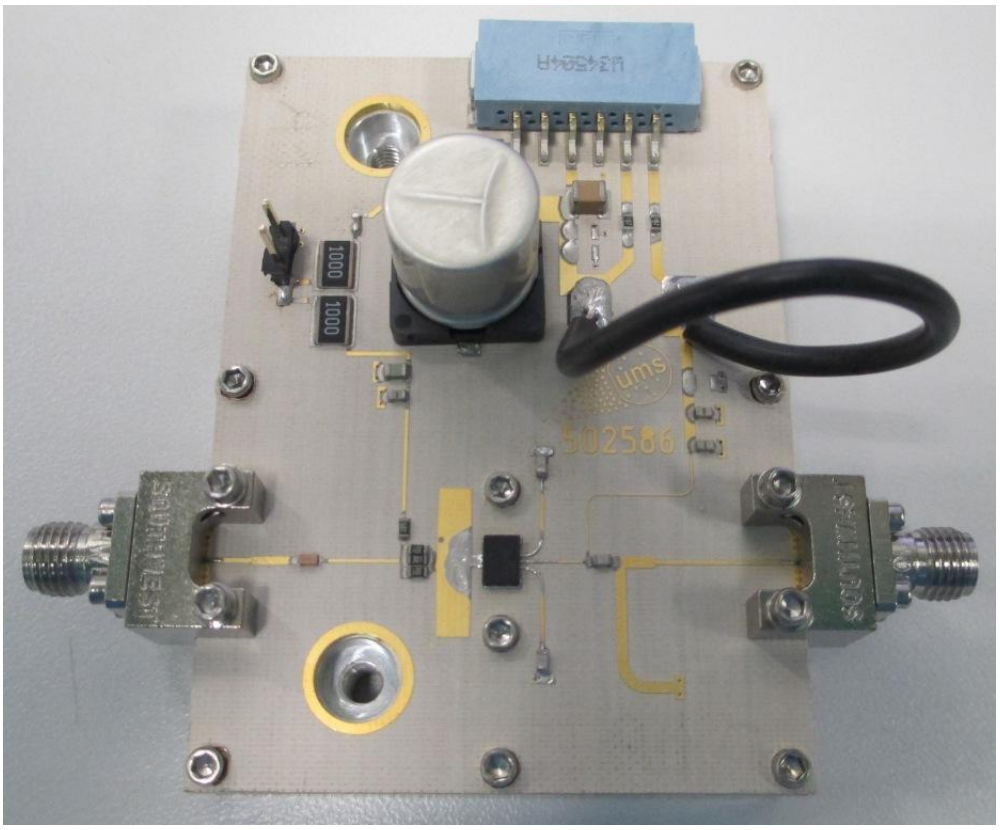
Demonstration Amplifier Circuit (Ref. 61502522)



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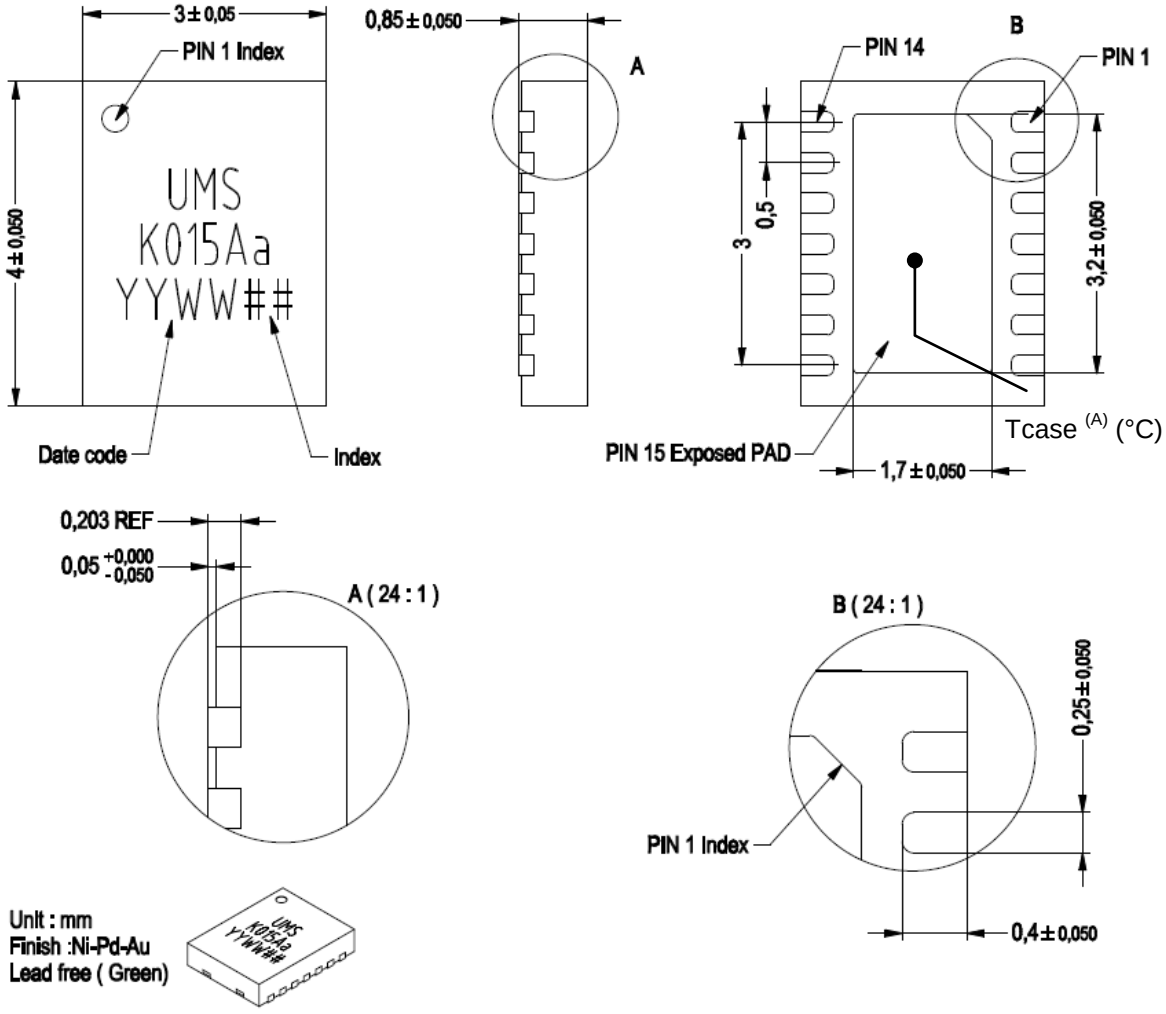
Package outline



1- Nc	6- Nc	11- D2
2- Nc	7- Nc	12- D1
3- G1	8- GND	13- Nc
4- G2	9- Nc	14- GND
5- G3	10- D3	15- GND

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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

DFN 3x4 package:	CHK015AaQIA/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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