United Monolithic Semiconductors

CHK9013-99F

85W Power Transistor

GaN HEMT on SiC

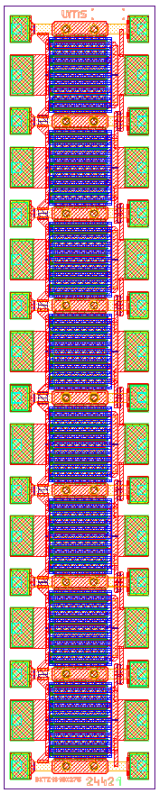
Description

The CHK9013-99F is a 85W Gallium Nitride High Electron Mobility Transistor.

This product offers a general purpose and broadband solution for a variety of RF power applications such as radar and telecommunication.

The circuit is manufactured on a 0.25µm gate length GaN HEMT technology on SiC substrate.

It is proposed in a bare die form and requires an external matching circuitry.



Main Features

- Wide band capability up to 8GHz
- Pulsed and CW operating modes
- GaN technology: High Pout & High PAE
- DC bias: V_D up to 30V
- Chip size: 0.9x4.27x0.1mm
- RoHS N°2011/65
- REACh N°1907/2006

Main Electrical Characteristics

Tref= +25°C, pulsed mode, Freq=6GHz, V_{DS}=30V, I_{D_Q}=1.1A

Symbol	Parameter	Min	Typ	Max	Unit
G_{SS}	Small Signal Gain		18		dB
P_{SAT}	Saturated Output Power		88		W
PAE	Max Power Added Efficiency		65		%
G_{PAE_MAX}	Associated Gain at Max PAE		14		dB

These values are deduced from elementary power cell performances.

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Recommended Operating Ratings

Tref = +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{DS}	Drain to Source Voltage			30	V	
V_{GS}	Gate to Source Voltage		-3.3		V	V_{DS}=30V, I_{D_Q}=1.1A
V_{DG_peak}	Drain-Gate Voltage		80		V	DC+RF
V_{GS_peak}	Gate-Source Voltage	-20			V	DC+RF
I_{D_Q}	Quiescent Drain Current		1.1	2.5 (1)	A	V_{DS}=30V
I_{D_MAX}	Drain Current			5.7 (1)	A	V_{DS}=30V, compressed mode
I_{G_MAX}	Gate Current in forward mode		0	90	mA	DC or Compressed mode
T_{j_MAX}	Junction temperature			200	°C	(1)

(1) Power dissipation must be considered.

DC Characteristics

Tref= +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_P	Pinch-Off Voltage	-4	-3.4	-2.8	V	V_D=10V,I_D= I_{DSS} /100
I_{D_SAT}	Saturated Drain Current		20		A	(1), V_D=10V, V_G=1V
I_{G_leak}	Gate Leakage Current	-4.4			mA	V_D=50V, V_G=-7V
V_{BDG}	Drain-Gate Break-down Voltage		120		V	V_G=-7V, I_D=20mA

(1) For information, limited by I_{D_MAX}, see on ROR & AMR.

RF Characteristics

Tref= +25°C, pulsed mode, Freq=6GHz, V_{DS}=30V, I_{D_Q}=1.1A

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
G_{SS}	Small Signal Gain		18		dB	
P_{SAT}	Saturated Output Power		88		W	
PAE	Max Power Added Efficiency		65		%	
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Absolute Maximum Ratings

Tref = +25°C[1] [2] [3]

Symbol	Parameter	Rating	Unit	Note
V_{DS}	Drain-Source Biasing Voltage	55	V	
V_{GS}	Gate-Source Biasing Voltage	-15, +2	V	[4], [5]
V_{DG_peak}	Drain-Gate Voltage (DC+RF)	120	V	
V_{GS_peak}	Gate-Source Voltage (DC+RF)	-25	V	
I_{G_MAX}	Maximum Gate Current	175	mA	
I_{G_MIN}	Minimum Gate Current	-11	mA	
I_{D_MAX}	Maximum Drain Current	See note		[4]
P_{IN}	Maximum Input Power	See note		[5]
T_j	Maximum Junction Temperature	230	°C	
T_{STG}	Storage Temperature	-55 to +150	°C	
T_{Case}	Case Operating Temperature	See note	°C	[4]

[1] Operation of this device above anyone of these parameters may cause permanent damage.
[2] Duration < 1s.
[3] The given values must not be exceeded at the same time even momentarily for any parameter, since each parameter is independent from each other, otherwise deterioration or destruction of the device may take place.
[4] Max junction temperature must be considered.
[5] Linked to and limited by Ig_max & Ig_min values. Maximum input power depends on frequency and should not exceed 2dB above PAE_max.

Biasing procedure

1. Bias power bar gate voltage at Vg close to $V_{pinch\text{-}off}$ (Typically: $V_{GS} \approx -5V$)
2. Apply V_{DS} bias voltage (Typically: $V_{DS} = 30V$)
3. Increase V_{GS} up to quiescent bias drain current I_{D_Q}

The quiescent current steady state must be carefully controlled as it is influenced by the operating mode, the temperature and the overall thermal resistance.
A drain current control is recommended on the biasing network.

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Device thermal information

The thermal performances of the device are based on UMS rules to evaluate the junction temperature (Tj). This temperature is defined as the peak temperature in the channel area.
This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHK9013-99F is fabricated (GaN Power PHEMT 0.25µm).
The temperature Tb is defined as the chip back side temperature
The thermal resistance (Rth) is given for the full power bar, in "equivalent" CW operating mode and in two different configurations as given in the table. The device assembly must be adapted to the operating mode. Thermal analysis is recommended. More information is available on request.

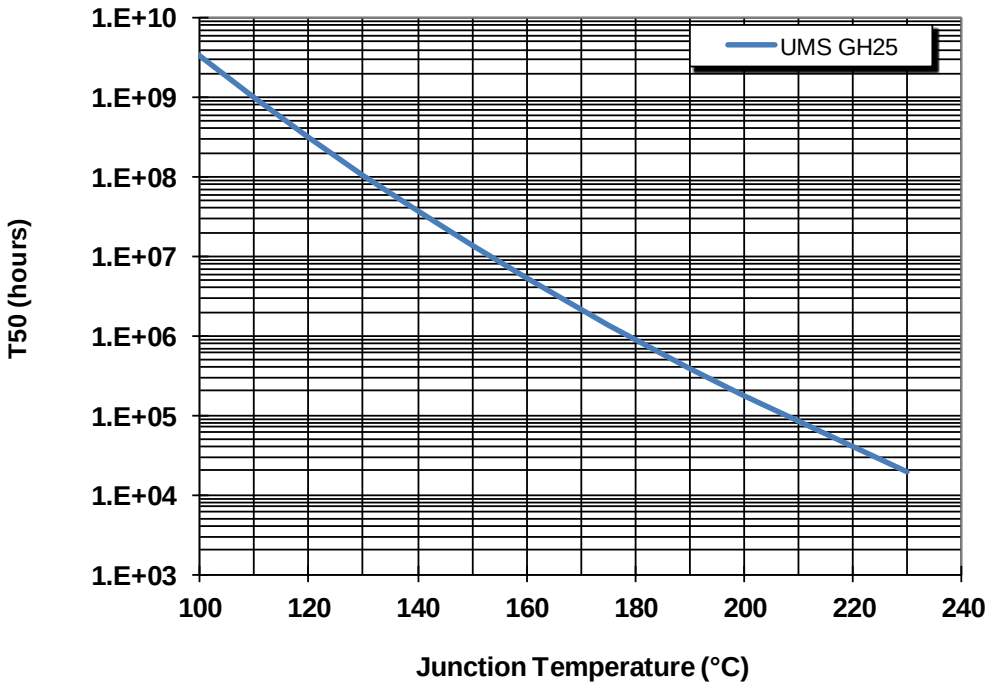
Parameters	Symbol	Conditions	Value	Unit
Typical Thermal Resistance	Rth	Bare die characteristic Tb=125°C Pdiss=83W **CW**	0.9	°C/W
Junction Temperature	Tj		200	°C

The back side temperature (Tb) is considered uniform on all the surface

Typical Thermal Resistance	Rth	Bare die on carrier characteristic Tc=85°C Pdiss=55W **CW**	2.1	°C/W
Junction Temperature	Tj		200	°C

The reference temperature (Tc) is defined on the carrier back side. The power bar is mounted on carrier plate (20µm Au/Sn soldering + 1.4mm Cu/Mo/Cu).

Median Life Time versus Junction Temperature



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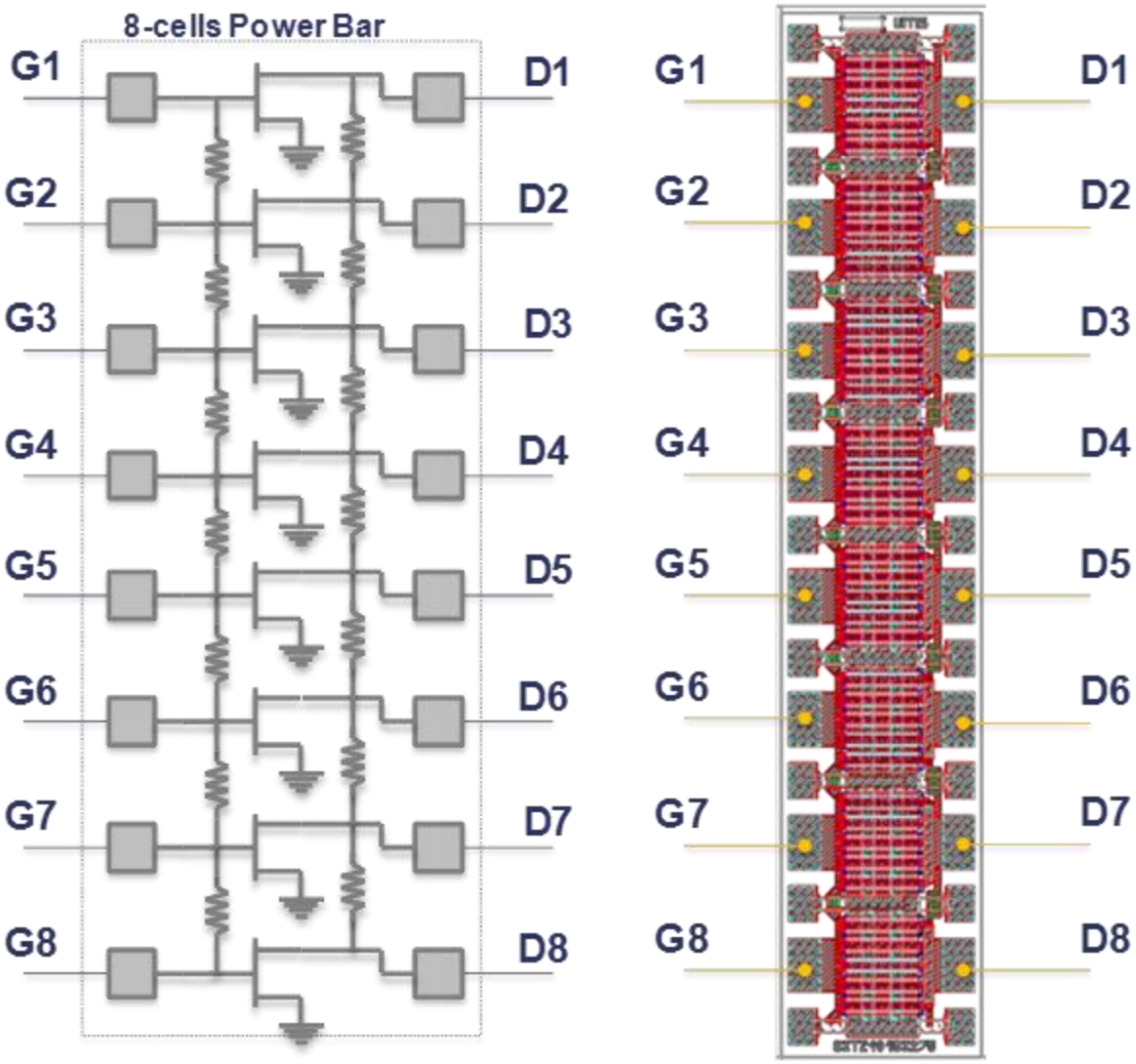
Power Bar Description

The device is composed of 8x11W elementary cells. These cells are connected together with a specific network providing a good trade-off between performance and stability (resistance between gates and drains as described on the schematic). The reference planes are on the center of the bonding pads.
A multiport non-linear model is available on request.



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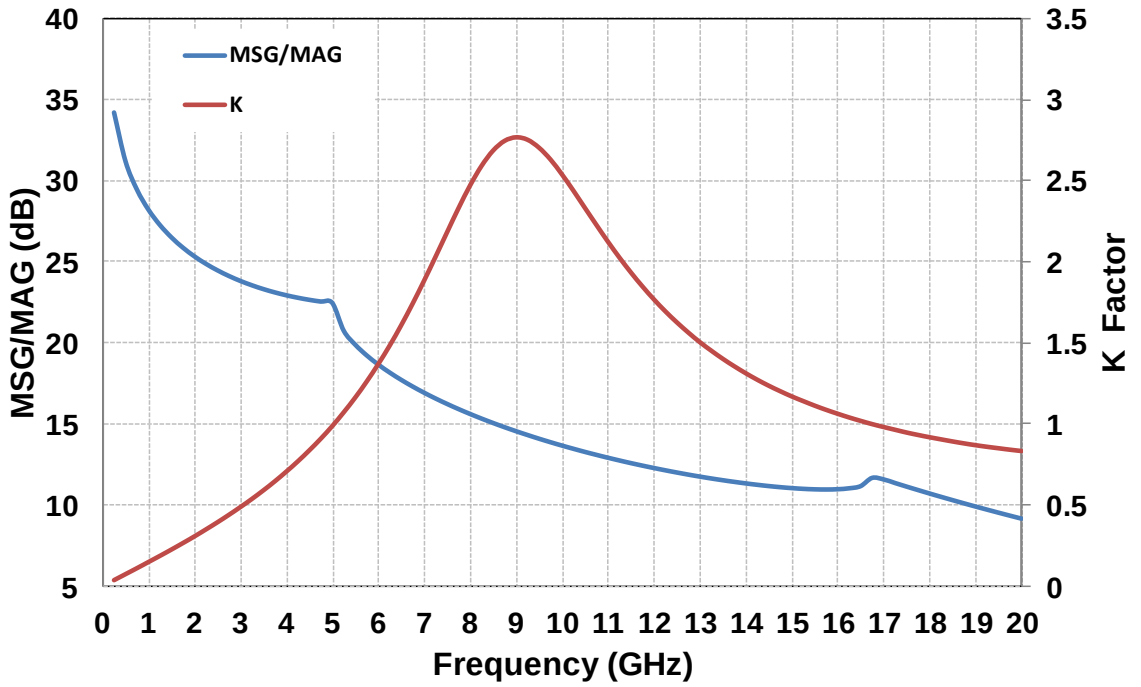
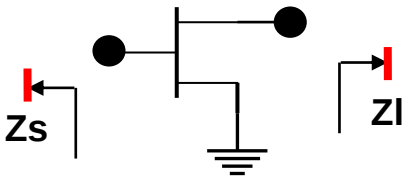
Elementary Cell Maximum Gain & Stability Characteristics

Tref = +25°C, V_{DS} = +30V, I_{D_Q} = 140mA, simulated results



Elementary Cell Load Pull Performances

Tref = +25°C, V_{DS} = +30V, I_{D_Q} = 140mA, simulated results



The impedances are chosen as a trade-off between Output Power, PAE and Stability of the device. Second harmonic of output load has been tuned.
These values are given in the bonding pads reference plane.

Frequency (GHz)	Zs	Zl	Gain (dB) @PAE_{max}	Pout (W) @PAE_{max}	PAE_{max} (%)	$Pout_{max}$ (W)
1	11.6+ j28.4	51+ j20.3	16	12.5	75	13.2
3	2.2+ j11	23.8+ j27.1	16	11.4	72	12.4
5	1.3+ j5.5	11.4+ j20.7	15	11.3	69	12.3
7	1.5+ j2.9	8.7+ j15.4	11.5	11.2	63	12
8	1.3+ j1.6	5.4+ j13.4	10	10.5	62	11

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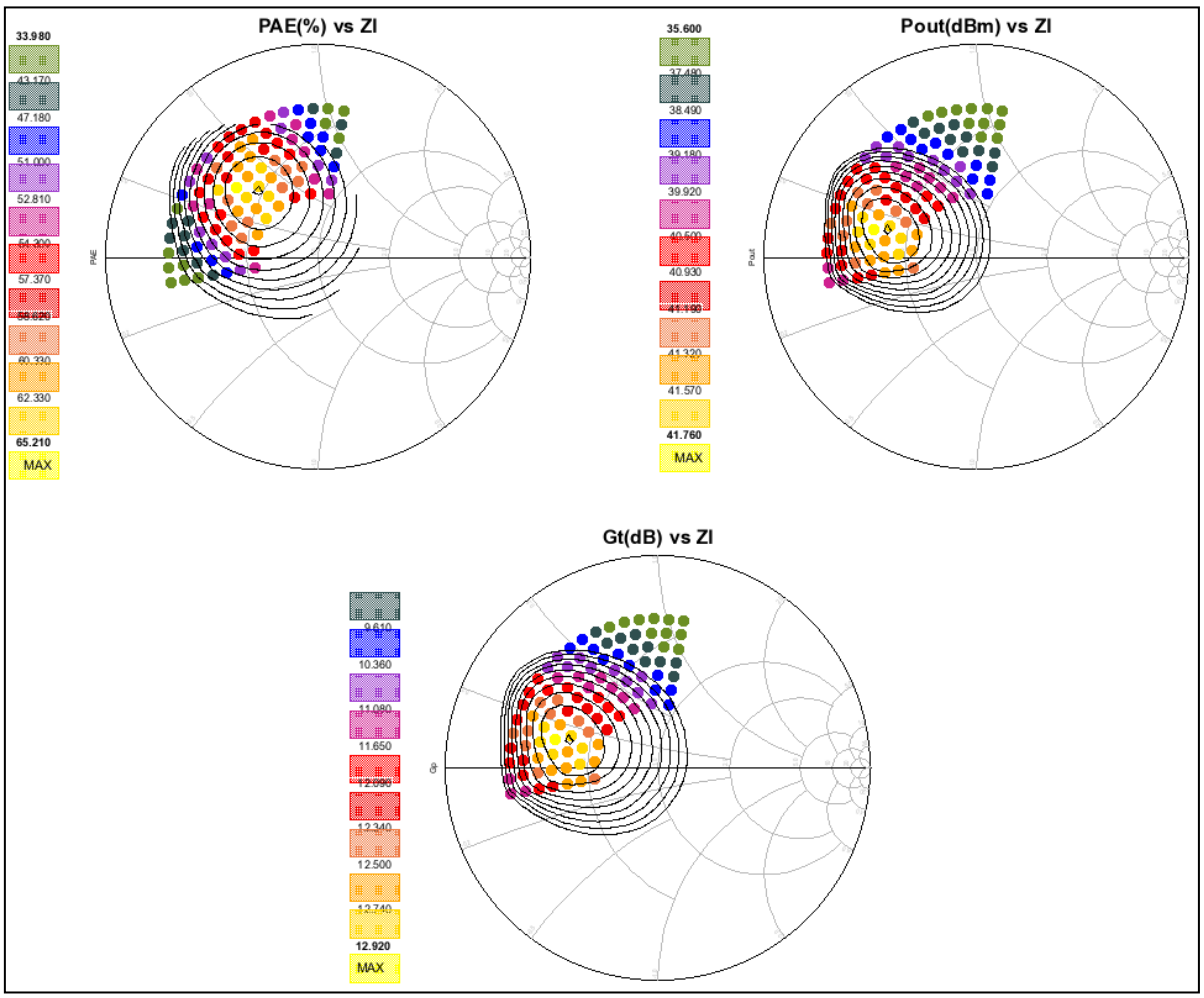
Comparison Simulation/Measurement of Elementary Cell Load Pull Performances

Tref= +25°C, Vg pulsed mode 10µs - 10%, Freq=3GHz, V_{DS}=28V, I_{D_Q}=0mA/mm (Class B)

- ZloadH2=ZloadH3=50Ω
- Zsource matched for maximum gain
- On wafer measurement
- Measurement are given in the transistor plan at 5dB of compression

PAE(%), Output Power (dBm) and transducer gain (dB) vs the load impedance



Measurements are represented by multicolour dots and model by black contours.

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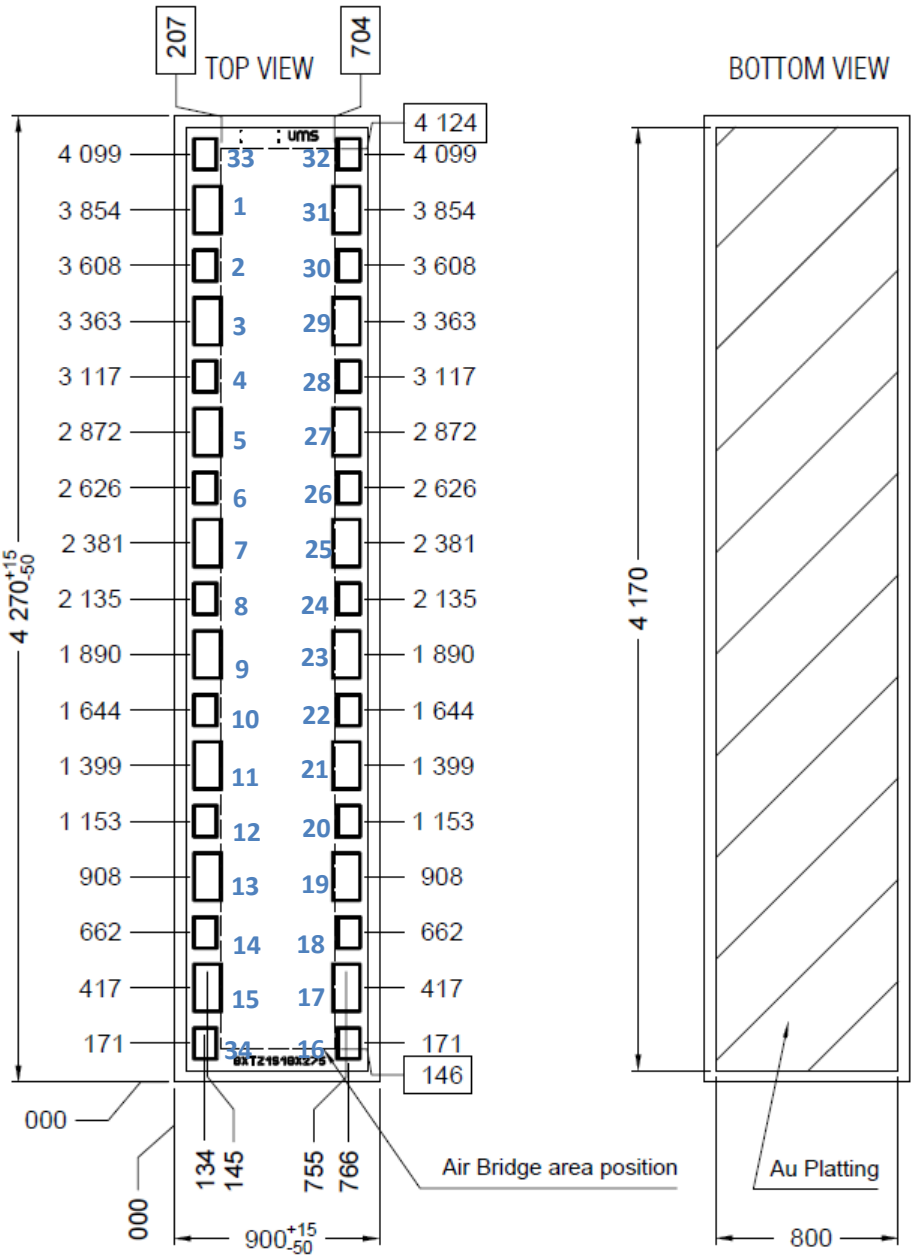
Mechanical data



Chip thickness: 100µm +/- 10 µm
All dimensions are in micrometers

All Gate and Drain pads must be connected, ground connection is optional (source is grounded through vias hole)

Reference	Pad number	Pad size
DC Gate pads	(1, 3, 5, 7, 9, 11, 13, 15)	204 x 115µm²
DC Drain pads	(17, 19, 21, 23, 25, 27, 29, 31)	204 x 115µm²
GND pads	(2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, 33, 34)	117x113µm²

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Notes

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Qualification domain

This part is qualified according to UMS standards, excluding humid environment.

User guide for MMIC storage, pick & place, die attach, wire bonding

Refer to the application note AN0001 available at http://www.ums-gaas.com for general recommendations on chip handling.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

User guide GaN Power Bars Assembly guide lines

Refer to the application note AN0026 available at http://www.ums-gaas.com for general recommendations on GaN-on-SiC Transistor handling and assembly.

Ordering Information

Chip form:	CHK9013-99F/00

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