

15W L-Band Driver

GaN HEMT on Sic in SMD leadless package

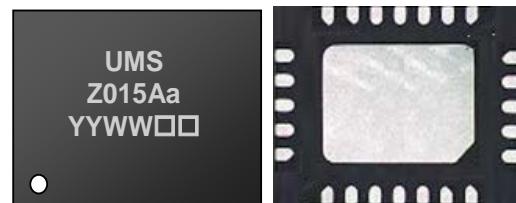
Description

The CHZ015AaQEG is an input matched packaged Gallium Nitride High Electron Mobility Transistor.

It allows broadband solutions for a variety of RF power applications in L-band. The circuit is well suited for pulsed radar application.

The CHZ015AaQEG is proposed on a $0.5\mu\text{m}$ gate length GaN HEMT process. It is based on Quasi MMIC technology.

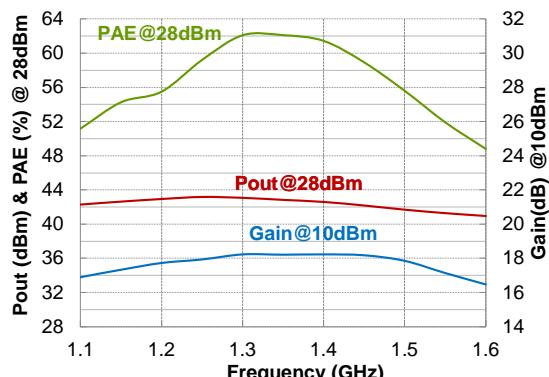
It is supplied in RoHS compliant SMD package.



Main Features

- Wide band capability: 1.2 - 1.4GHz
- Pulsed operating mode
- High power: > 15W
- High PAE: up to 60%
- DC bias: $V_{DS}=45V$ @ $I_{D_Q}=100\text{mA}$
- Low cost package: 24L-QFN4x5
- MTTF > 10^6 hours @ $T_j=200^\circ\text{C}$

$V_{DS} = 45V$, $I_{D_Q} = 100\text{mA}$, $\text{Pin} = 28\text{dBm}$
Pulsed mode (1ms-10%)



Performances on the connector access planes

Main Electrical Characteristics

Tamb.= +25°C, pulsed mode, $V_{DS}=45V$, $I_{D_Q}=100\text{mA}$

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	1.2		1.4	GHz
G_{SS}	Small Signal Gain	16.7	17.2		dB
P_{OUT}	Output Power	41.5	42.5		dBm
PAE	Max Power Added Efficiency	50	55		%
I_{dSAT}	Saturated Drain Current			750	mA

Recommended DC Operating Ratings

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V _{DS}	Drain to Source Voltage	20	45	50	V	
V _{GS_Q}	Gate to Source Voltage		-1.9		V	V _{DS} =45V, I _{D_Q} =50mA
I _{D_Q}	Quiescent Drain Current		50	350	mA	V _{DS} =45V
I _{D_MAX}	Drain Current		750	⁽¹⁾	mA	V _{DS} =45V, Compressed mode
I _{G_MAX}	Gate Current (forward mode)		0	16	mA	Compressed mode
P _W	Pulse width			1.5	ms	
D _C	Duty cycle		10		%	
Top	Operating temperature range	-40		+85	°C	
T _{j_MAX}	Junction temperature			200	°C	

⁽¹⁾ Limited by dissipated power.

DC Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V _P	Pinch-Off Voltage	-2.7	-2	-1.5	V	V _{DS} = 10V, I _{DS} = I _{DSS} /100
I _{D_SAT} ⁽²⁾	Saturated Drain Current		2.4		A	V _{DS} = 10V, V _{GS} = 1V ⁽¹⁾
I _{G_leak}	Gate Leakage Current (reverse mode)	-0.8			mA	V _{DS} =50V, V _{GS} =-7V ⁽¹⁾
V _{BDS}	Drain-Source Break-down Voltage		180		V	V _{GS} = -7V, I _{DS} = 20mA ⁽¹⁾

⁽¹⁾ Parameters extrapolated from unit cell measurement.

⁽²⁾ For information, limited by I_{D_MAX}, see on Absolute Maximum Ratings.

RF Characteristics ⁽¹⁾Tamb.= +25°C, pulsed mode ⁽²⁾, on board 61504312⁽¹⁾, V_{DS}=45V, I_{D_Q}=50mA, I_{D_Q}=100mA

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	1.2		1.4	GHz
G _{SS}	Small Signal Gain @ I _{D_Q} =50mA ⁽³⁾	15.5	16.0		dB
G _{SS}	Small Signal Gain @ I _{D_Q} =100mA	16.7	17.2		dB
dG _{SS}	Small Signal Gain flatness		+/-0.6		dB
P _{SAT}	Saturated Output Power	41.5	42.5		dBm
PAE	Power Added Efficiency	50	55		%
I _{DSAT}	Saturated Drain Current		750		mA
Rlin	Input Return Loss		-12	-9	dB

⁽¹⁾ Measured on evaluation board 61504312 on the connector access planes.⁽²⁾ Input RF and gate voltage are pulsed. Conditions are 1ms width, 10% duty cycle and 1µs offset between RF and DC pulse.⁽³⁾ Recommended biasing point for better linearity

Absolute Maximum Ratings

Tamb.= +25°C ^{(1), (2), (3)}

Symbol	Parameter	Rating	Unit	Note
V _{DS}	Drain-Source Voltage	60	V	
V _{GS_Q}	Gate-Source Voltage	-10, +2	V	^{(4), (6)}
I _{G_MAX}	Maximum Gate Current in forward mode	32	mA	
I _{G_MIN}	Maximum Gate Current in reverse mode	-2	mA	
I _{D_MAX}	Maximum Drain Current	2	A	⁽⁴⁾
P _{IN}	Maximum Input Power	32	dBm	⁽⁵⁾
P _{W_MAX}	Pulse width	3	ms	
D _{C_MAX}	Duty cycle	20	%	
Top	Operating temperature range	-40 to +100	°C	
T _j	Junction Temperature	230	°C	
T _{STG}	Storage Temperature	-55 to +150	°C	

⁽¹⁾ Operation by this device above anyone of these parameters may cause permanent damage.

⁽²⁾ Duration < 1s.

⁽³⁾ The given values have not to be exceeded at the same time even momentarily for any parameter, since each parameter is independent from each other, otherwise deterioration or destruction of the device may take place.

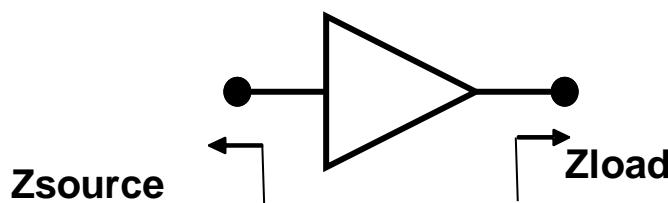
⁽⁴⁾ Max junction temperature has to be considered.

⁽⁵⁾ Linked to and limited by I_{G_MAX} & I_{G_MIN} values.

⁽⁶⁾ V_{GS_Q} max limited by I_{D_MAX} and I_{G_MAX} values.

Simulated Source and Load Impedance

V_{DS} = 45V, I_{D_Q} = 50mA



Frequency (GHz)	Source	Load
Typical [1.2-1.4]	50 + j0	27 + j23

These values are defined at the package interface with PCB.

Device thermal information

The thermal performances of the device are based on UMS rules to evaluate the junction temperature (T_j). This temperature is defined as the peak temperature in the channel area.

This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime (see graph below) and activation energy for the particular technology on which the CHZ015AaQEG is fabricated (GaN Power HEMT 0.5μm).

The temperature T_{case} is defined as the package back side temperature.

The thermal resistance (R_{th}) is given in "equivalent" CW operating mode between junction and T_{case} . For information, the R_{th} is also given on the UMS Evaluation Board, defined between junction and T_{ref} .

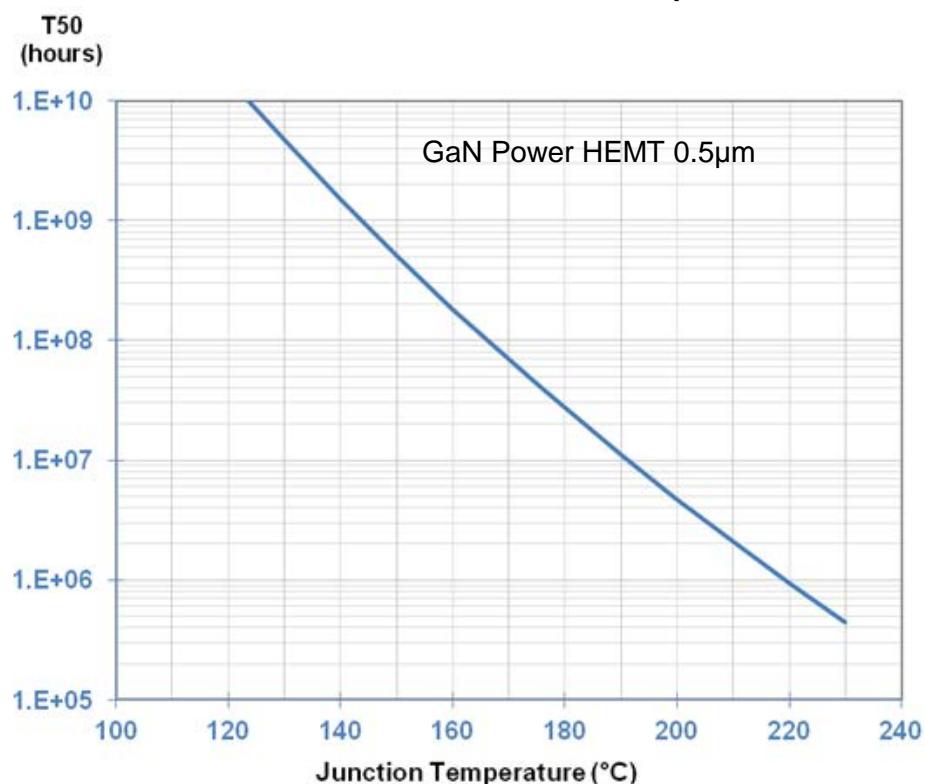
Parameters	Symbol	Conditions	Value	Unit
Typical Thermal Resistance	R_{th}	Packaged Device characteristic $T_{case} = 85^\circ\text{C}$ $P_{diss} = 20\text{W}$ CW	5	°C/W
Junction Temperature	T_j		185	°C

T_{case} = Package Backside Temperature

Parameters	Symbol	Conditions	Value	Unit
Typical Thermal Resistance	R_{th}	Packaged Device on board characteristic $T_{ref} = 85^\circ\text{C}$ $P_{diss} = 14.5\text{W}$ CW	7.85	°C/W
Junction Temperature	T_j		200	°C

T_{ref} = Reference temperature of the thermal drain below the PCB

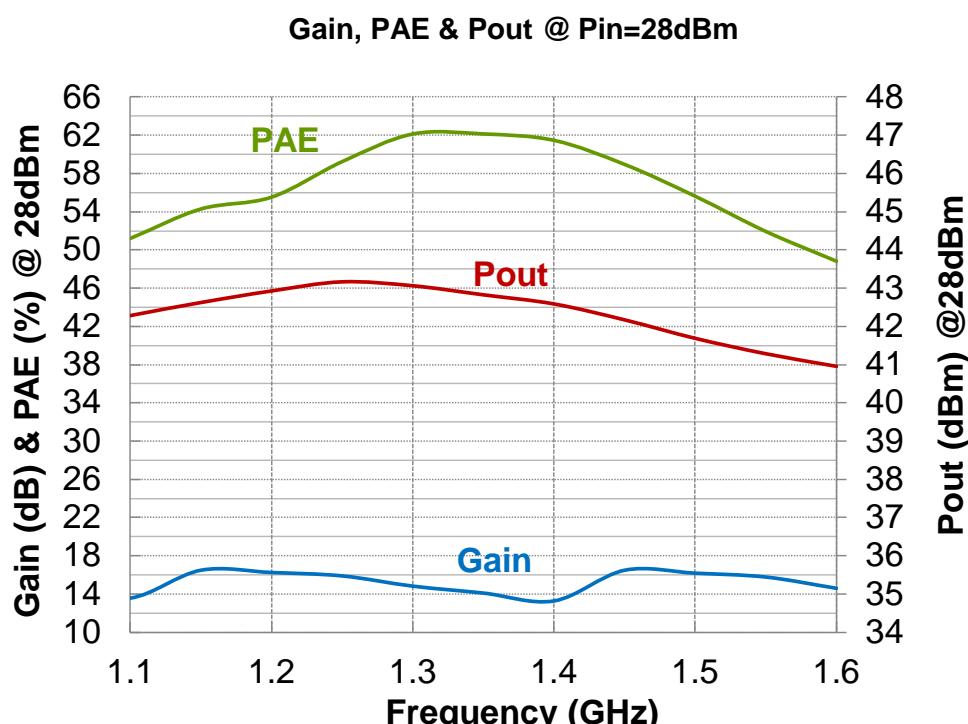
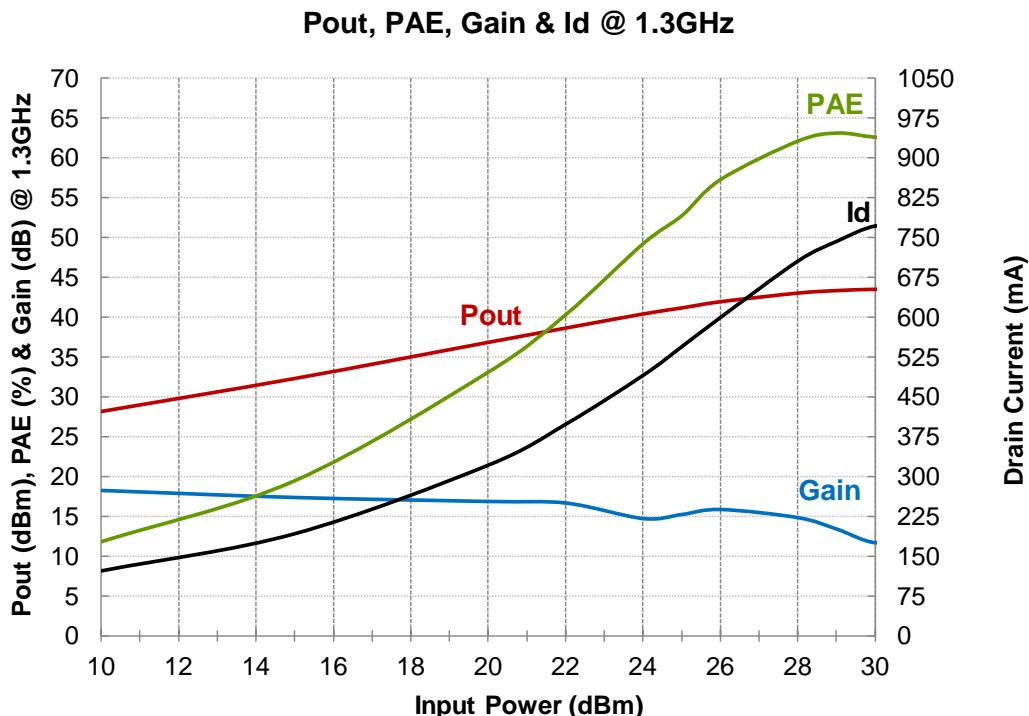
Median Life Time versus Junction Temperature



Typical Performance on Evaluation Board (ref 61504312)

Calibration and measurements are performed on the connector access planes of the evaluation boards.

Tamb.= +25°C, pulsed mode⁽¹⁾, V_{DS}=45V, I_{D_Q}=100mA



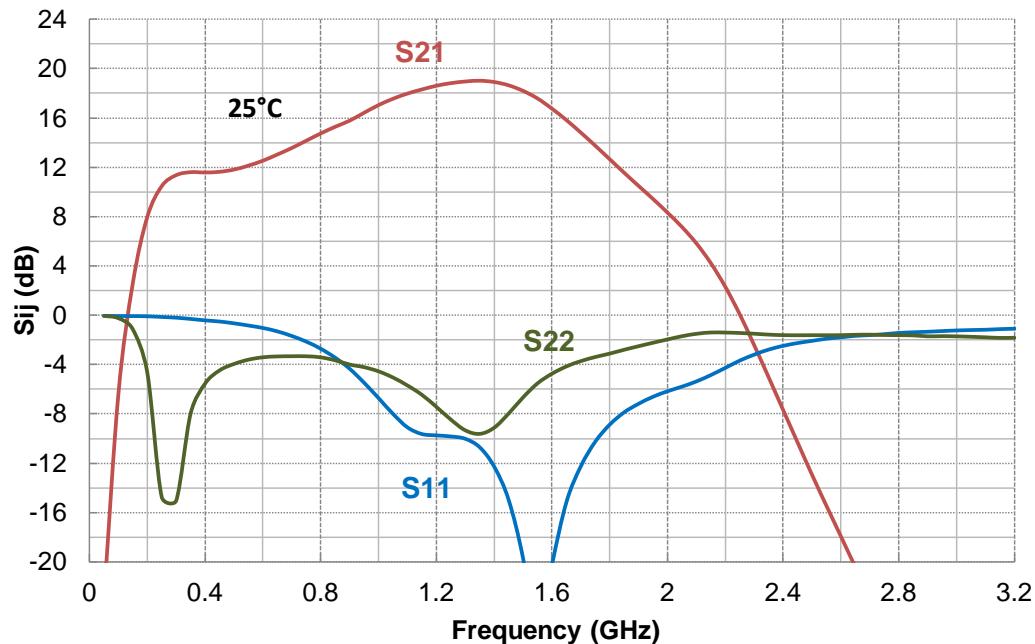
⁽¹⁾ Input RF and gate voltage are pulsed. Conditions are 1ms width, 10% duty cycle and 1μs offset between DC and RF pulse.

Typical Performance on Evaluation Board (ref 61504312)

Calibration and measurements are performed on the connector access planes of the evaluation boards.

Tamb.= +25°C, **pulsed mode**⁽¹⁾, V_{DS}=45V, I_{D_Q}=100mA

S parameters versus frequency



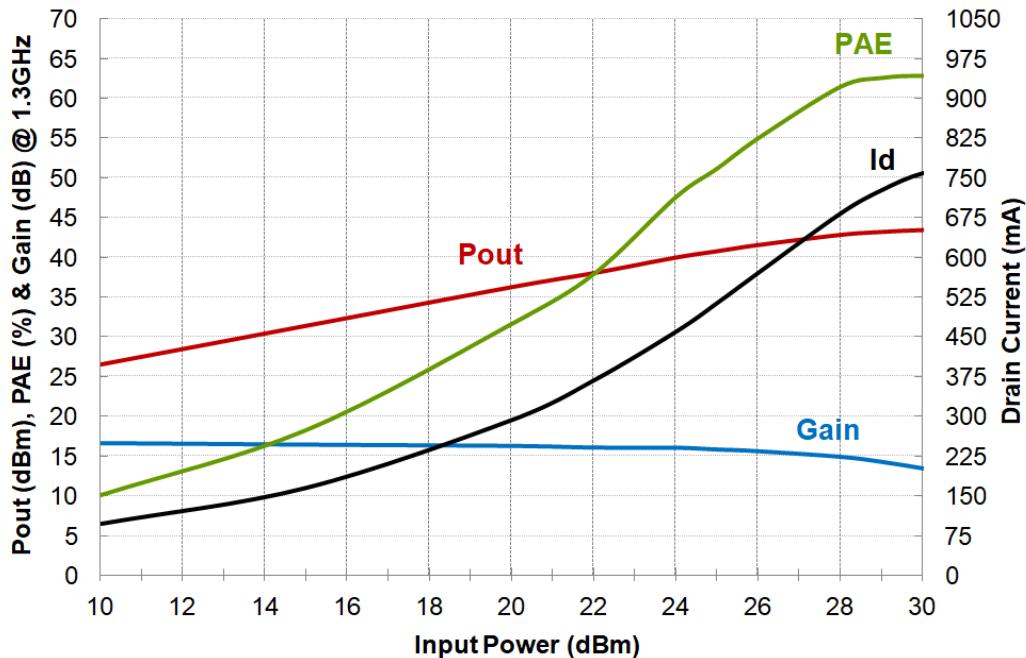
⁽¹⁾ Input RF and gate voltage are pulsed. Conditions are 1ms width, 10% duty cycle and 1μs offset between DC and RF pulse.

Typical Performance on Evaluation Board (ref 61504312)

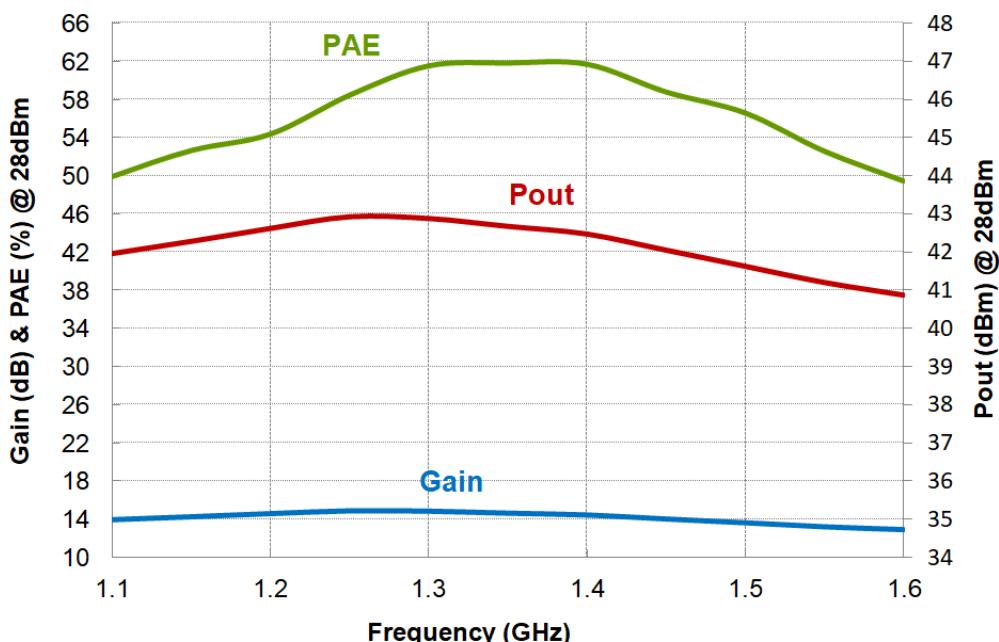
Calibration and measurements are performed on the connector access planes of the evaluation boards.

Tamb.= +25°C, pulsed mode ⁽¹⁾, V_{DS}=45V, I_{D_Q}=50mA

Pout, PAE, Gain & Id @ 1.3GHz



Gain, PAE & Pout @ Pin=28dBm



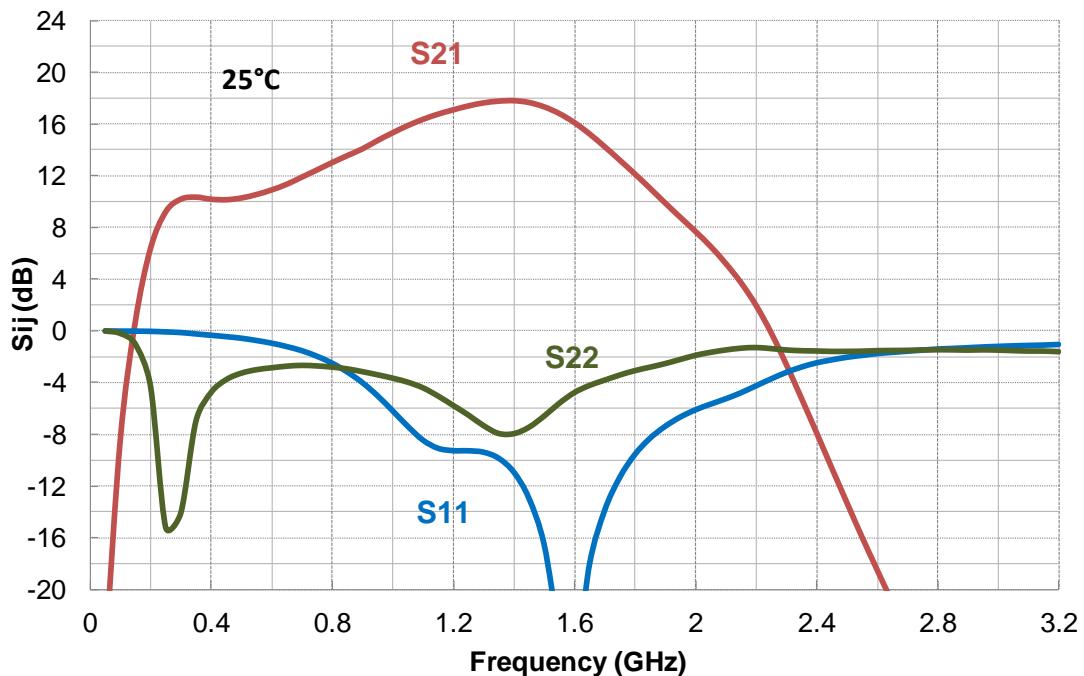
⁽¹⁾ Input RF and gate voltage are pulsed. Conditions are 1ms width, 10% duty cycle and 1μs offset between DC and RF pulse.

Typical Performance on Evaluation Board (ref 61504312)

Calibration and measurements are performed on the connector access planes of the evaluation boards.

Tamb.= +25°C, **pulsed mode**⁽¹⁾, V_{DS}=45V, I_{D_Q}=50mA

S parameters versus frequency



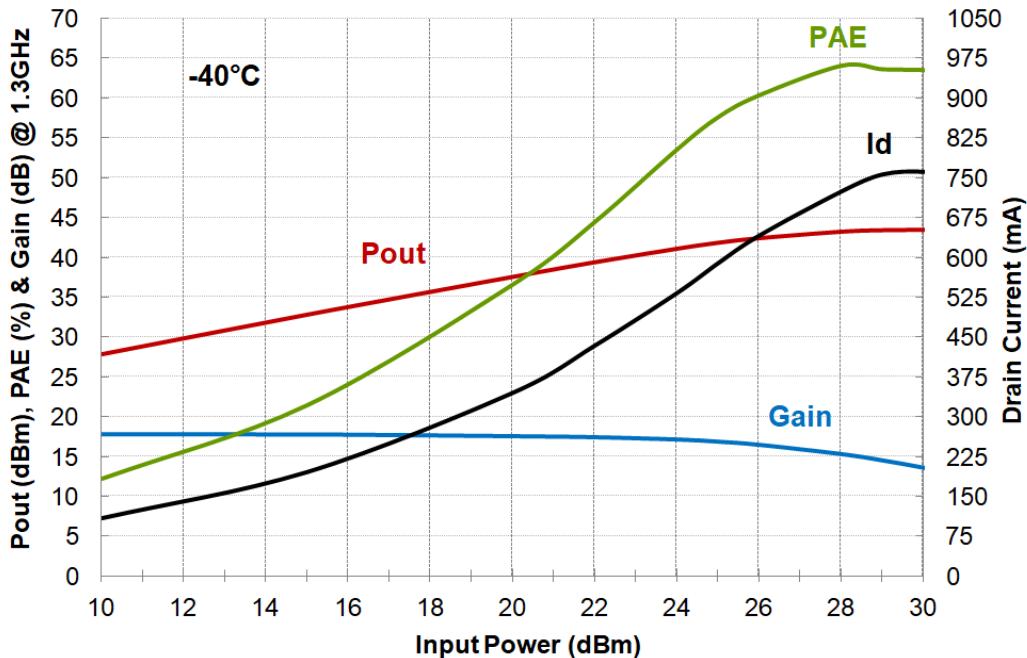
⁽¹⁾ Input RF and gate voltage are pulsed. Conditions are 1ms width, 10% duty cycle and 1μs offset between DC and RF pulse.

Typical Performance in Temperature (on evaluation board)

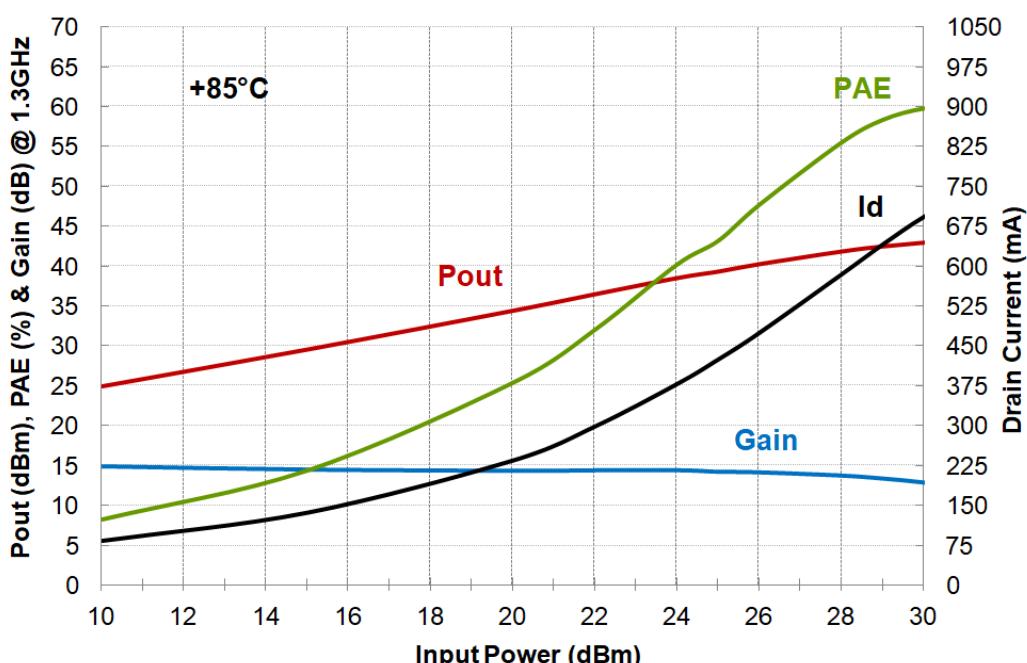
Calibration and measurements are performed on the connector access planes of the evaluation boards (ref 61501358).

Tamb.= -40°C, +25°C, +85°C, **pulsed mode**⁽¹⁾, V_{DS}=45V, V_{gs} fixed (I_{D_Q}=50mA @ +25°C)

Pout, PAE, Gain & Id @ 1.3GHz & -40°C



Pout, PAE, Gain & Id @ 1.3GHz & +85°C



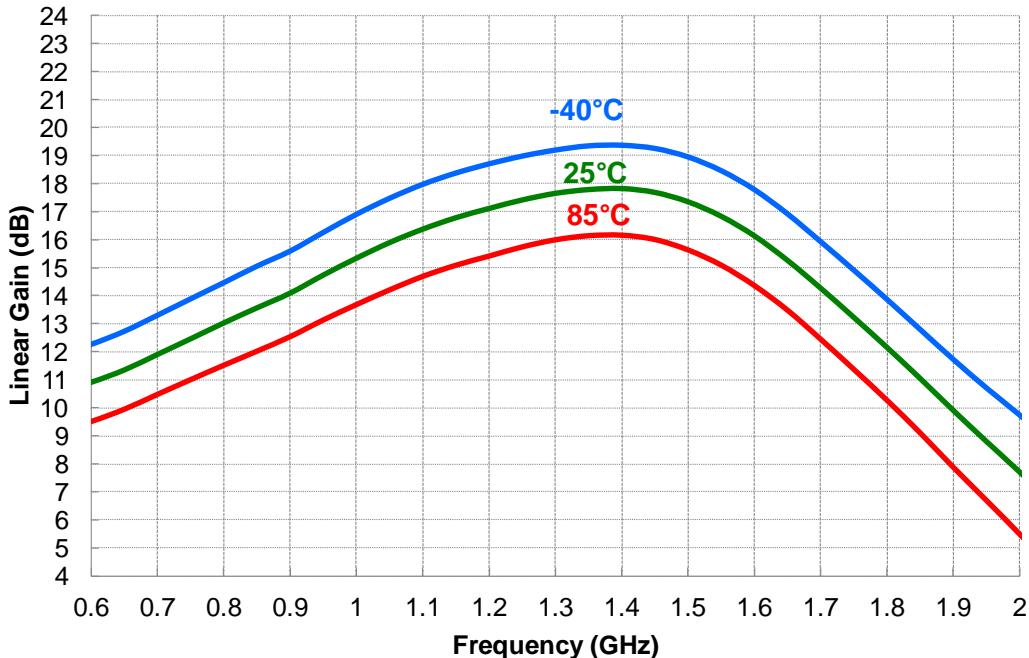
⁽¹⁾ Input RF and gate voltage are pulsed. Conditions are 1ms width, 10% duty cycle and 1μs offset between DC and RF pulse.

Typical Performance in Temperature (on evaluation board)

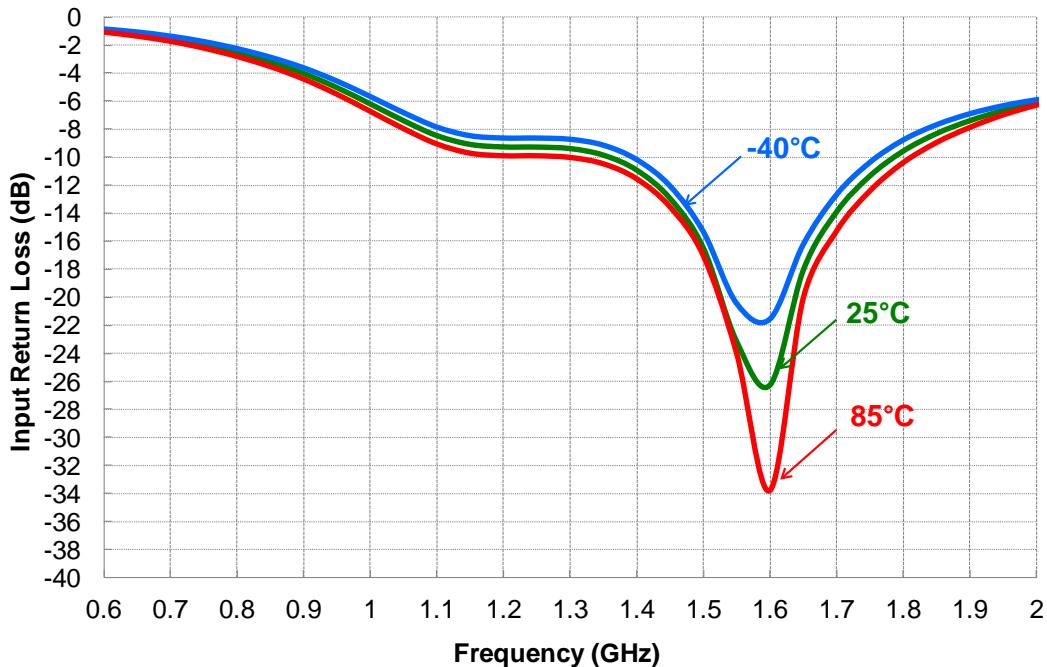
Calibration and measurements are performed on the connector access planes of the evaluation boards (ref 61501358).

Tamb.= -40°C, +25°C, +85°C, **pulsed mode**⁽¹⁾, V_{DS}=45V, I_{D_Q}=50mA (V_{GS} fixed @ +25°C)

Linear Gain versus temperature with ID_Q fixed @ +25°C (50mA)

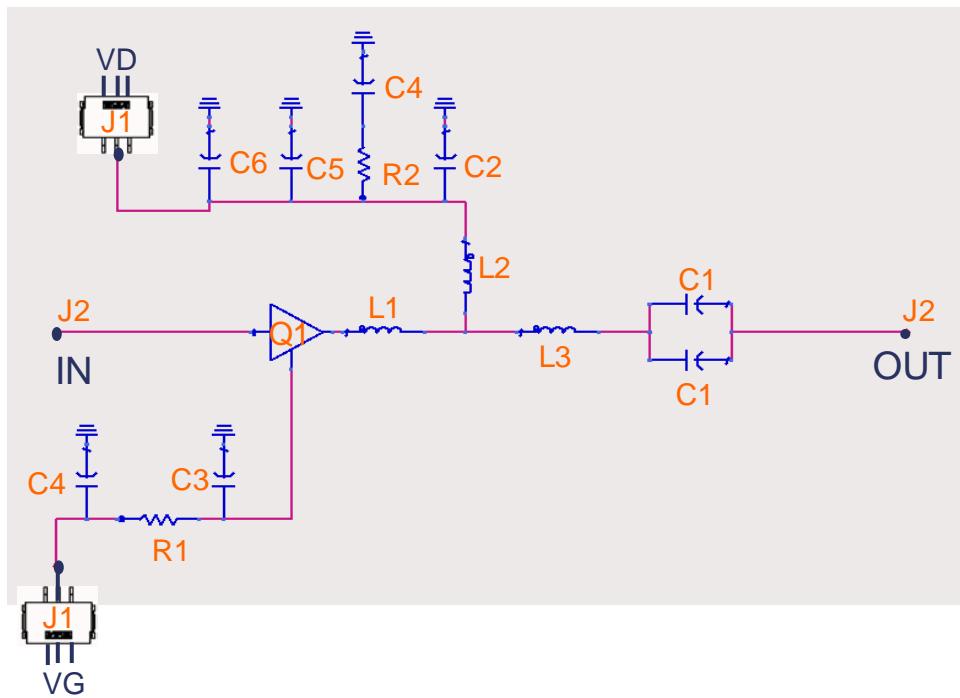


Input Return Loss versus temperature with ID_Q fixed @ +25°C (50mA)



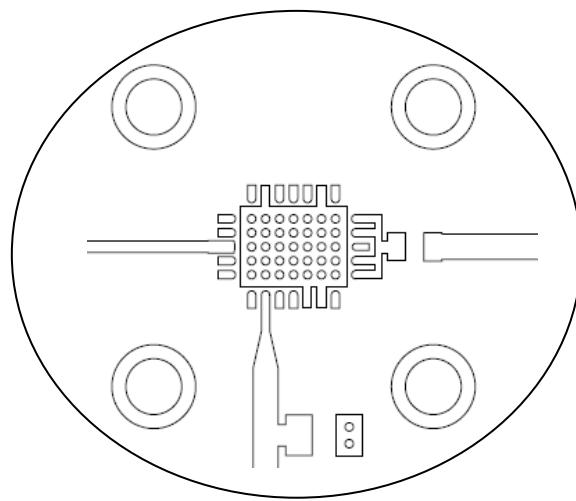
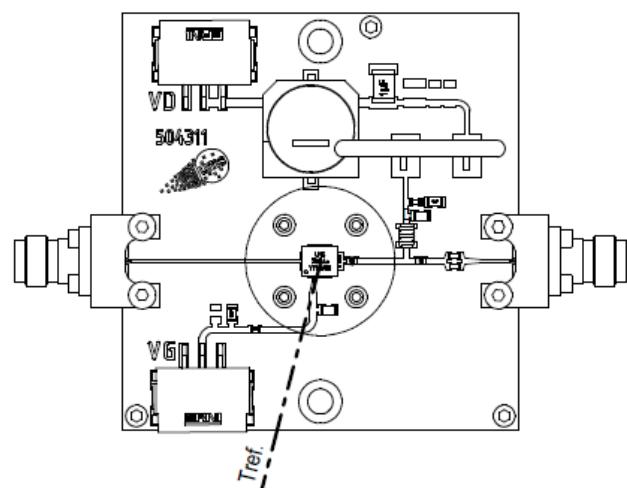
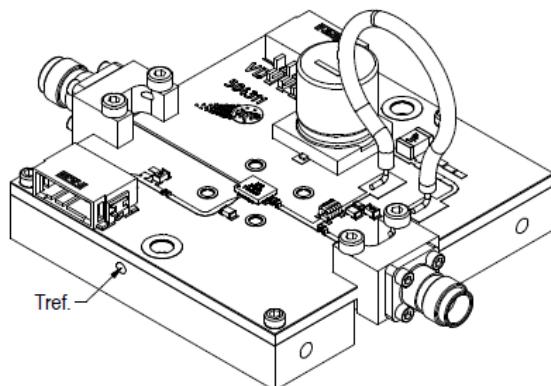
⁽¹⁾ CW Mode.

**Demonstration Amplifier Low Frequency Equivalent Schematic
(ref 61504312)**

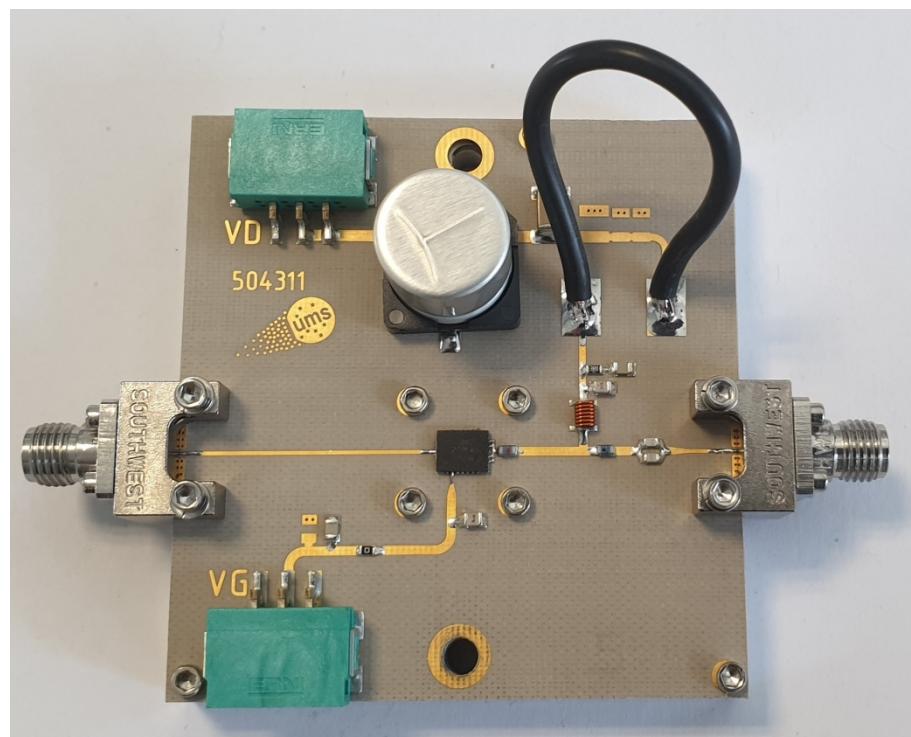


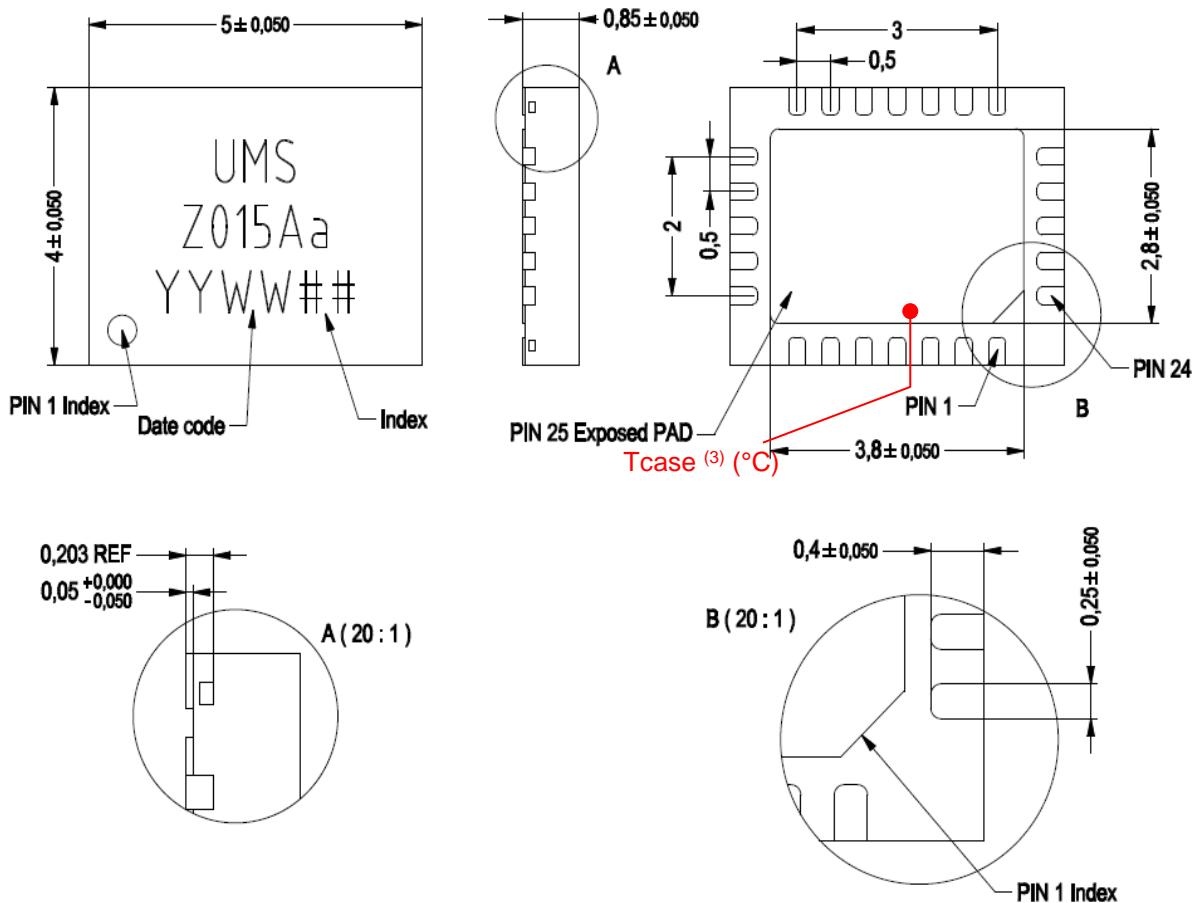
Demonstration Amplifier (ref 61504312) / Bill of Materials

Designator	Type	Value - Description	Qty
L1	Inductor for output pre-matching	3.9nH. +/- 5%. 0603	1
L2	Inductor	27nH. +/- 5.2%. 0908	1
L3	Inductor	1.6nH. +/- 5%. 0603	1
C1	Capacitor	4.7pF. +/- 0.25pF. 0603	2
C2	Capacitor	120pF. +/- 5%. 0805	1
C3	Capacitor	220pF. +/- 5%. 0805	1
C4	Capacitor	1nF. +/- 5%. 0805	2
C5	Capacitor	1μF. +/- 10%. 1810	1
C6	Capacitor	68μF. +/- 20%	1
R1	Jumper	Jumper 0 Ω. 0603	1
R2	Resistor	3Ω. +/- 1%. 0603	1
J1	Connector	SMD 3 contacts	2
J2	Connector	SMA	2
Q1	Driver	CHZ015AaQEG	1
-	PCB	RFP35. Er=3.5. h=203μm	-

Amplifier Demonstration Board (ref 61504312)

Amplifier Demonstration Board (ref 61504312)



Package outline ⁽¹⁾

Matt tin, Lead Free (Green)	1- Nc	9- OUT	17- Nc
Units : mm	2- DC	10- Nc	18- GND ⁽²⁾
From the standard : JEDEC MO-220 (VGHD)	3- Nc	11- OUT	19- Nc
	4- Nc	12- Nc	20- Nc
25- GND	5- GND ⁽²⁾	13- Nc	21- GND ⁽²⁾
	6- GND ⁽²⁾	14- GND ⁽²⁾	22- IN
	7- Nc	15- Nc	23- GND ⁽²⁾
	8- Nc	16- Nc	24- Nc

⁽¹⁾ The package outline drawing included in this data-sheet is given for indication. Refer to the application note AN0017 (<http://www.ums-gaas.com>) for exact package dimensions.

⁽²⁾ It is strongly recommended to ground all pins marked "Gnd" through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

⁽³⁾ The temperature is monitored at the package back-side interface (Tcase) as shown above.

Recommended package footprint

Refer to the application note AN0017 available at <http://www.ums-gaas.com> for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <http://www.ums-gaas.com>.

Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x5 package:

CHZ015AaQEG/XY

Stick: XY = 20

Tape & reel: XY = 21

Information furnished is believed to be accurate and reliable. However **United Monolithic Semiconductors S.A.S.** assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of **United Monolithic Semiconductors S.A.S.**. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. **United Monolithic Semiconductors S.A.S.** products are not authorised for use as critical components in life support devices or systems without express written approval from **United Monolithic Semiconductors S.A.S.**.