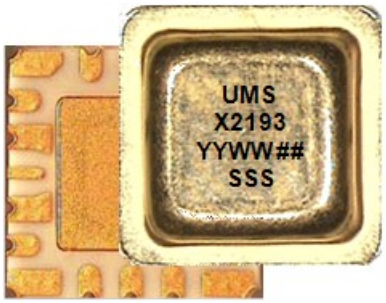
6.25-8.25GHz Frequency Multiplier

GaAs Monolithic Microwave IC in SMD leadless package

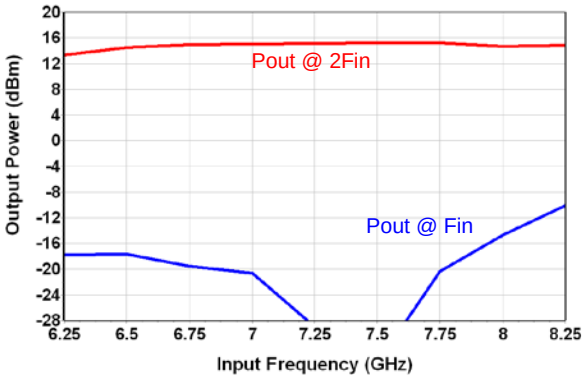
Description

The CHX2193-FAB is a 6.25-8.25GHz frequency doubler designed for a wide range of applications, from military to commercial communication systems.
It is proposed in leadless surface mount hermetic metal ceramic 6x6mm² package. The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is supplied in RoHS compliant SMD package.



Main Features

- Broadband performances: 6.25-8.25GHz
- 14dBm output power for 10dBm input power
- DC power consumption: 60mA @ 3.5V (with RF)
- 6x6mm² hermetic metal ceramic package



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
F_{in}	Input frequency range	6.25		8.25	GHz
F_{out}	Output frequency range	12.5		16.5	dB
P_{in}	Input power		10		dBm
P_{out}	Output power for 10dBm input power	10	14	16	dBm

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!

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Electrical Characteristics

Tamb.= +25°C, V_{g1} = -0.9V, V_{g2} adjusted for I_d = 60mA under RF, P_{in}=+10dBm

Symbol	Parameter	Min	Typ	Max	Unit
F_{in}	Input frequency range	6.25		8.25	GHz
F_{out}	Output frequency range	12.5		16.5	GHz
P_{in}	Input power		10		dBm
$Pout_{@2Fin}$	Output power	10	14	16	dBm
Rej_H1	Fundamental rejection		30		dBc
$VSWR_{in}$	Input VSWR		2.5:1		
$VSWR_{out}$	Output VSWR		2.5:1		
V_d	Drain bias voltage		3.5		
I_d	Bias current		60		mA

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation board description".
Performances are provided in the package reference planes.

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
V_d	Drain bias voltage	4	V
I_d	Drain bias current	150	mA
V_g	Gate bias voltage	-2 to +0.4	V
Tj	Junction temperature	175	°C
Pin	Input power	14	dBm

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Temperature Range

Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-50 to +150	°C

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad Nº	Parameter	Values	Unit
V_d	12	Drain bias voltage	+3.5	V
V_{g1}	14	Gate bias voltage 1	-0.9	V
V_{g2}	12	Gate bias voltage 2	-0.25 typ.	V

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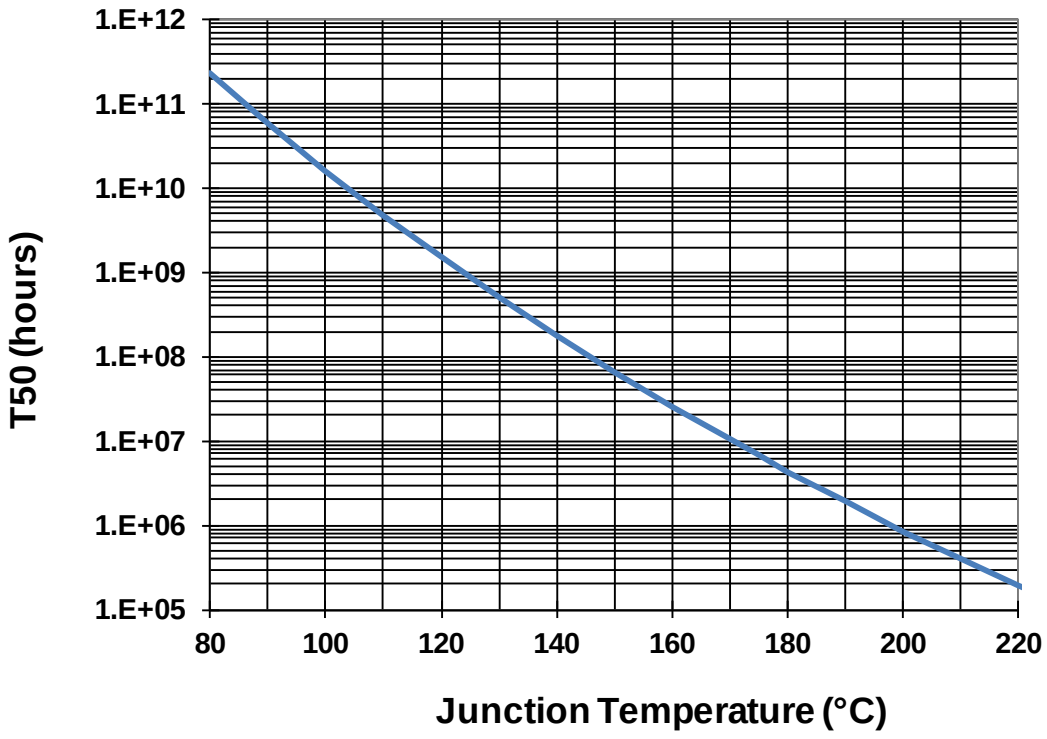
Device thermal performances

All the figures given in this section are obtained assuming that the packaged device is only cooled down by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tcase).
The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Absolute Maximum Ratings table.
So, the system PCB must be designed to comply with these requirements.

Parameter	Biasing conditions	Tjunction (°C)	R_{TH} (°C/W)	T50 (hours)
R_{TH} (1) Thermal Resistance (Junction to Case)	V_d = 3.5V, V_{g1} = -0.9V(2) Pin = 7dBm Pdiss = 186mW	125	214.5	9.0E+08
R_{TH} (1) Thermal Resistance (Junction to Case)	V_d = 3.5V, V_{g1} = -0.9V(2) Pin = 10dBm Pdiss = 190mW	120	185	1.5E+09
R_{TH} (1) Thermal Resistance (Junction to Case)	V_d = 3.3V, V_{g1} = -0.9V(2) Pin = 7dBm Pdiss = 180mW	122	206	1.5E+10
R_{TH} (1) Thermal Resistance (Junction to Case)	V_d = 3.3V, V_{g1} = -0.9V(2) Pin = 10dBm Pdiss = 181mW	117.5	179.5	2.0E+09

(1) Assuming 85°C Tcase
(2) V_{g2} set to get Idq = 60mA at 85°C Tcase



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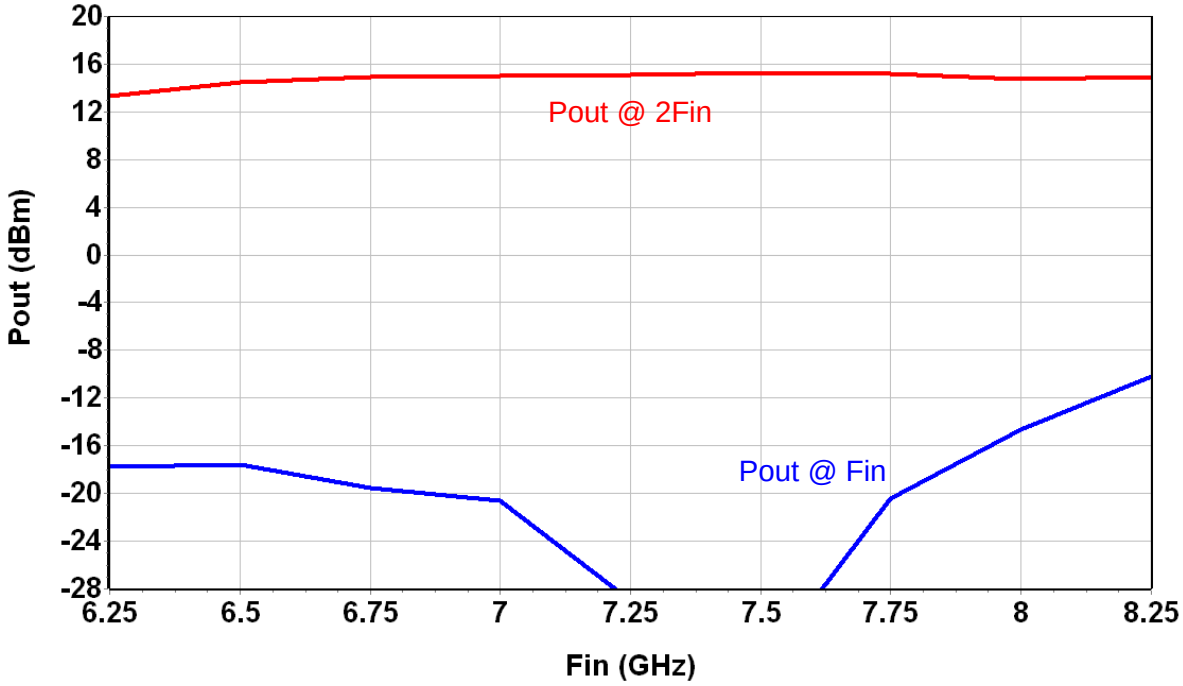
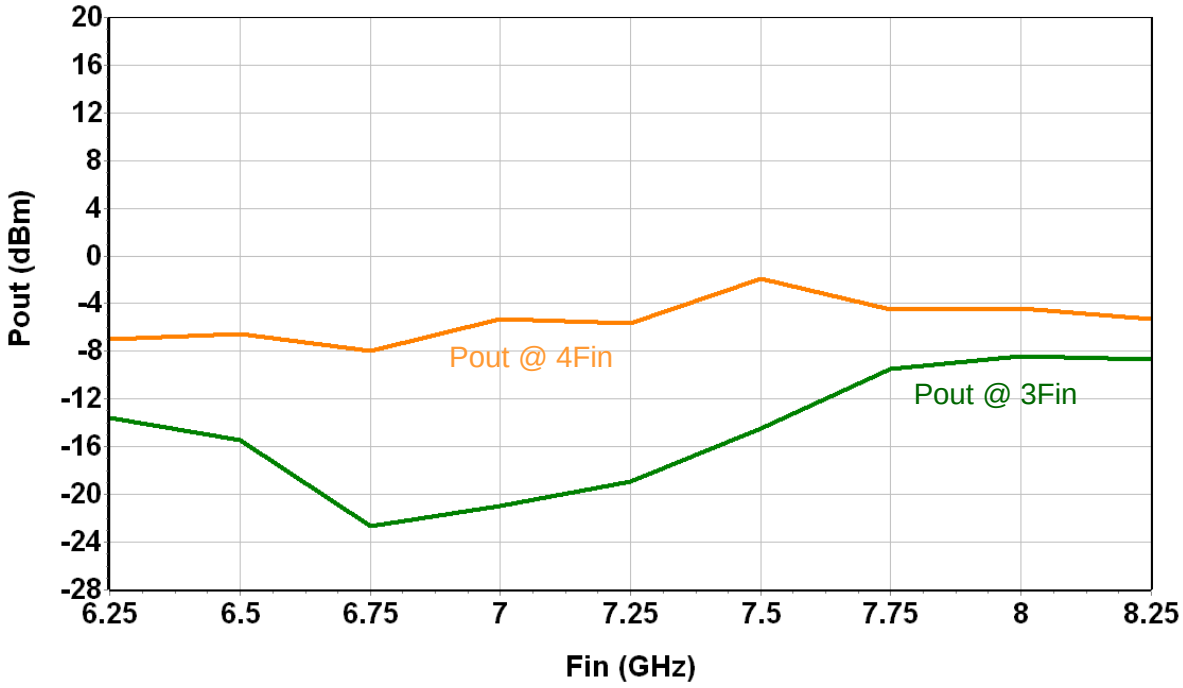
Typical Board Measurements

T_{case} = +25°C, V_d = +3.5V, V_{g1} = -0.9V, V_{g2} adjusted for I_d = 60mA under RF, P_{in}=+10dBm

Output Power @ F_{in} and $2F_{in}$ versus Input Frequency



Output Power @ $3F_{in}$ and $4F_{in}$ versus Input Frequency



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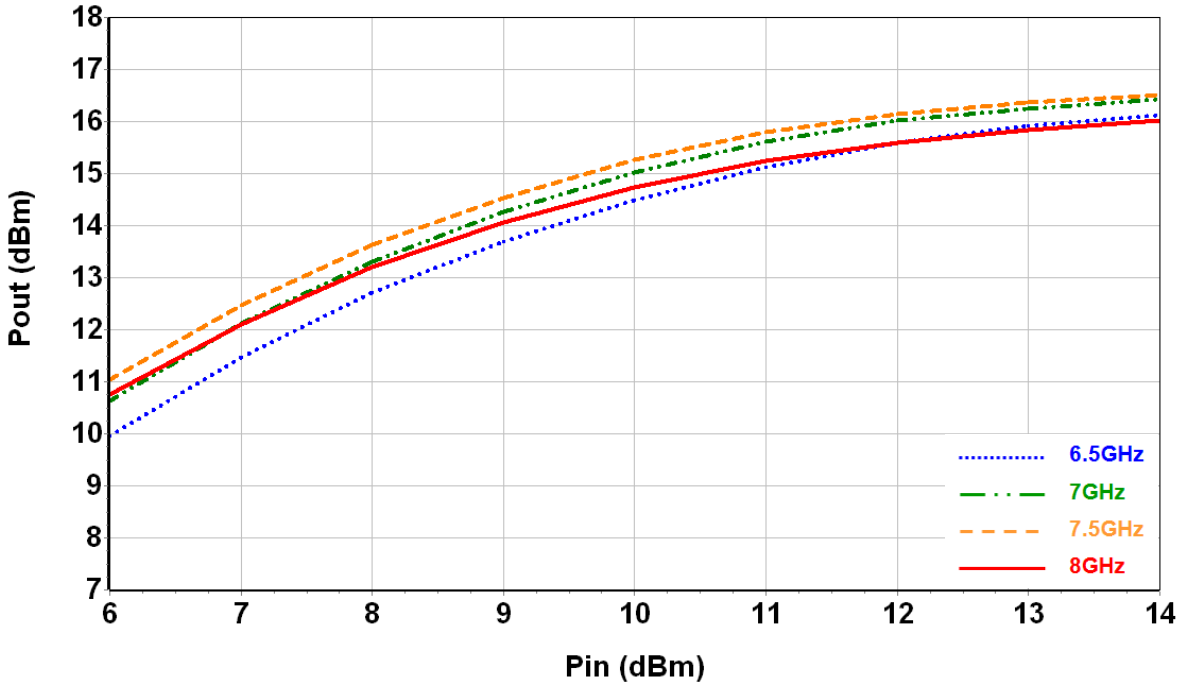
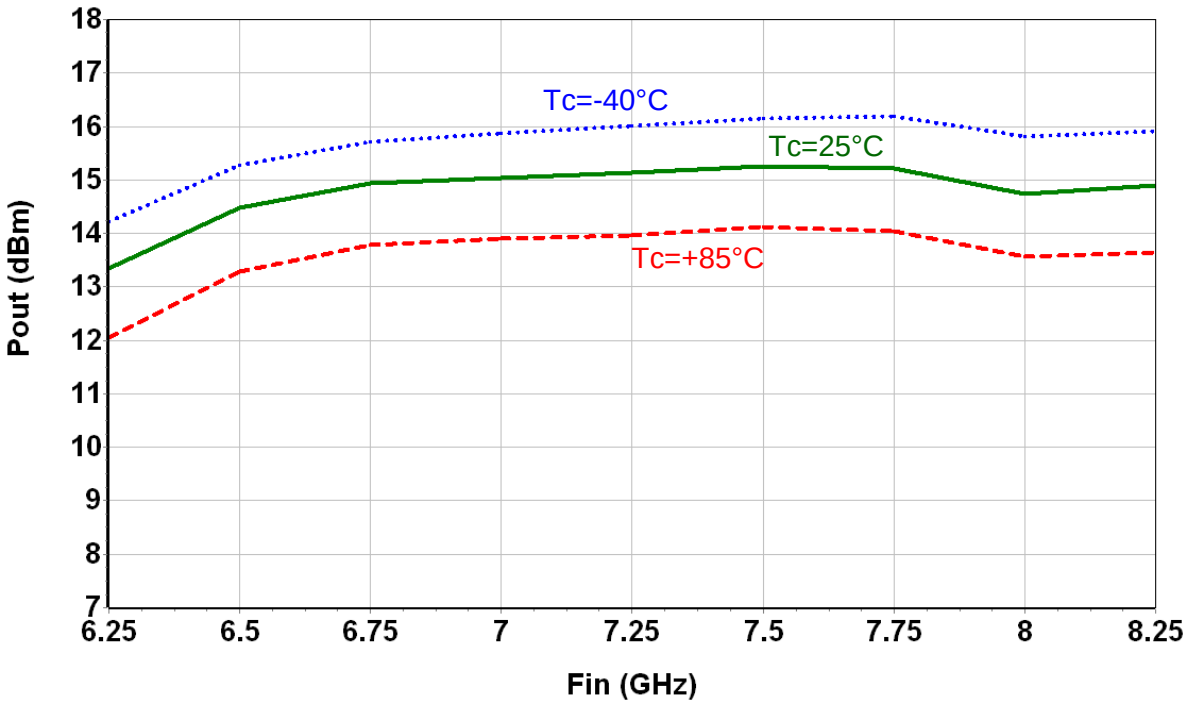
Typical Board Measurements

V_d = +3.5V, V_{g1} = -0.9V, V_{g2} adjusted for I_d = 60mA under RF

Output Power @ $2F_{in}$ versus Input Power
(F_{in} = 6.5GHz / 7GHz / 7.5GHz / 8 GHz; T_{case} = +25°C)



Output Power @ $2F_{in}$ versus Input Frequency
(T_{case} = -40°C / 25°C / 85°C; P_{in}=+10dBm)



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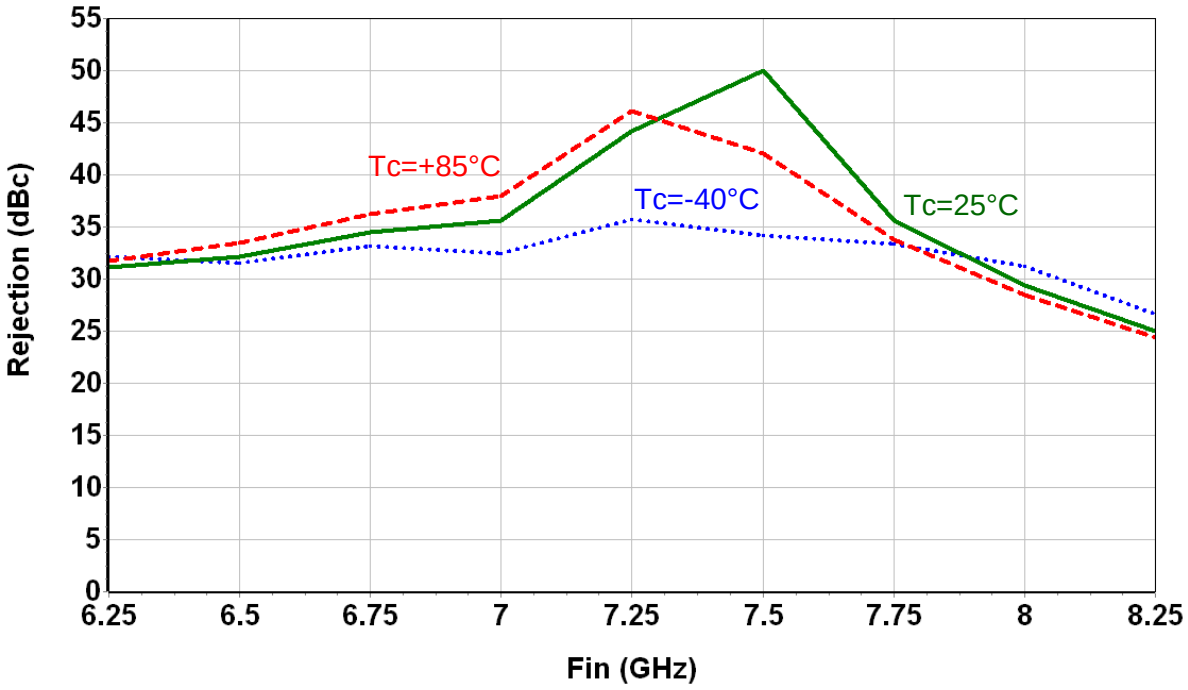
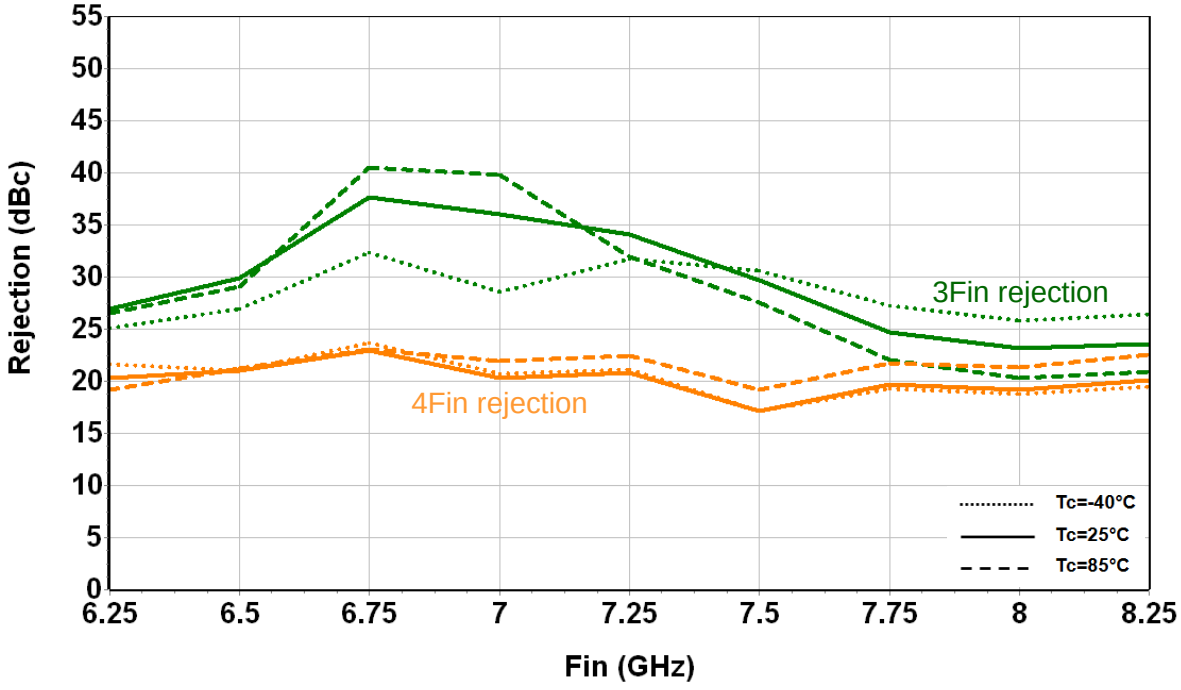
Typical Board Measurements

V_d = +3.5V, V_{g1} = -0.9V, V_{g2} adjusted for I_d = 60mA under RF, P_{in}=+10dBm

F_{in} rejection versus Input Frequency
(T_{case} = -40°C / 25°C / 85°C)



$3F_{in}$ and $4F_{in}$ rejection versus Input Frequency
(T_{case} = -40°C / 25°C / 85°C)



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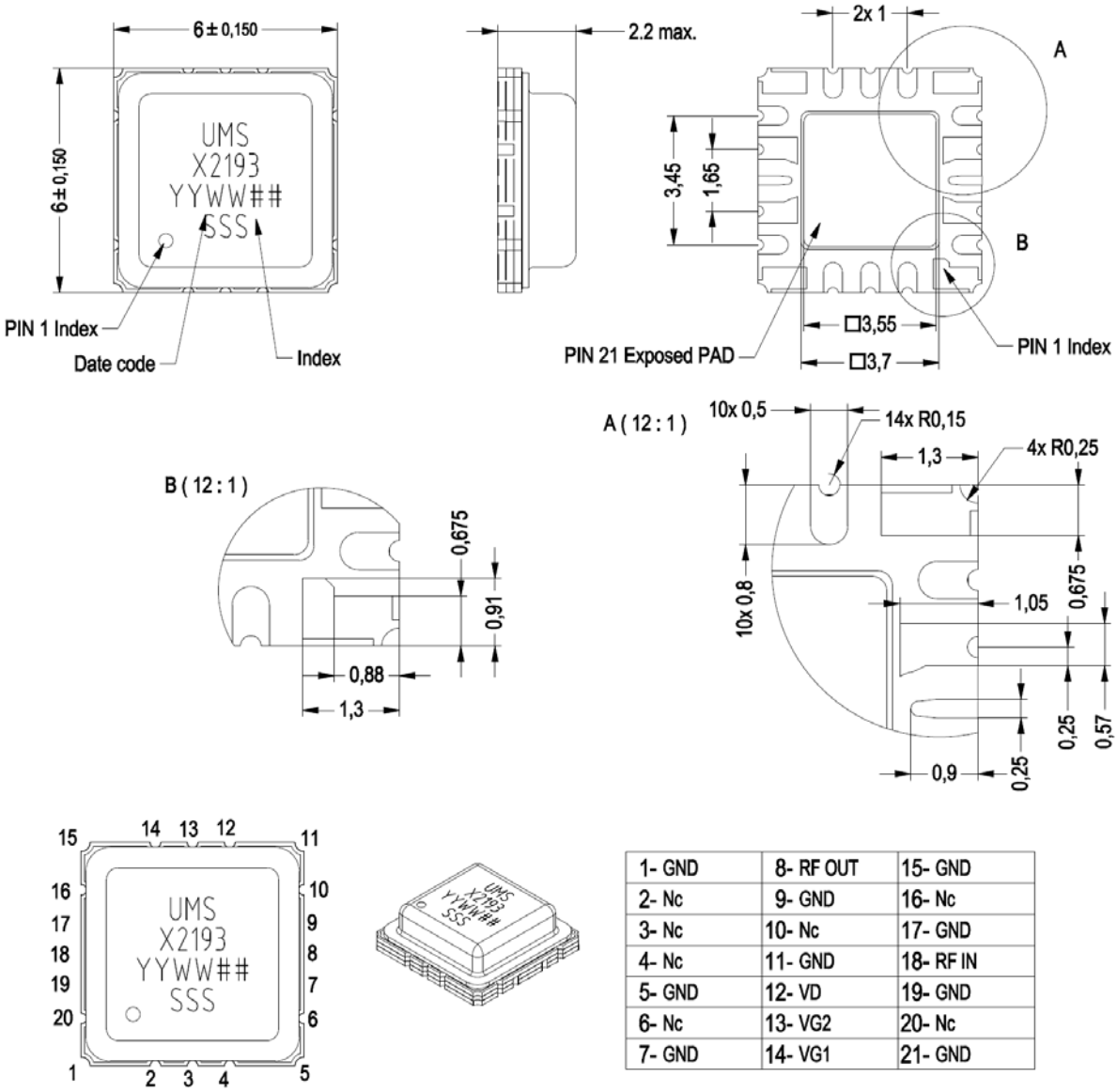
Package outline (1)



1- GND	8- RF OUT	15- GND
2- Nc	9- GND	16- Nc
3- Nc	10- Nc	17- GND
4- Nc	11- GND	18- RF IN
5- GND	12- VD	19- GND
6- Nc	13- VG2	20- Nc
7- GND	14- VG1	21- GND

Dimensions in mm

It is strongly recommended to ground all pins marked “GND” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

(1) The package outline drawing included in this data-sheet is given for indication. Refer to the application note AN0024 (http://www.ums-gaas.com) for exact package dimensions.

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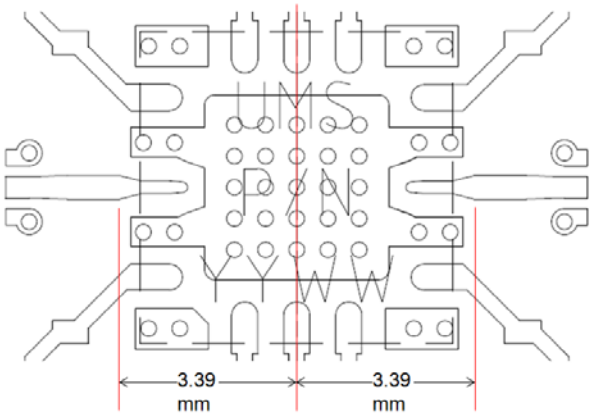
Definition of the Power measurements reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.39mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation board description".



Package Information

Parameter	Value
Package body material	RoHS-compliant
Lead finish	Gold
Hermetic sealing (fine leak compliant Mil-Std-883 Method 1014.10 Condition A4, tracer gas He at 1atm)	$1x10^{-8}$ ccHe/s/atm

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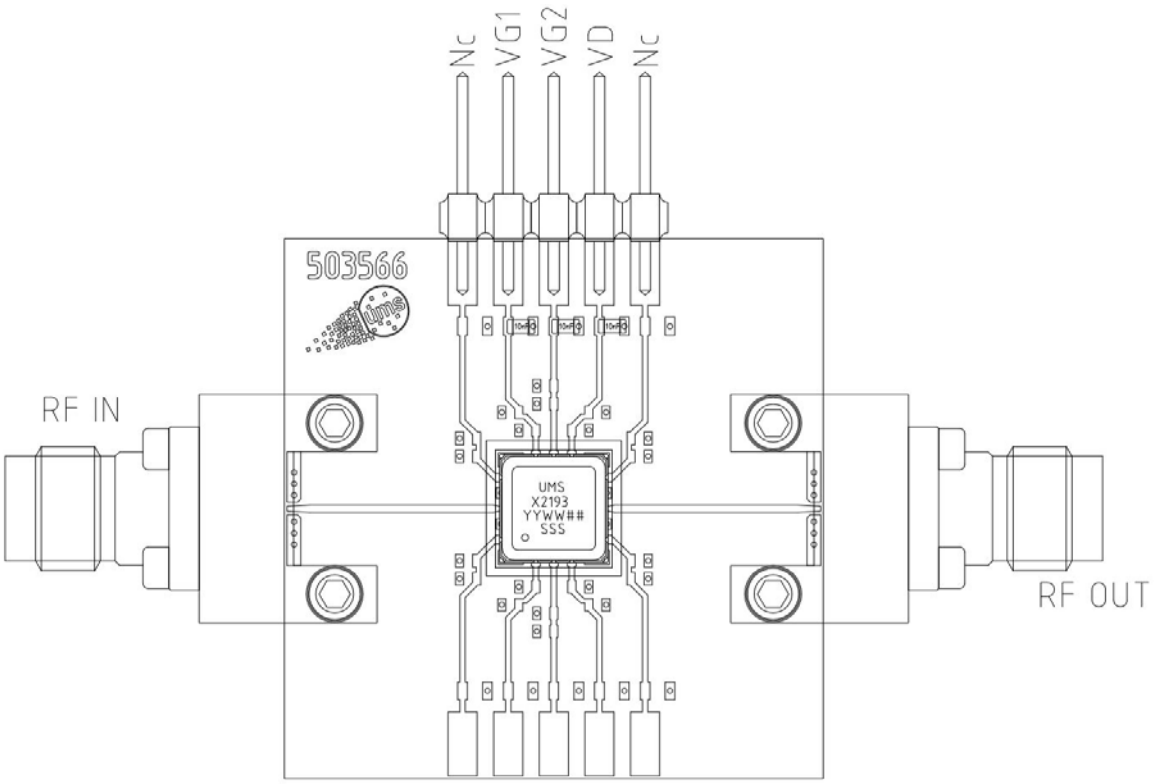
Evaluation board description

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF are recommended on each DC access (Vg1 / Vg2 / Vd).



Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.

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Notes

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SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017 available at http://www.ums-gaas.com.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

FAB Type Surface Mount Hermetic Package

Refer to the application note AN0024 available at http://www.ums-gaas.com for assembly recommendations for the UMS FAB package products.

Ordering Information

Leadless hermetic package:	CHX2193-FAB/XY Waffle pack: XY = 24

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