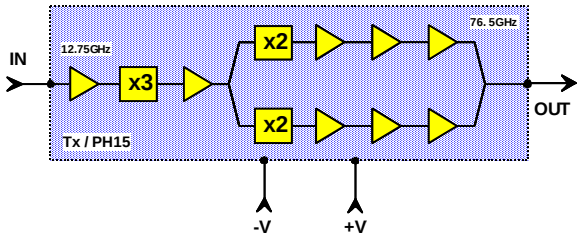
W-band Multifunction: Multiplier / MPA

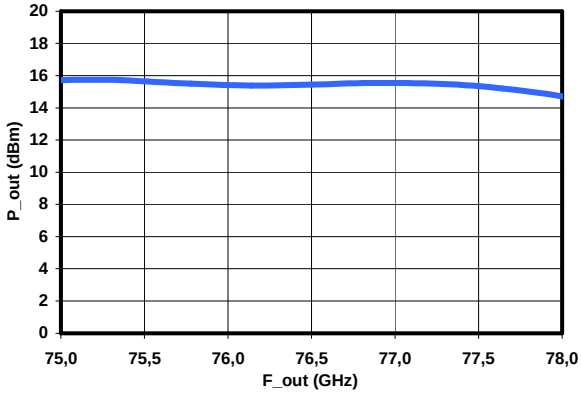
GaAs Monolithic Microwave IC

Description

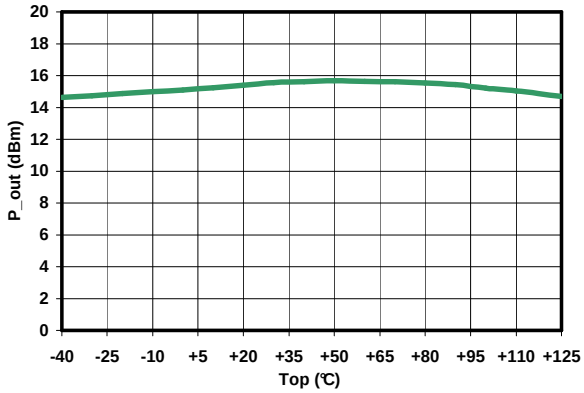
The CHU3377 is a W-band monolithic multifunction, which integrates an input buffer, a frequency multiplier by three followed by an amplifier splitter and two W-band chains in parallel combined at the output. Each W-band chain includes a frequency multiplier and a medium power amplifier. The frequency multipliers are based on active transistors and allow operation at low input level with reduced power consumption.
All the active devices are internally self-biased to ease bias configuration. This chip is compatible with automatic equipment for assembly.
The circuit is manufactured with the pHEMT process: 0.15µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is available in chip form.



W-band multifunction block-diagram



Typical P_out (F_out) measurement



Typical P_out (Top) measurement

Main Features

- -40°C to +125°C temperature range
- Low temperature dependence
- Low AM noise
- High output power
- Wide operating frequency range
- Low input power
- On-chip self biasing
- Very simple bias configuration
- Low DC power consumption
- Automatic assembly oriented
- BCB layer protection
- Chip size: 3.86 x 1.62 x 0.1mm

Main Characteristics

Tamb = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
F_in	Input frequency	12.67		12.83	GHz
P_in	Input power	0		8	dBm
F_out	Output frequency	76		77	GHz
P_out	Output power		15		dBm

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Electrical Characteristics

Full operating temperature range, used according to section “Typical assembly and bias configuration”

Symbol	Parameter (1)	Min	Typ	Max	Unit
F_in	Input frequency	12.67		12.83	GHz
F_out	Output frequency	76		77	GHz
P_in	Input power at IN port	0	4	8	dBm
VSWR_in	IN port VSWR on 50Ω load		1.5:1	2.5:1	
P_out	Output power at OUT port on load VSWR ≤1.5:1	12	15	17	dBm
VSWR_out	OUT port VSWR on 50Ω load		1.5:1	2.5:1	
An	Amplitude noise @ 1kHz (SSB)		-135	-125	dBc/Hz
	@ 10kHz (SSB)		-142	-137	
	@ 100kHz (SSB)		-151	-144	
	@ 200kHz (SSB)		-153	-146	
	≥ 1MHz (SSB)		≤ -155	-150	
Hn_p	Harmonics output power (@ k*6.375 GHz)				dBm
	@ 6.375 GHz to 51 GHz		-50	-40	
	@ 57.375 GHz to 102 GHz		-35	-25	
NHn_p	Non harmonics output power			-50	dBm
+V	Positive supply voltage	+4.4	+4.5	+4.6	V
+I	Positive supply current		210	275	mA
-V	Negative supply voltage	-4.7	-4.5	-4.3	V
-I	Negative supply current		11	18	mA
Top	Operating temperature range (2)	-40		+125	℃

(1) All the parameters are given in the following conditions:
- OUT Port: 50Ω reference plan at ≤200µm (≤0.15nH) bonding length from OUT pad.

(2) Chip backside metal temperature.

Absolute Maximum Ratings (2)

Symbol	Parameter	Values	Unit
P_in	Input power	9	dBm
+V	Positive supply voltage	+5	V
-V	Negative supply voltage	-5	V
+I	Positive supply current	325	mA
-I	Negative supply current	25	mA
Tstg	Storage temperature range	-55 to +150	℃

(2) Operation of this device above anyone of these parameters may cause permanent damage.

CAUTION:

- ☞ Positive supply voltage must not be applied without negative supply voltage.
- ☞ ESD Protections: Electrostatic discharge sensitive device observe handling precautions!

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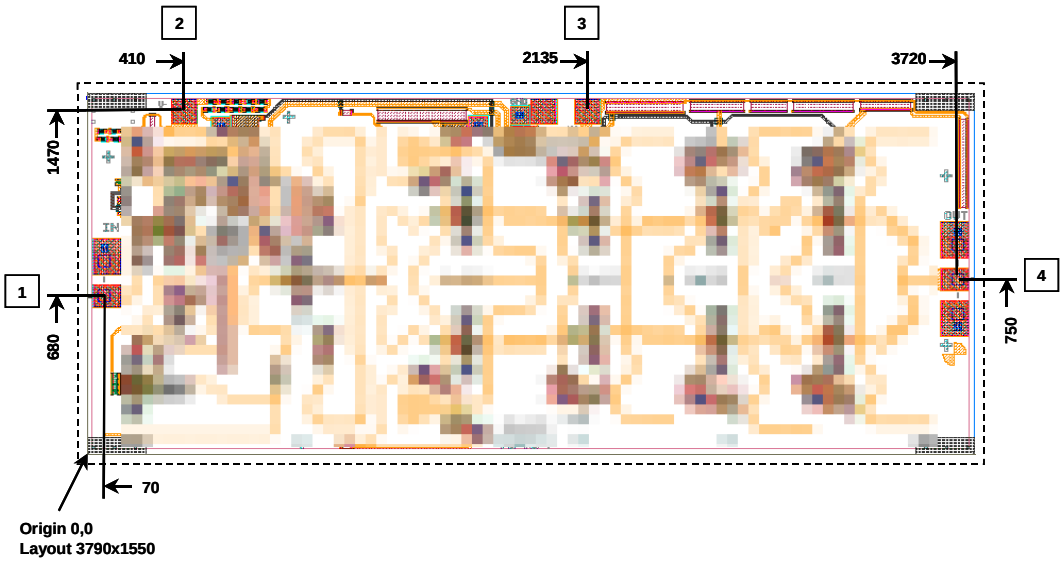
Chip Mechanical Data and Pin References



Unit = µm
External chip size (layout size + dicing streets) = 3860 x 1620 ± 35
Chip thickness = 100 +/- 10
RF Pads (1, 5) = 90 x 110 (BCB opening)
DC/IF Pads = 100 x 100 (BCB opening)

Pin number	Pin name	Description
1	**IN**	RF Input port
2	**-V**	Negative supply voltage port
3	**+V**	Positive supply voltage port
4	**OUT**	RF Output port

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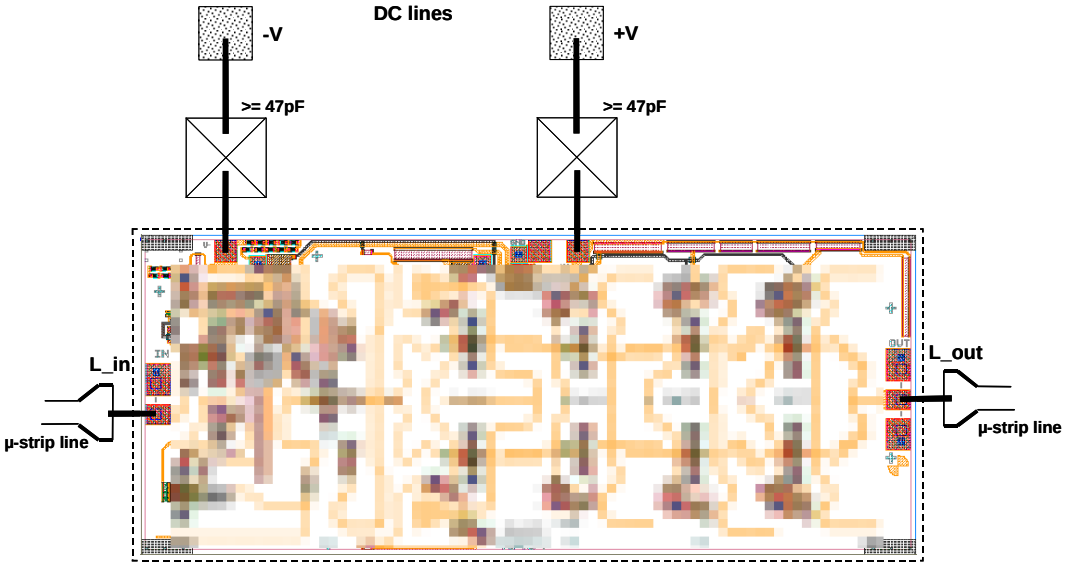
Typical Assembly and Bias Configuration



This drawing shows an example of assembly and bias configuration. All the transistors are internally self biased. An external chip capacitor of at least 47pF is necessary for the positive and negative supply voltages.
For the RF pads the equivalent wire bonding inductance (diameter=25µm) have to be according to the following recommendation.

Pin name	Equivalent inductance	Wire length (1)
IN	L_in ≤ 0.3 nH	≤ 0.4 mm
OUT	L_out ≤ 0.15 nH **(2)**	0.2 mm **(2)**

(1) This value is the total length including the necessary loop from pad to pad.
(2) For longer wire length or higher inductance, an external compensation is required to match 50Ω between OUT Pin and 0.15nH wire inductance plan. (For example with a matching network on the substrate)

☞ Chip backside must be RF grounded.

Ordering Information

Chip form : CHU3377-98F/00

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