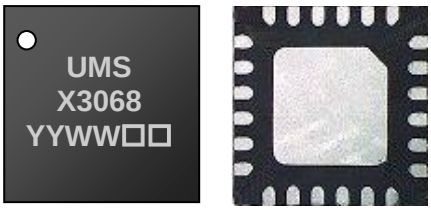
15-30GHz Frequency Multiplier

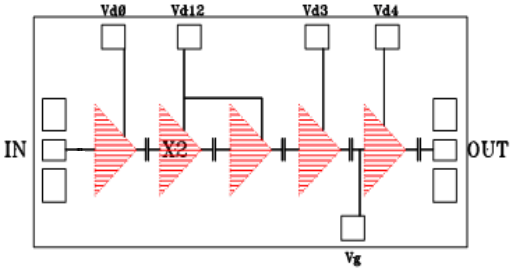
GaAs Monolithic Microwave IC in SMD leadless package

Description

The CHX3068-QDG is a Ka-band frequency multiplier monolithic integrated circuit. Typical applications are for telecommunication such as DVB-RCS.

The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is supplied in lead-free SMD package





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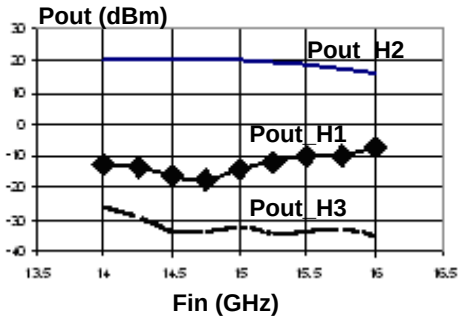
Main Features

- 14 to 15 GHz input frequency
- Input and output integrated buffers
- 20dBm output power
- Low input power: 0 to 5dBm
- DC bias 270mA @ 4V
- 24L-QFN4X4 SMD package
- MSL 1



Main Characteristics

Tamb. = 25°C, Vd = 4.V typical consumption ≈270mA

Symbol	Parameter	Min	Typ	Max	Unit
Fin	Input frequency range	14		15	GHz
Fout	Output frequency range	28		30	GHz
Pin	Input power	0		5	dBm
Pout	Output power		20		dBm

ESD Protections: Electrostatic discharge sensitive device observe handling precautions!

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Electrical Characteristics

Tamb = +25°C, Vd0=Vd1,2=Vd3=Vd4= 4.V Consumption(Id0+Id1,2+Id3+Id4) ≈ 270mA (1)

Symbol	Parameter	Min	Typ	Max	Unit
Fin	Input frequency range	14		15	GHz
Fout	Output frequency range	28		30	GHz
Pin	Input power	0		5	dBm
Pout_H2	Output power for +2 dBm input power		20		dBm
Rej_H1	Fundamental rejection for +2dBm input power		30		dBc
Rej_H3	Third harmonic rejection for +2dBm input power		50		dBc
VSWRin	Input VSWR		2.0:1		
VSWRout	Output VSWR		2.0:1		
Vd	Drain voltage supply		4	4.3	V
Vg	Gate voltage supply (1)		-1.8		V
Id	Bias current (with RF)		270		mA

(1) Adjust Vg to achieve Id4=115 mA

(These values are representative of onboard measurements as defined on the drawing at page 6)

Absolute Maximum Ratings (1)

Tamb = +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4.5	V
Id	Drain bias current	330	mA
Pin	Maximum input power	+8	dBm
Tjmax	Maximum Junction Temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage or reduce MTTF

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Device thermal performances:

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tcase) as shown below.
The system maximum temperature must be adjusted in order to guarantee that Tcase remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

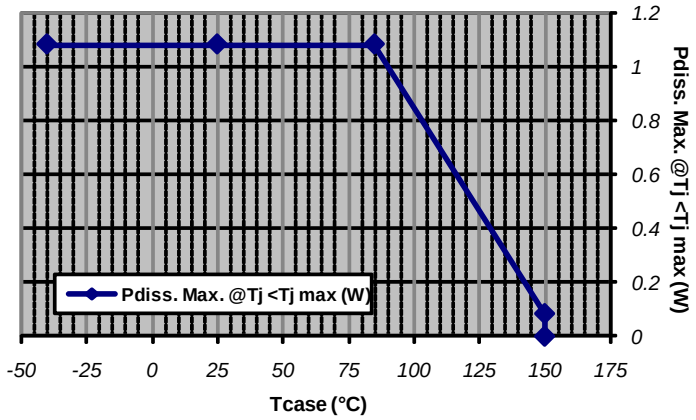
A derating must be applied on the dissipated power if the case temperature (Tcase) can not be maintained below the maximum temperature specified in order to guarantee the nominal device life time (MTTF) (see the curve Pdiss. Max).

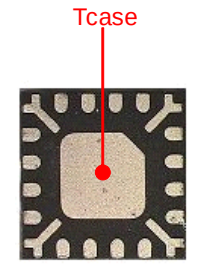
DEVICE THERMAL SPECIFICATION : CHX3068-QDG			
Recommended max. junction temperature (Tj max)	:	155	°C
Junction temperature absolute maximum rating	:	175	°C
Max. continuous dissipated power (Pdiss. Max.)	:	1.1	W
=> Pdiss. Max. derating above Tcase(1)= 85 °C	:	15	mW/°C
Junction-Case thermal resistance (Rth J-C)(2)	:	<65	°C/W
Minimum Tcase operating temperature(3)	:	-40	°C
Maximum Tcase operating temperature(3)	:	85	°C
Minimum storage temperature	:	-55	°C
Maximum storage temperature	:	150	°C

(1) Derating at junction temperature constant = Tj max

*(2) Rth J-C is calculated for a worst case where the **hottest junction** of the MMIC is considered.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example: QFN 16L 3x3
Location of temeprature reference point (Tcase) on package's bottom side

6.0

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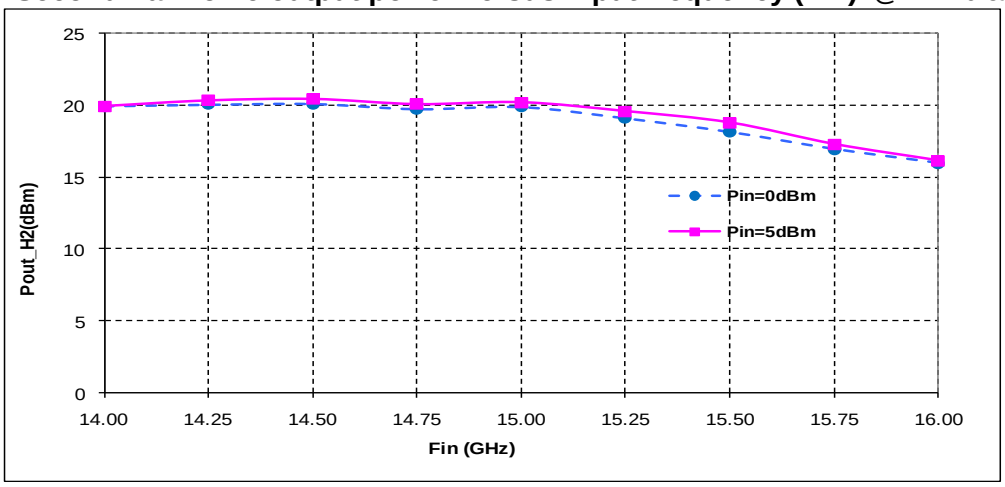
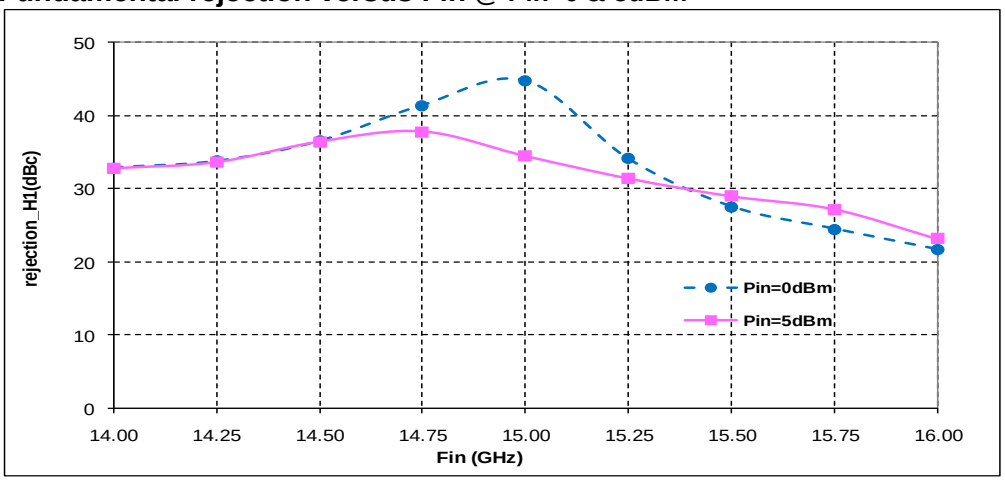
Typical PCB Measured Performances

Tamb=+25°C, Vd0=Vd1,2=Vd3=Vd4=4V Vg for Id4=115mA (≈-1.8V)

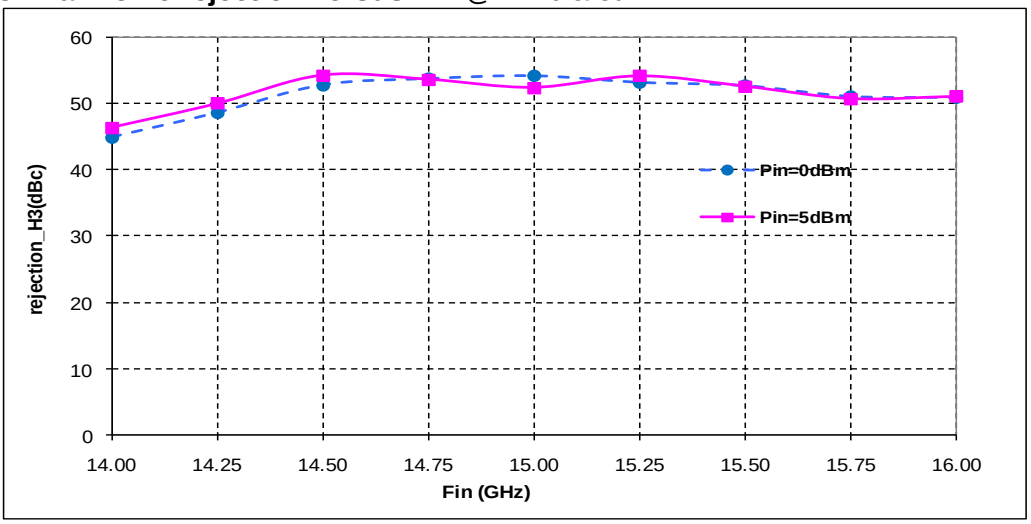
Second harmonic output power versus input frequency (Fin) @ Pin=0 & 5dBm



Fundamental rejection versus Fin @ Pin=0 & 5dBm



3rd harmonic rejection versus Fin @Pin=0 & 5dBm



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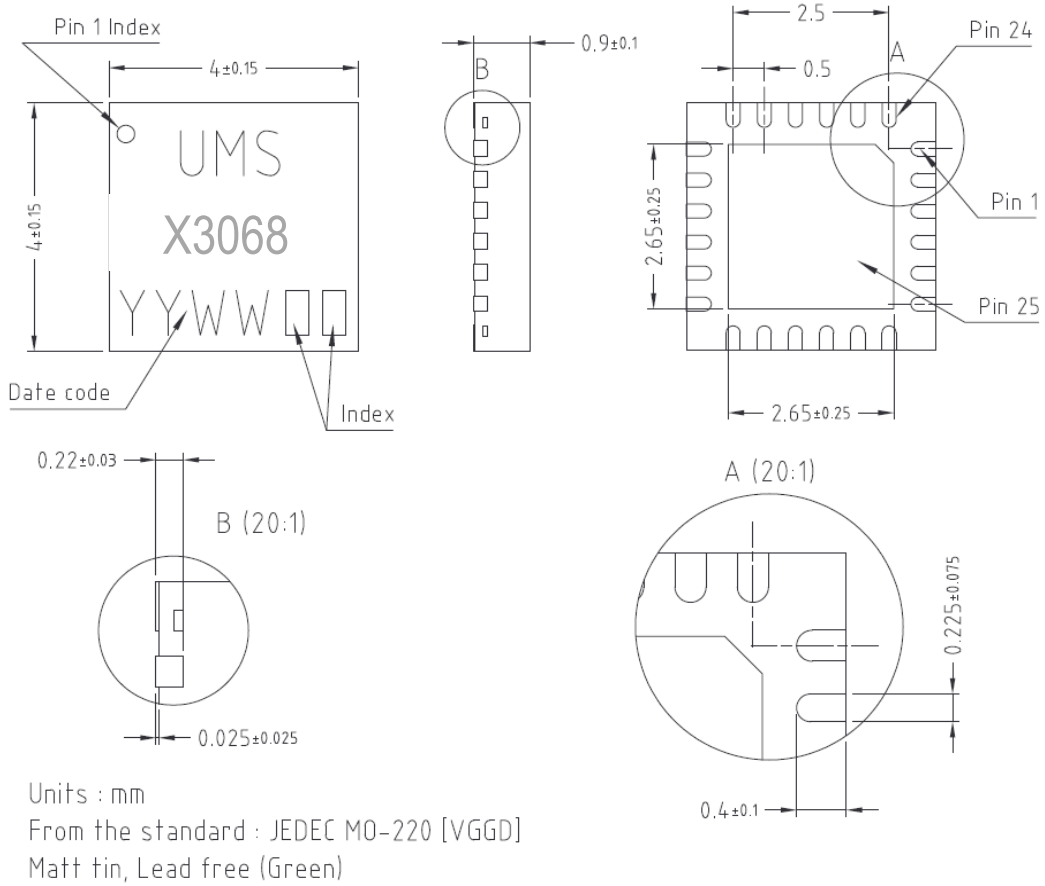
Package outline [(1)]:



Matt tin, Lead Free	(Green)	1-	NC	13-	NC
Units	mm	2-	NC	14-	GND
From the standard	JEDEC MO-220	3-	GND	15-	RF OUT
	(VGGD)	4-	RF IN	16-	GND
25	GND	5-	GND	17-	NC
		6-	NC	18-	NC
		7-	NC	19-	Vd4
		8-	NC	20-	NC
		9-	NC	21-	Vd3
		10-	Vg	22-	Vd1, 2
		11-	NC	23-	Vd0
		12-	NC	24-	NC

[(1)]The package outline drawing included to this data-sheet is given for indication. Refere to the application note AN0017 available at http://www.ums-gaas.com for exact package dimensions.

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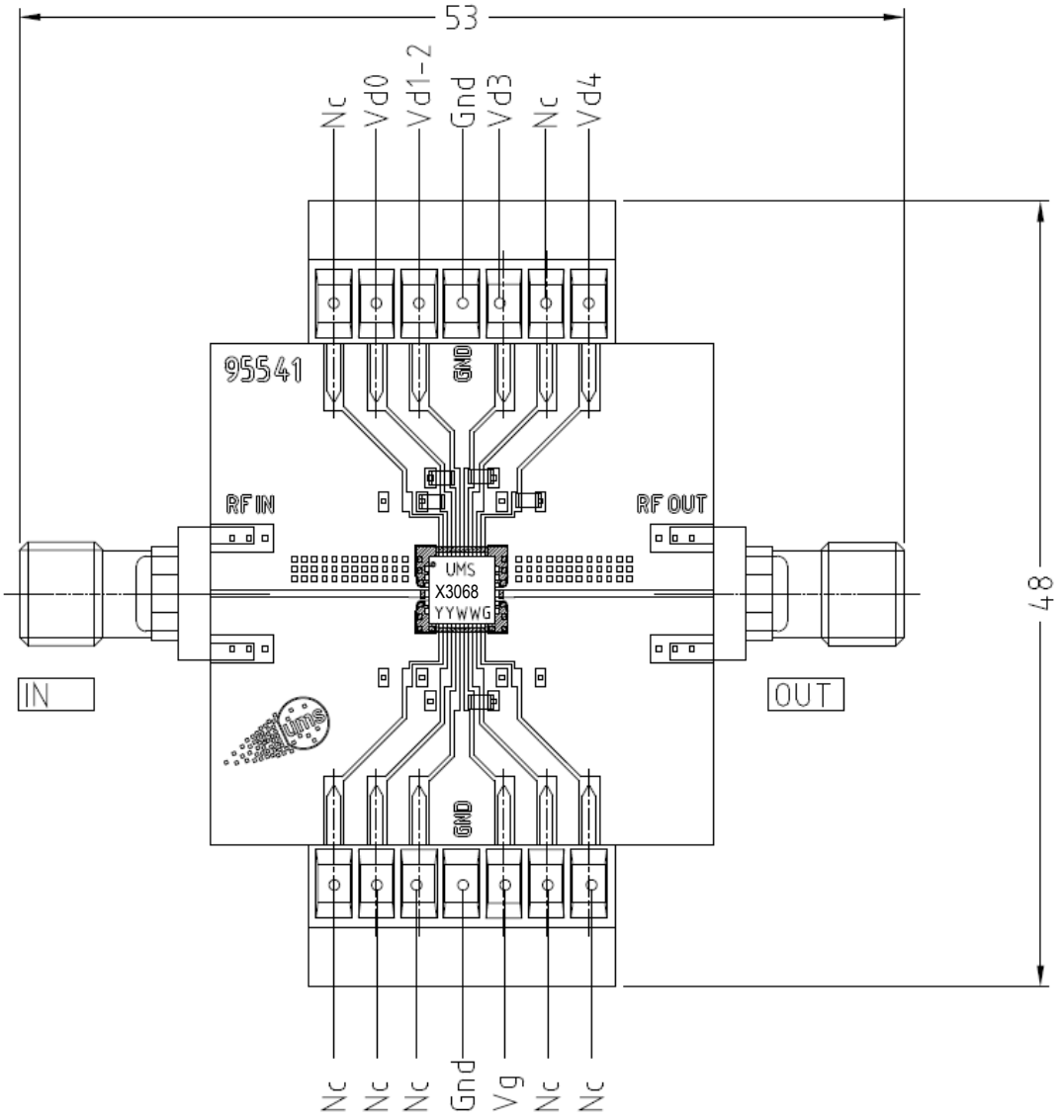
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip access to the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.
- See application note AN0017 for details.



Capacitors 10nF ± 10%

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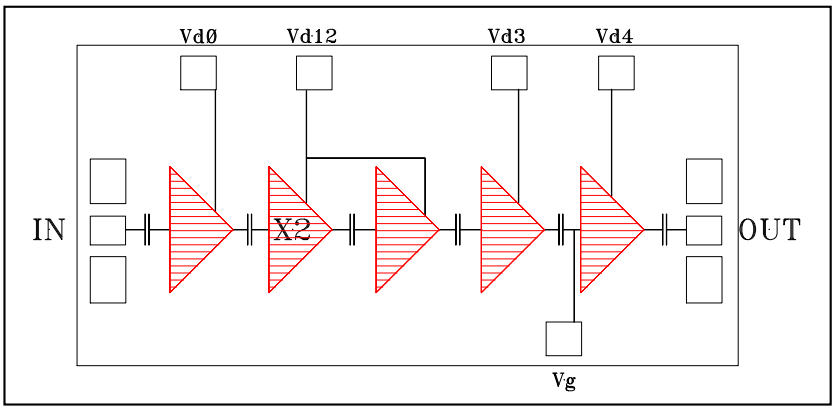
Chip schematic and biasing



Biasing :

-Vd0=Vd1,2=Vd3=Vd4=4V
-Adjust Vg to achieve Id4=115mA typically Vg=-1.8V)

Id0+Id1,2+Id3+Id4 ≈270mA

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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

Refer to the application note AN0019 available at http://www.ums-gaas.com for environmental data on UMS package products.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x4 RoHS compliant package : CHX3068-QDG/XY
Stick: XY = 20 Tape & reel: XY = 21

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