United Monolithic Semiconductors

CHV1203-FAB

Low Phase Noise S band HBT VCO

GaAs Monolithic Microwave IC in SMD leadless package

Description

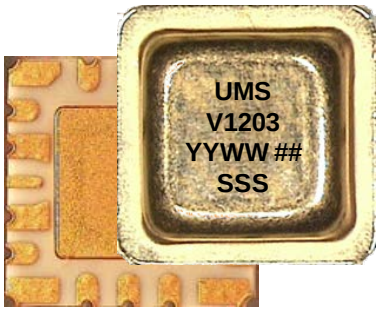
The CHV1203-FAB is a low phase noise S-band HBT Voltage Controlled Oscillator integrating negative resistor, varactors and buffer amplifiers. It provides an excellent phase noise of 108dBc/Hz at 100kHz offset.

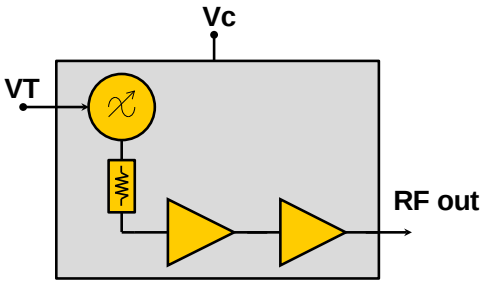
It is designed for a wide range of applications, from space to commercial communication systems.

The circuit is fully integrated on InGaP HBT process: 2µm emitter length, via holes through the substrate and high Q passive elements.

It is available in leadless surface mount hermetic metal ceramic 6x6mm² package.

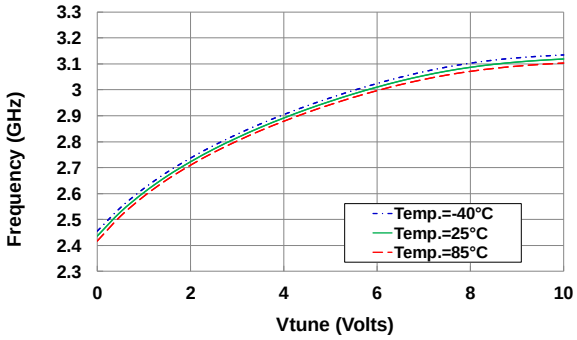
It is supplied in RoHS compliant SMD package.





Main Features

- S-band VCO + S buffers
- Fully integrated VCO
  (no need for external resonator)
- Low phase noise
- High frequency stability
- On chip self-biased devices
- 6x6mm² hermetic metal ceramic package



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
F_out	Output frequency range on RF_out port	2.6		3	GHz
P_out	Output power on RF_out port		8		dBm
PN_100	SSB Phase Noise @ F_out @ 100kHz offset		108		dBc/Hz

United Monolithic Semiconductors S.A.S.
Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

Electrical Characteristics

Tamb.= +25°C, Vd = +3V

Symbol	Parameter	Min	Typ	Max	Unit
F_out	Output frequency range	2.6		3	GHz
V_Tune	Voltage Tuning range	0		10	V
	Tuning sensitivity	40		110	MHz/V
	Frequency drift rate		0.3		MHz/°C
H1	Harmonics ½ F_out rejection		43		dBc
H3	Harmonics 3/2 F_out rejection		35		dBc
H4	Harmonics 2xF_out rejection		35		dBc
PN_10	SSB Phase Noise given @ F_out @ 10 kHz		-85		dBc/Hz
PN_100	SSB Phase Noise given @ F_out @ 100 kHz		-108		dBc/Hz
	Pulling into 2:1 VSWR for all phases		0.1		MHz
	Pushing vs Vc		14		MHz/V
P_out	Output Power on RF_out port		8		dBm
	Output power variation vs Tuning Voltage		0.8		dB
Vc	Positive supply voltage		3	3.5	V
I_Vc	Positive supply current		50		mA

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board".

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
VT	Tuning voltage	15	V
Vd	Drain bias voltage	4	V
Id	Drain bias current	100	mA
Tj	Junction temperature	175	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Temperature Range

Ta	Operating temperature range	-50 to +125	°C
Tstg	Storage temperature range	-50 to +150	°C

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad Nº	Parameter	Values	Unit
Vc	VC	Positive voltage supply	3	V
VT	VT	Tuning Voltage	0 to 10	V

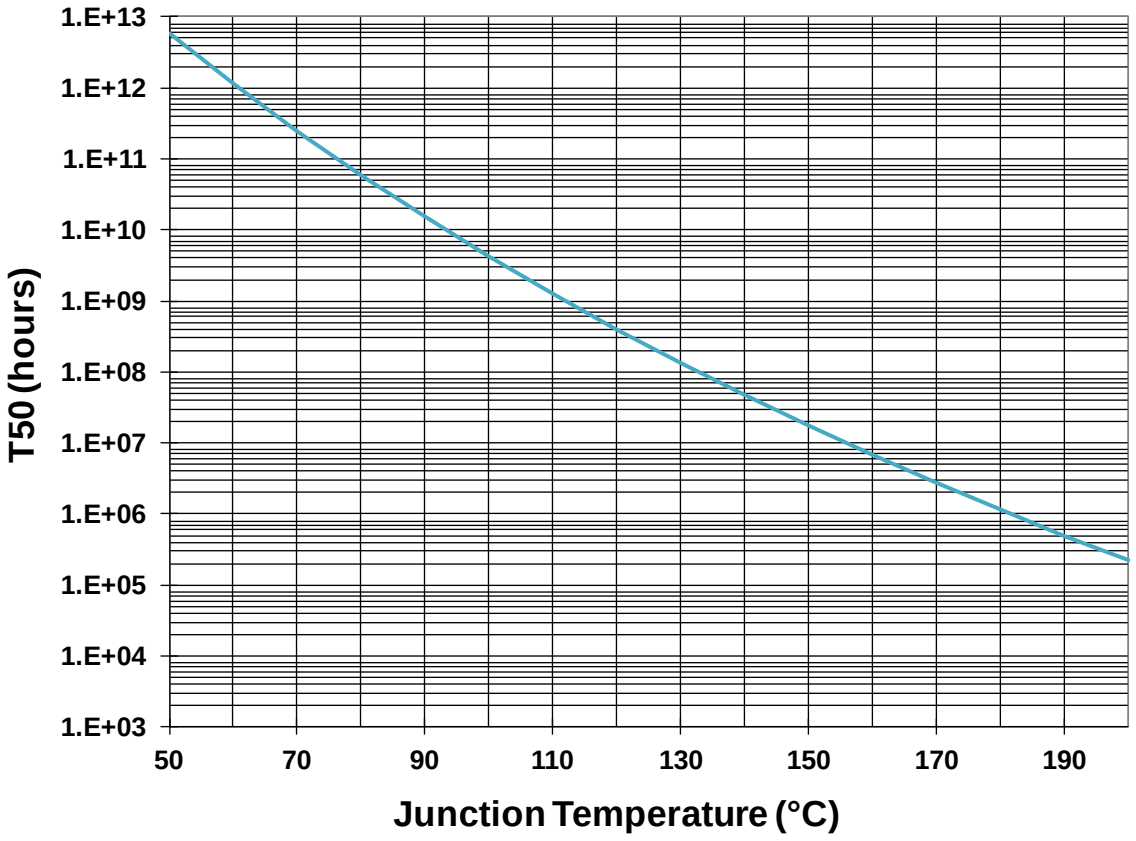
Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

Device thermal performances

All the figures given in this section are obtained assuming that the FAB device is only cooled down by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tcase).
The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Absolute Maximum Ratings table.
So, the system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	Tjunction (°C)	R_{TH} (°C/W)	T50 (hours)
R_{TH} (1) Thermal Resistance (Junction to Case)	Vd= 3V Id= 60mA Pdiss= 0.172W	90	29	1.05E+10

(1) Assuming 85°C Tcase

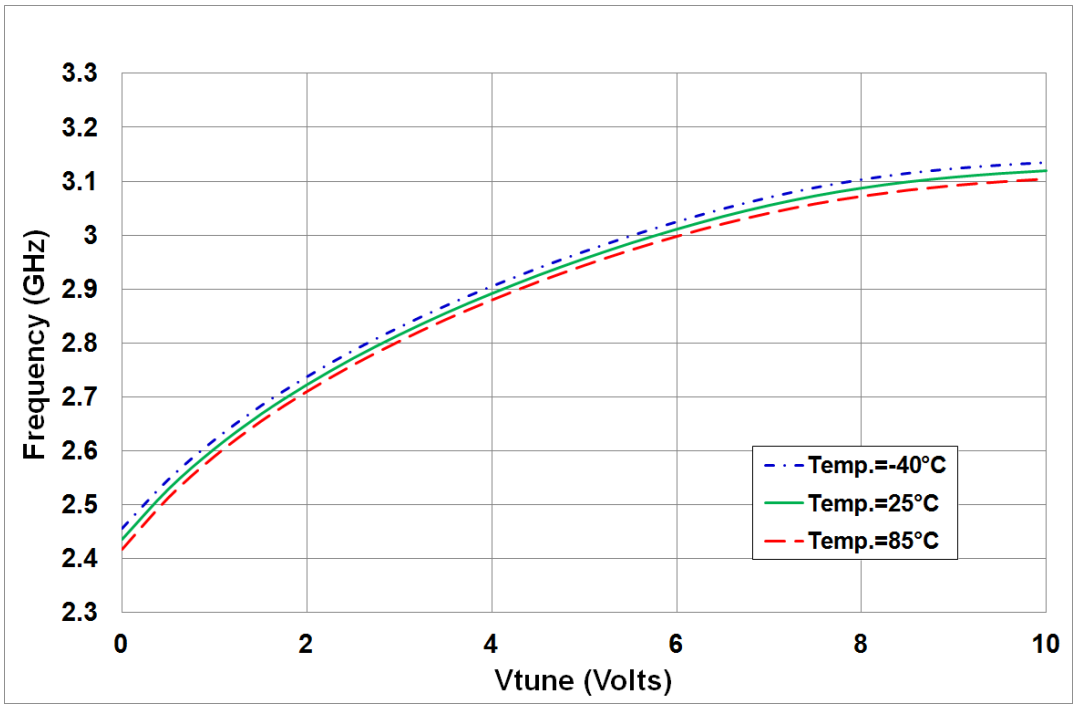


Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

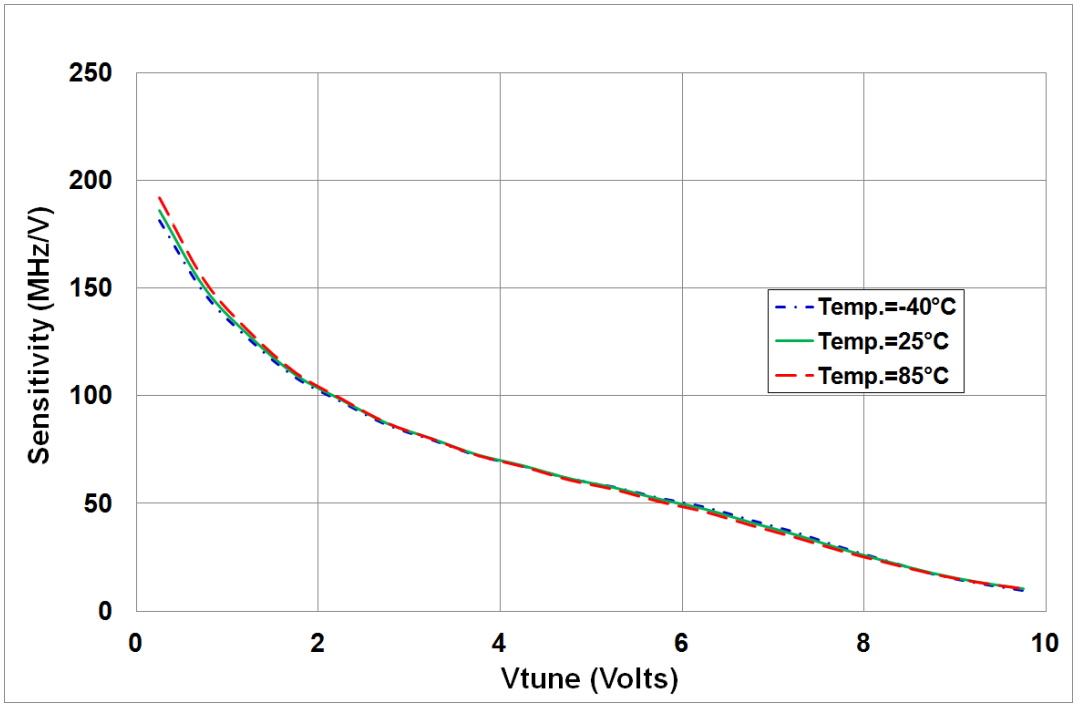
Typical Board Measurements

Temperature = -40, +25, +85°C, Vd = +3V, Id = 50mA
Measurements in the package reference planes.

Output Frequency versus Tuning Voltage



Sensitivity versus Tuning Voltage

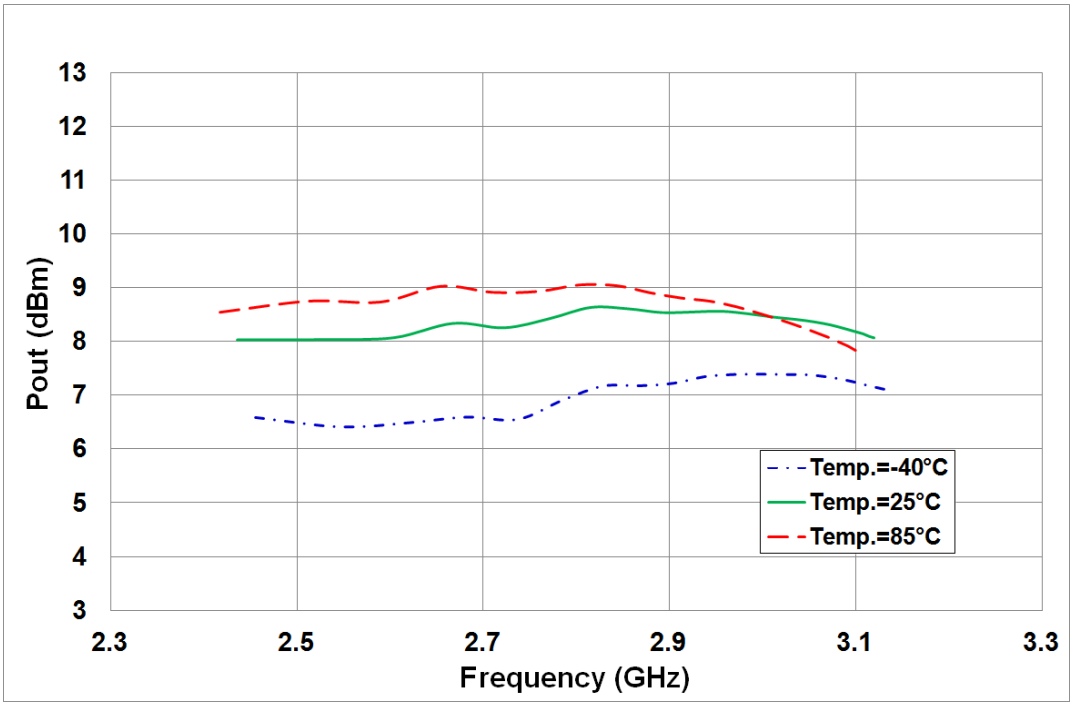


Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

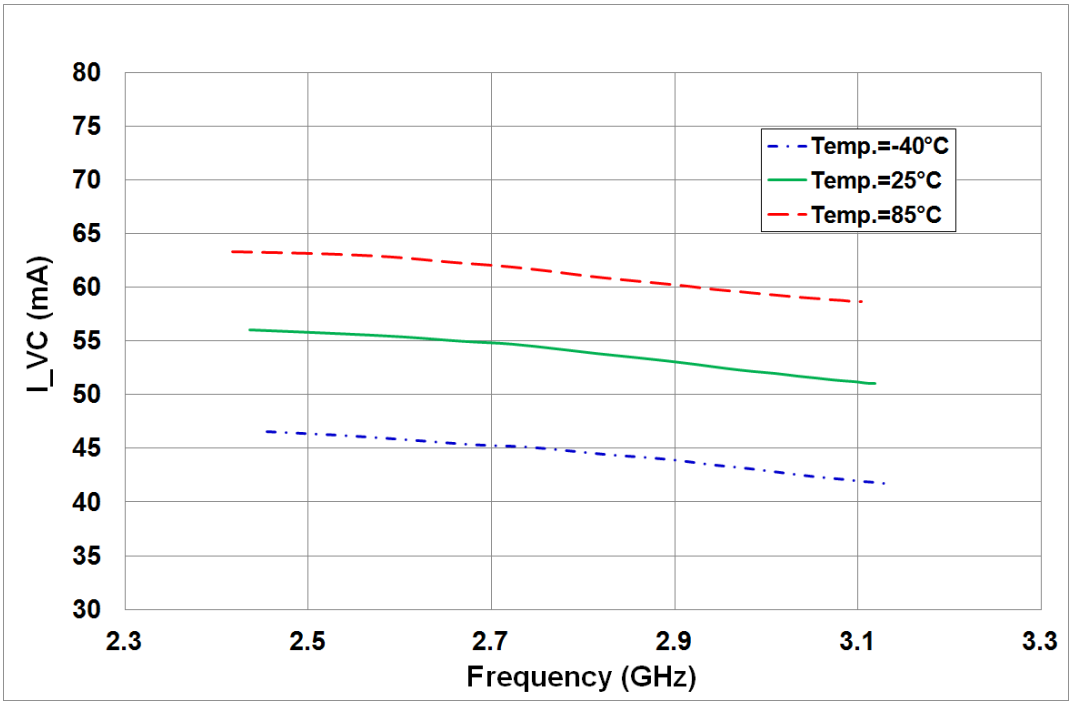
Typical Board Measurements

Temperature = -40, +25, +85°C, Vd = +3V, Id = 50mA
Measurements in the package reference planes.

Output Power versus Frequency



Supply Current versus Frequency

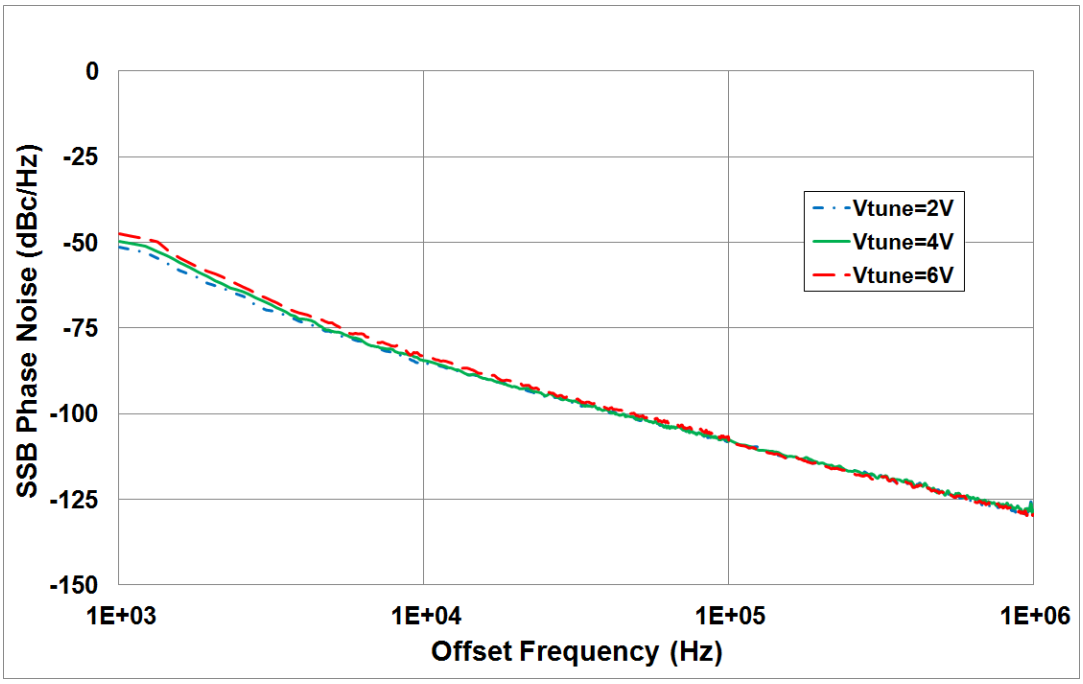


Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

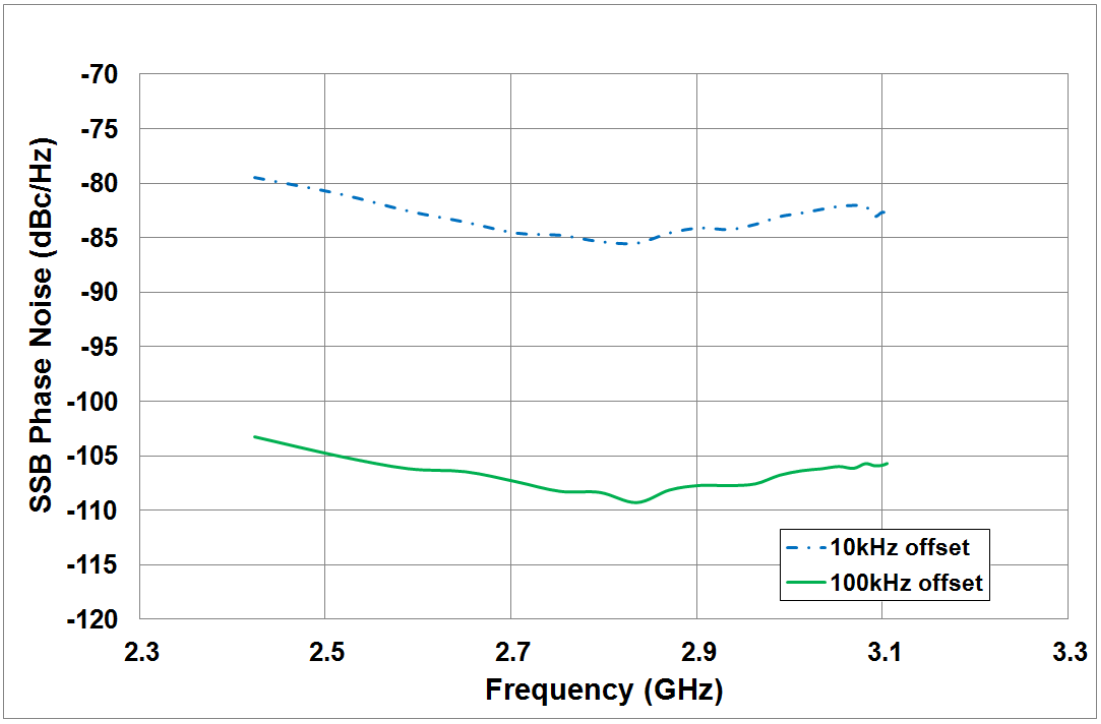
Typical Board Measurements

Temperature = +25°C, Vd = +3V, Id = 50mA
Measurements in the package reference planes.

Typical SSB Phase Noise @ Vtune = +2 / +4 / +6V

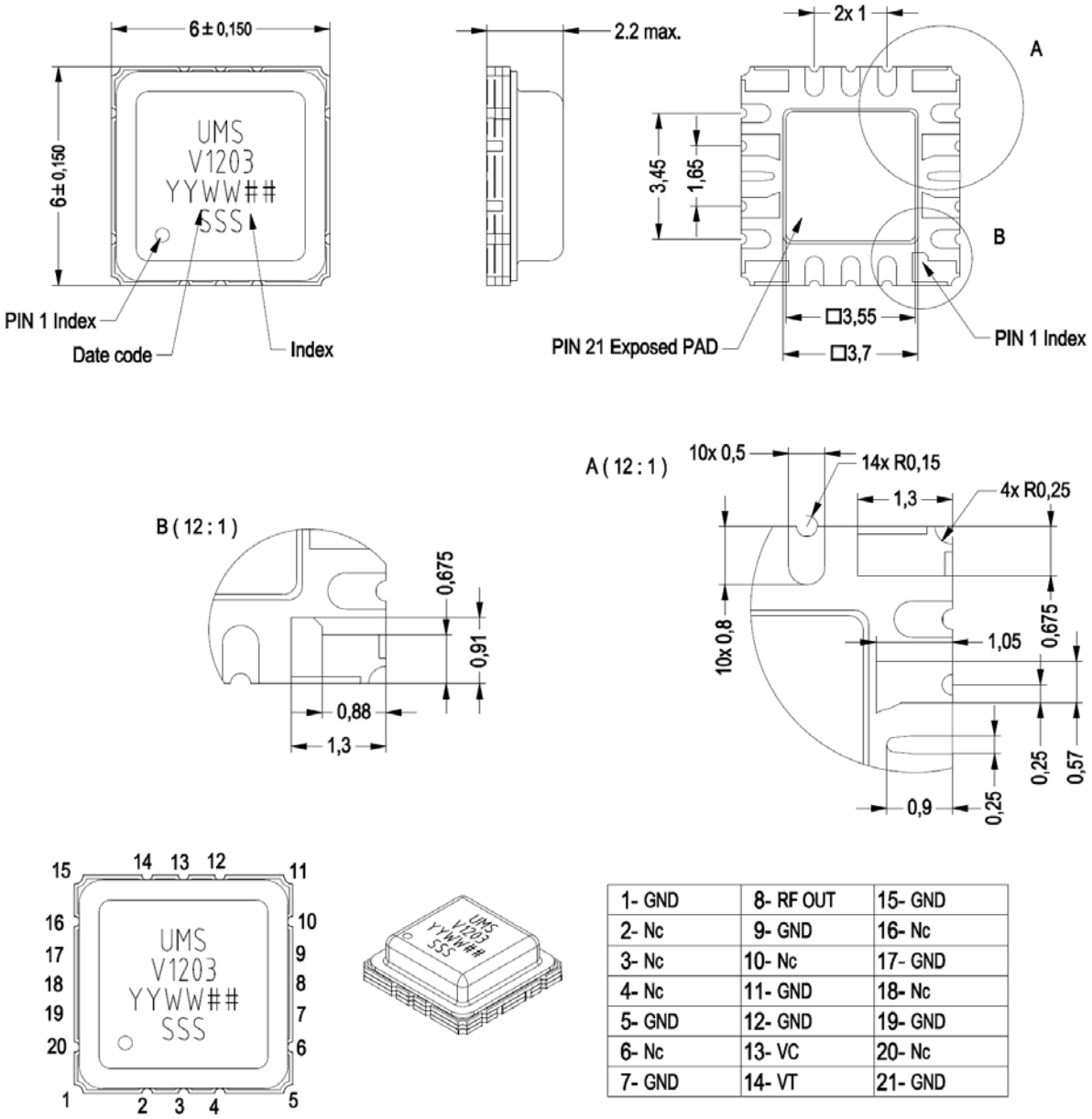


Phase Noise versus Frequency



Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

Package outline (1)



1- GND	8- RF OUT	15- GND
2- Nc	9- GND	16- Nc
3- Nc	10- Nc	17- GND
4- Nc	11- GND	18- Nc
5- GND	12- GND	19- GND
6- Nc	13- VC	20- Nc
7- GND	14- VT	21- GND

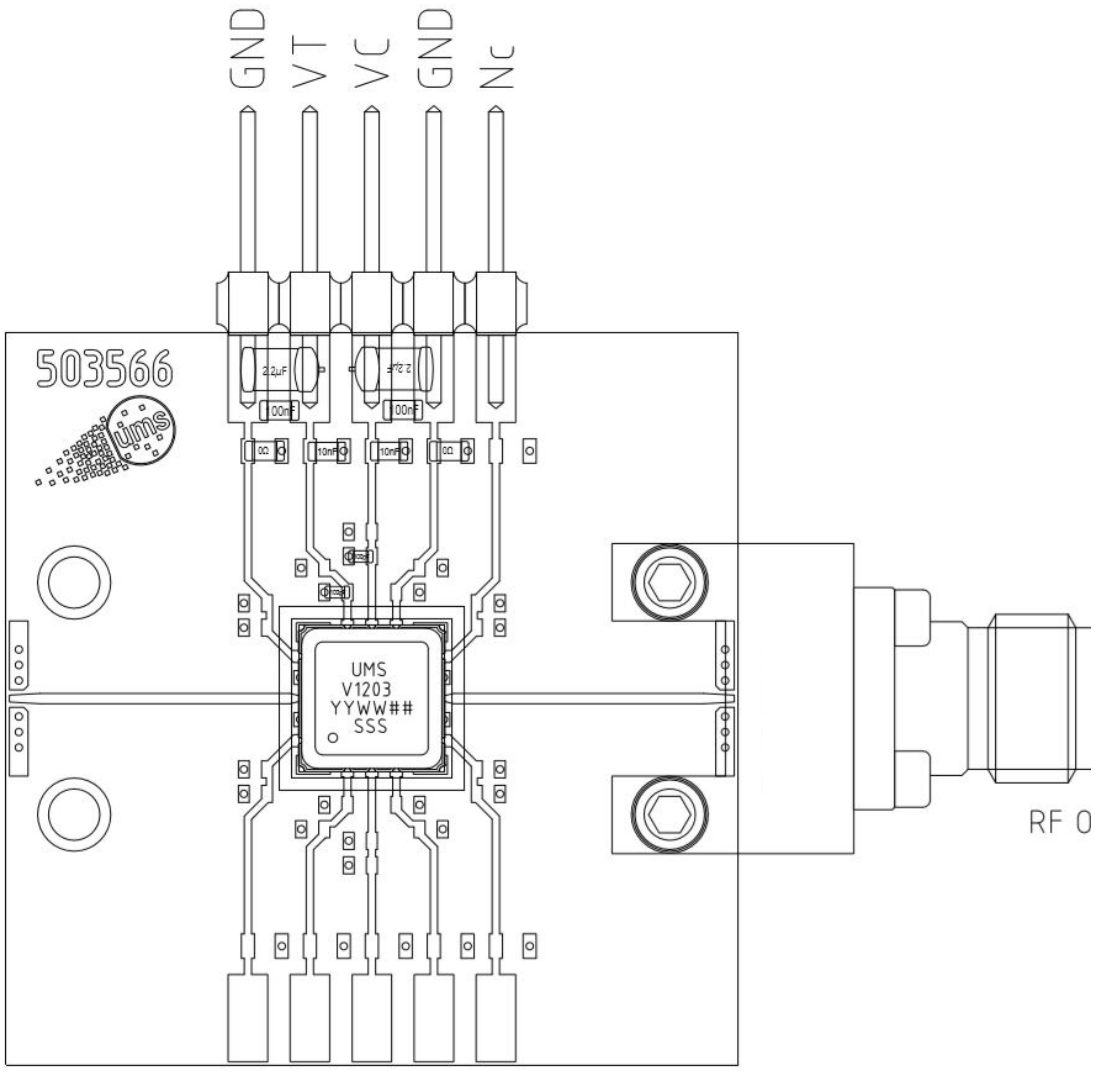
All dimensions are in mm

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0024 (http://www.ums-gaas.com) for exact package dimensions.
It is strongly recommended to ground all pins marked “GND” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 100pF, 10nF ±10% and 100nF, 2.2µF ±10% are recommended for all DC accesses.



Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com

Recommended package footprint for FAB Package

Refer to the application note AN0024 available at http://www.ums-gaas.com for package foot print recommendations and exact package dimensions.

SMD mounting procedure for FAB Package

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0024 available at http://www.ums-gaas.com.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

FAB 6x6 package:	CHV1203-FAB/XY Waffle pack: XY = 24

Bât. Charmille - Parc SILIC - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-gaas.com