Fully Integrated Q-band VCO

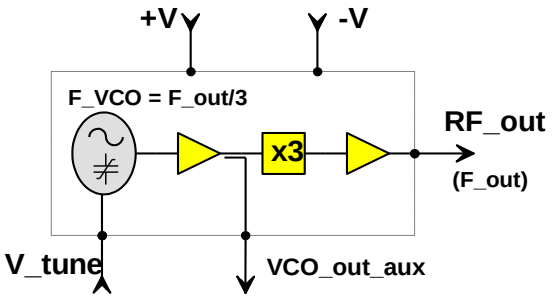
GaAs Monolithic Microwave IC

Description

The CHV2243a99F is a monolithic multifunction circuit dedicated to frequency generation. It integrates a Ku-band oscillator with frequency control (VCO), a Q-band frequency multiplier and buffer amplifiers. The VCO is fully integrated. On chip pHEMT based Schottky diode is used as varactor. All the active devices are internally self biased.

The circuit is manufactured with the pHEMT process 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

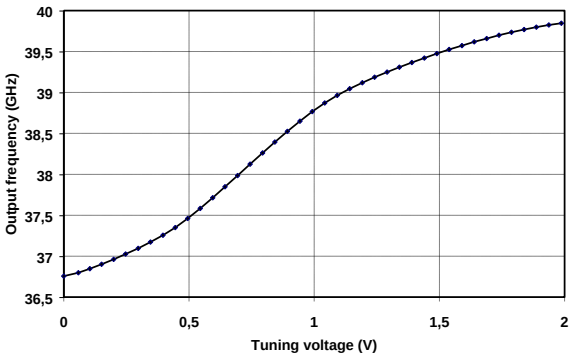
It is available in chip form.



Multifunction block diagram

Main Features

- Ku-band VCO + Q-band multiplier
- Fully integrated VCO
- Wide frequency tuning range
- PLL oriented
- Auxiliary output at VCO frequency
- High temperature range
- On-chip self biasing
- Automatic assembly oriented
- Chip size 2.48x1.18x0.1mm



Typical tuning characteristic

Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
F_out	Output centre frequency	38	38.25	38.5	GHz
F_vco	Oscillator frequency		F_out/3		
F_tune1	Output frequency tuning range	1.5	3		GHz
Pout	Output power	4	8	12	dBm

ESD Protections: Electrostatic discharge sensitive device observe handling precautions !

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Electrical Characteristics

Tamb.= +25°C, Vd = +4.5V

Symbol	Parameter	Min	Typ	Max	Unit
F_out	Output centre frequency	38	38.25	38.5	GHz
F_vco	VCO frequency	F_out/3			dB
F_tune1	Maximum frequency tuning range (@ F_out)	1.5	3	4	GHz
F_tune2	Specified frequency tuning range (@ F_out) (1)	200	300	500	MHz
ΔF_tune2 (T)	Maximum variation of Frequency over temperature (2)	-300		+300	MHz
P_out	Output power on RF_out port	4	8	12	dBm
H1	Sub-harmonics rejection (F_out/3) (2)		-16	-11	dBc
H2	Sub-harmonics rejection (2*F_out/3) (2)		-17	-12	dBc
P_VCO	VCO output power on VCO_out_aux port (4)		-10		dBm
V_tune	Control voltage range		0.5-1	0 - 2	V
F_slope	Frequency tuning slope (2)	1000	2800	4500	MHz/v
ΔF_slope (T)	Maximum variation of Frequency tuning slope over temperature (2)	-26		+34	%
P_V+	Frequency pushing vs positive supply voltage (2)		150	450	MHz/v
P_V-	Frequency pushing vs negative supply voltage (2)		80	250	MHz/v
PN	Phase noise (given at F_out) (2) @ 1kHz @ 10kHz @ 100kHz @ 200kHz @ 1MHz		 -5 -35 -65 -73 -92	 +5 -25 -55 -63 -82	dBc/Hz
+V	Positive supply voltage (3)	4.4	4.5	4.6	V
+I	Positive supply current		115	180	mA
-V	Negative supply voltage (3)	-4.6	-4.5	-4.4	V
-I	Negative supply current		4	10	mA
Top	Operating temperature range	-40		+100	°C

(1) F_tune2 is the frequency tuning range relative to the specified parameters, this frequency tuning range has to be inside 38 to 38.5GHz.
(2) Specified within F_tune2
(3) Negative supply voltage must be applied at least 1µs before positive supply voltage
(4) This output is optional, it can be not connected

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
V_tune	Tuning voltage	2.5	V
+V	Positive supply voltage	5	V
-V	Negative supply voltage	-5	V
+I	Positive supply current	250	mA
-I	Negative supply current	15	mA
Tstg	Storage temperature range	-55 to +155	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

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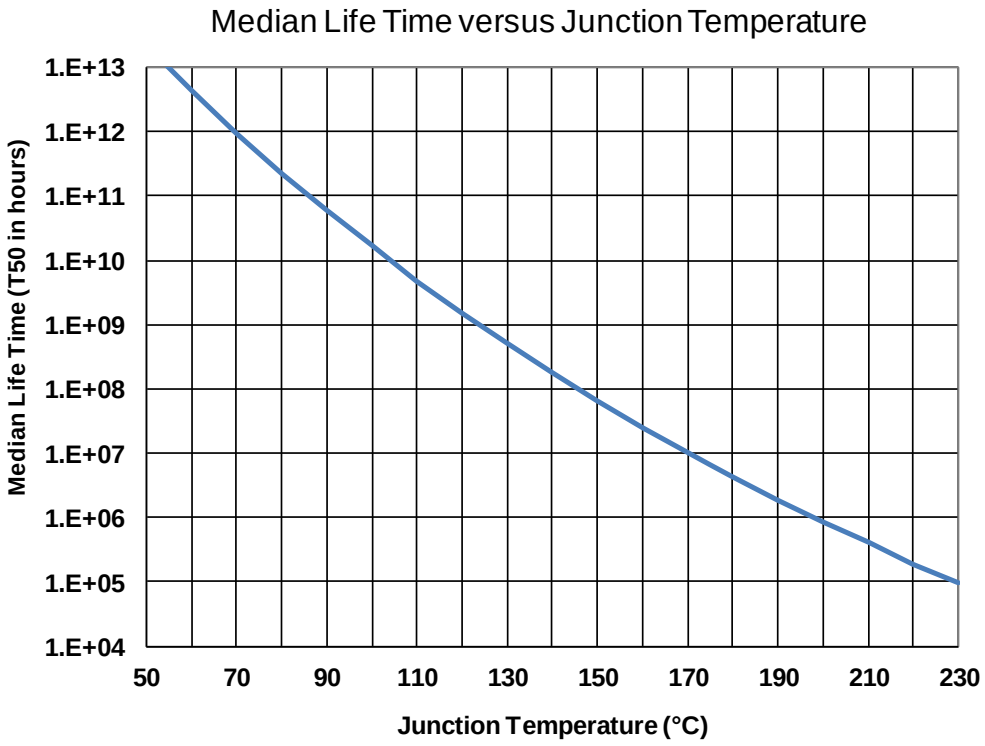
Device thermal performances

All the figures given in this section are obtained assuming that the packaged device is only cooled down by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tcase).
The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Absolute Maximum Ratings table.
So, the system PCB must be designed to comply with this requirement.

Parameter	Symbol	Conditions	Values	Unit
Thermal Resistance	Rth_eq	Tb = 85°C, V+=4.5V V-=-4.5V, 115mA, -4mA Pout=_dBm (Pdiss = 0.53W)	70	°C/W
Junction Temperature	Tj		122	°C
Median Lifetime	T50		$1.0x10^9$	Hrs

(1) Refer to “Chip Biasing options” section.



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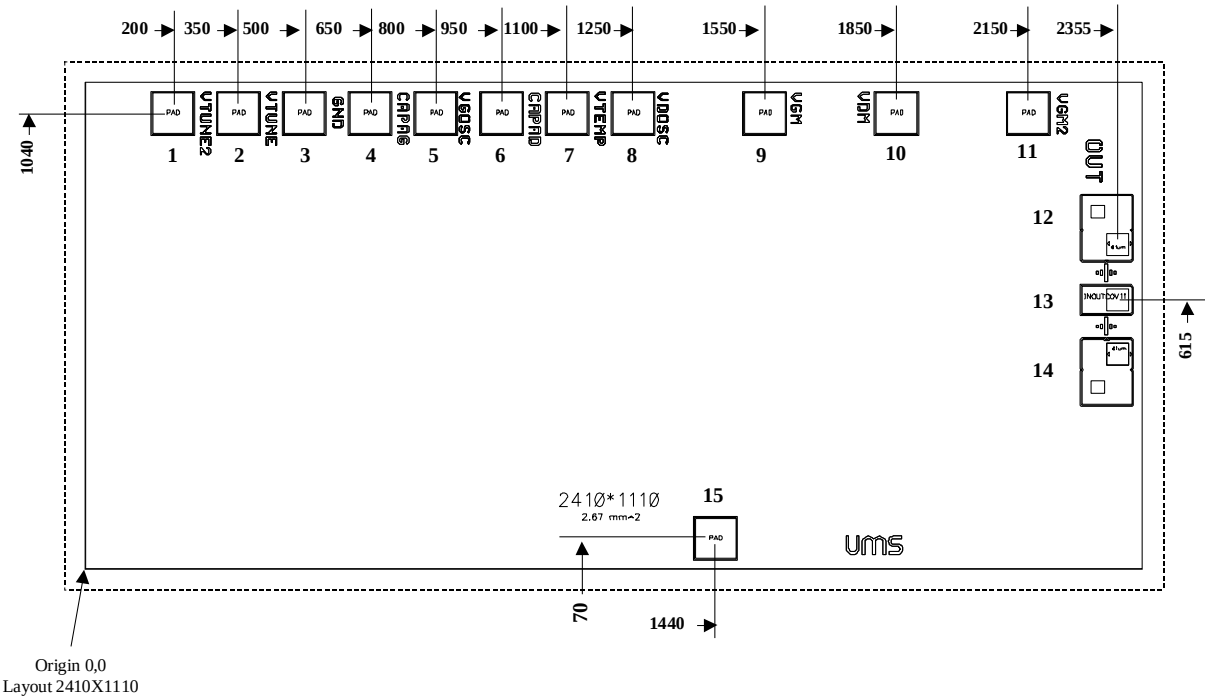
Mechanical data



Unit = µm
External chip size (including saw streets) = 2480 x 1180 +/- 35
Chip thickness = 100 +/- 10
RF Pad (13) = 68 x 118
VCO_out_aux Pad = 100 x 100
DC/IF Pads = 100 x 100

Pin number	Pin name	Description
12, 14		Ground: should not be bonded. If required, please ask for more information.
3		Ground (optional)
13	RF_out	RF output port @38GHz
8, 10	+V	Positive supply voltage
5, 9	-V	Negative supply voltage
4, 6, 7, 11		NC
1, 2	V_tune	Tuning voltage input ports (should be connected together, see typical assembly and bias configuration)
15	VCO_out_aux	Auxiliary VCO output at 12.7GHz (F_out / 3) (optional)

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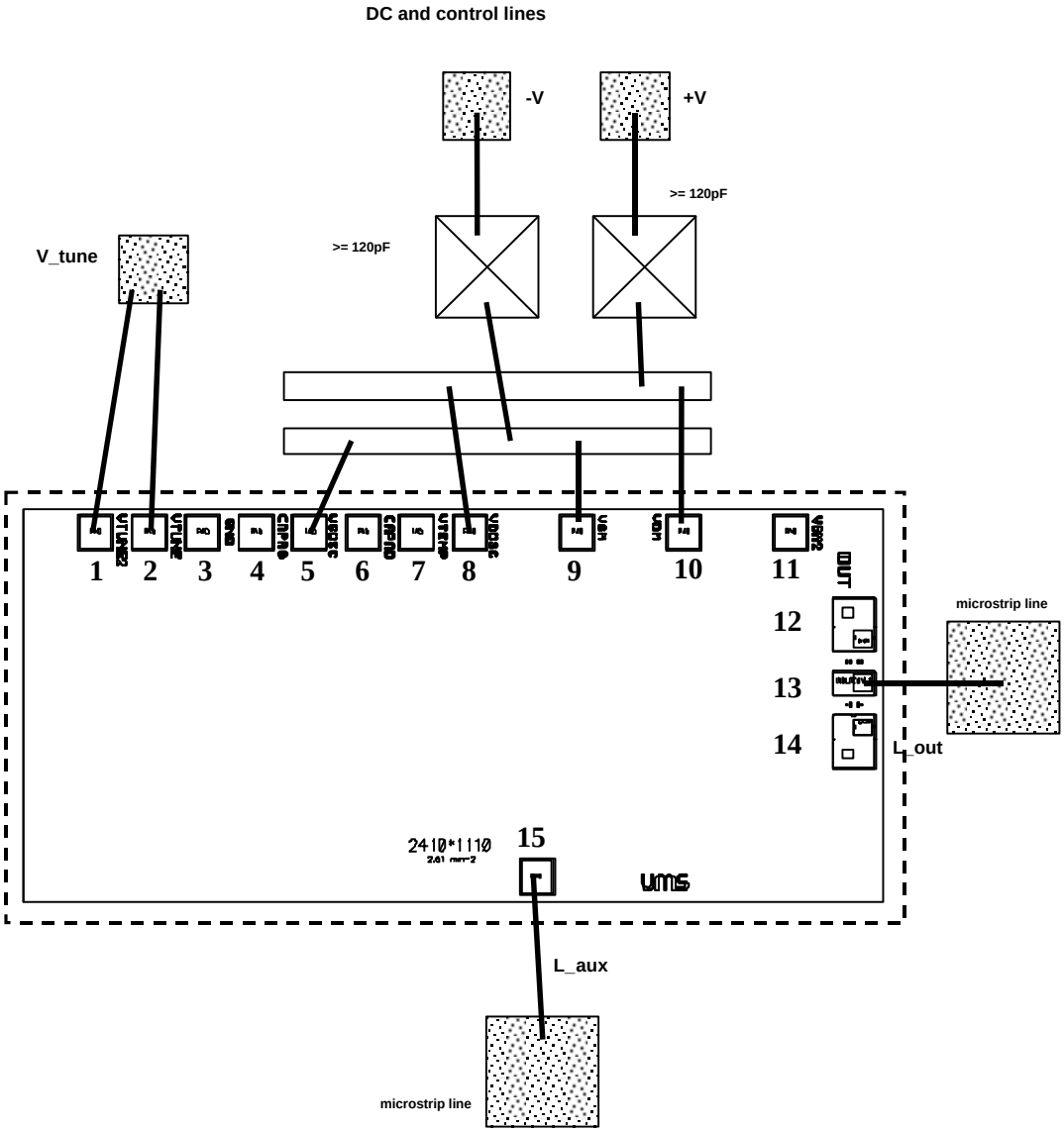
Recommended assembly plan



This drawing shows an example of assembly and bias configuration. All the transistors are internally self biased. The positive and negative voltages can be respectively connected together (see drawing) according to the recommended values given in the electrical characteristics table.

For the RF pads the equivalent wire bonding inductance (diameter=25µm) has to be according to the following recommendation:

Port	Equivalent inductance (nH)	Approximated wire length (mm)
RF_out (13)	L_out = 0.28	0.35
VCO_out_aux (15)	L_aux = 0.40	0.50

For a micro-strip configuration a hole in the substrate is recommended for chip assembly.

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Notes

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Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Ordering Information

Chip form:	CHV2243a99F/00

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