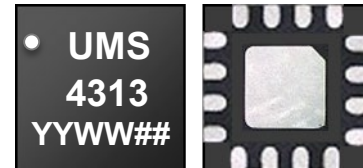


24-35GHz, 3-Way Power Divider/Combiner

GaAs Monolithic Microwave IC in SMD leadless package

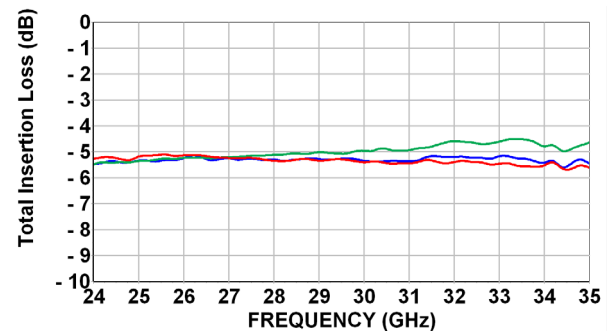
Description

The CHW4313-QAG is a 3-way 0° Power divider/Combiner designed for wideband operation from 24 to 35GHz. It supports many applications including phase array radars, 5G applications as well as satellites communications and Test & Measurements. The circuit is manufactured on a GaAs technology dedicated to high performance. It is supplied in RoHS compliant 3x3mm SMD package.



Main Features

- Broadband performances: 24-35GHz
- Insertion Loss (above 4.8 dB): 0.6dB
- Isolation in the range of 20dB
- Good amplitude unbalance: +/- 0.5dB
- Good phase unbalance: - 5°
- 16L QFN3x3
- MSL1



Path: S->1 Path S->2 Path S->3

Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	24		35	GHz
IL	Insertion Loss (above 4.8 dB):		0.6		dB
Isolation	Isolation		20		dB
AU	Amplitude Unbalance		+/- 0.5		dB
PU	Phase Unbalance		-5		°

CHW4313-QAG 24-35GHz, 3-Way Power Divider/Combiner

Specifications

Tamb.= +25°C,

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	24		35	GHz
IL	Insertion Loss (above 4.8 dB)		0.6		dB
Isolation	Isolation		20		dB
AU	Amplitude Unbalance		+/- 0.5		dB
PU	Phase Unbalance		-5		°
RL_Sum	Return Loss (Port Sum)		16		dB
RL_123	Return Loss (Port 1-2-3)		18		dB
PH	Power Handling			20	dBm

These values are representative of on board measurements as defined on the drawing in paragraph "Evaluation board for measurements accuracy (RF probes)"

The reference planes used for Sij measurements presented in this document are located at 0.8mm offset from the package edges.

Absolute Maximum Ratings ⁽¹⁾

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Pin	Maximum input power (AMR)	20	dBm

⁽¹⁾ Operation of this device above this parameter may cause permanent damage.

Temperature Range

Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

CHW4313-QAG 24-35GHz, 3-Way Power Divider/Combiner

Typical Package Sij parameters

Tamb.= +25°C.

The reference planes used for Sij measurements presented in this document are located at 0.8mm offset from the package edges.

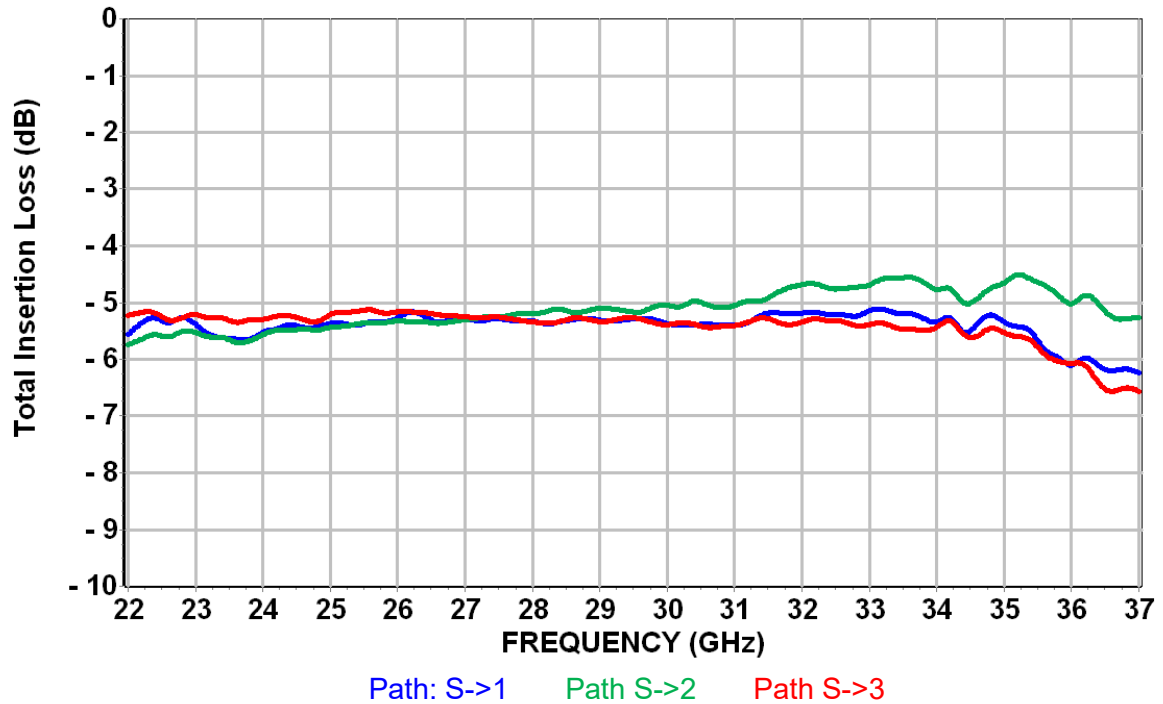
Path : S->1

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
22,00	-11,58	-136,01	-5,57	2,32	-5,57	2,30	-18,15	-171,94
22,50	-14,94	-136,14	-5,16	-5,93	-5,17	-5,97	-18,61	-175,76
23,00	-12,04	-132,78	-5,38	-16,60	-5,39	-16,64	-16,97	178,88
23,50	-12,42	-155,45	-5,53	-23,36	-5,55	-23,41	-16,77	170,83
24,00	-13,43	-173,51	-5,52	-30,61	-5,53	-30,66	-15,81	165,95
24,50	-16,92	-170,67	-5,25	-39,41	-5,27	-39,43	-15,77	160,59
25,00	-15,07	-172,22	-5,37	-48,58	-5,37	-48,63	-14,81	157,79
25,50	-15,83	170,86	-5,36	-56,64	-5,37	-56,63	-14,55	149,73
26,00	-18,14	166,75	-5,27	-65,00	-5,27	-64,99	-14,14	147,11
26,50	-16,30	171,42	-5,30	-74,45	-5,30	-74,42	-13,92	140,56
27,00	-18,15	169,65	-5,26	-83,52	-5,26	-83,40	-13,67	137,32
27,50	-19,90	159,90	-5,30	-91,58	-5,31	-91,45	-13,63	130,26
28,00	-18,73	155,41	-5,32	-100,39	-5,33	-100,27	-13,92	127,92
28,50	-20,12	149,08	-5,30	-109,16	-5,32	-109,00	-14,02	120,82
29,00	-24,36	171,88	-5,31	-117,91	-5,31	-117,77	-15,13	118,19
29,50	-21,56	167,51	-5,31	-127,09	-5,31	-126,92	-15,45	113,98
30,00	-19,51	-176,33	-5,37	-135,66	-5,37	-135,51	-16,91	112,72
30,50	-20,39	-170,92	-5,39	-144,40	-5,39	-144,25	-17,78	109,46
31,00	-14,36	-176,96	-5,39	-152,17	-5,39	-152,02	-19,82	108,05
31,50	-15,81	178,12	-5,29	-161,67	-5,29	-161,50	-22,93	112,05
32,00	-16,19	151,13	-5,18	-170,52	-5,18	-170,40	-27,73	136,35
32,50	-17,22	177,07	-5,16	179,95	-5,17	-179,92	-26,57	-171,44
33,00	-15,29	159,11	-5,14	171,08	-5,16	171,15	-21,92	-144,79
33,50	-18,38	-177,58	-5,13	160,42	-5,14	160,51	-17,12	-138,91
34,00	-14,02	-173,22	-5,34	150,83	-5,36	150,91	-14,34	-140,99
34,50	-12,57	-176,07	-5,33	142,22	-5,35	142,28	-11,83	-142,75
35,00	-12,30	179,21	-5,34	131,15	-5,35	131,23	-10,20	-149,87
35,50	-10,21	-177,30	-5,63	121,04	-5,63	121,15	-8,64	-152,51
36,00	-8,23	169,74	-6,10	112,12	-6,10	112,29	-7,62	-159,33
36,50	-8,81	159,55	-5,96	104,36	-5,96	104,51	-6,28	-161,90
37,00	-8,38	156,98	-6,24	93,82	-6,23	93,92	-5,35	-169,44

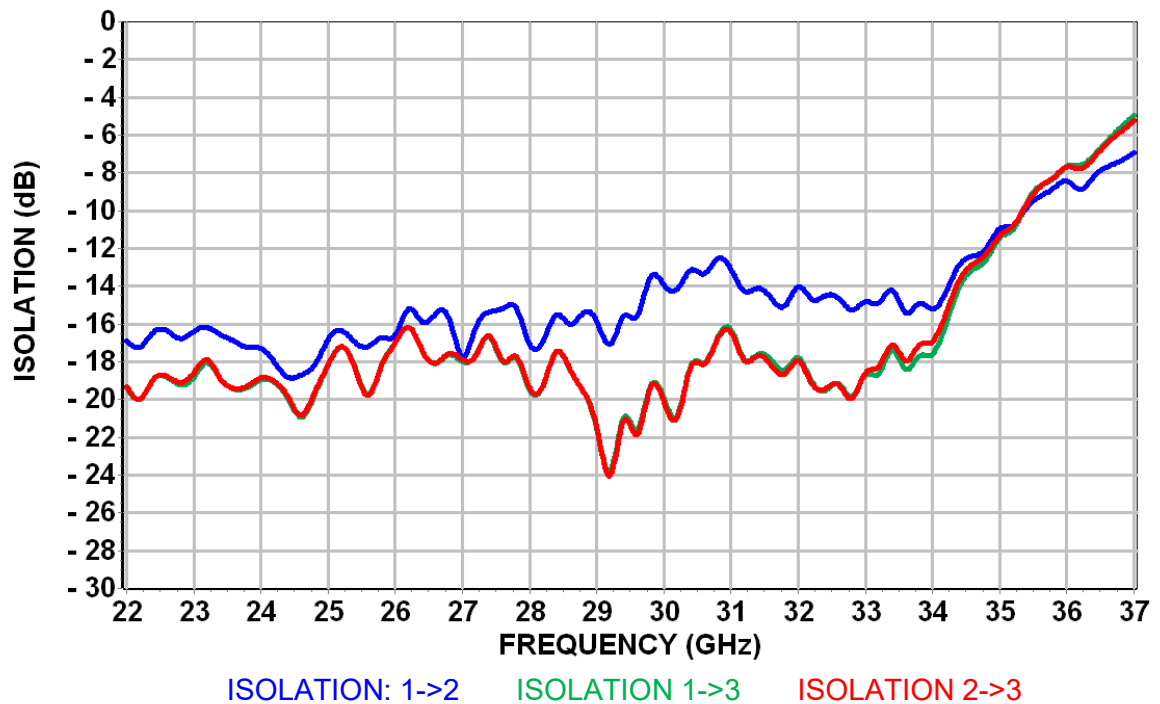
Typical on Board Measurements

Tamb.= +25°C (see "Evaluation board for measurements accuracy using RF probes")

Total Insertion Loss versus Frequency



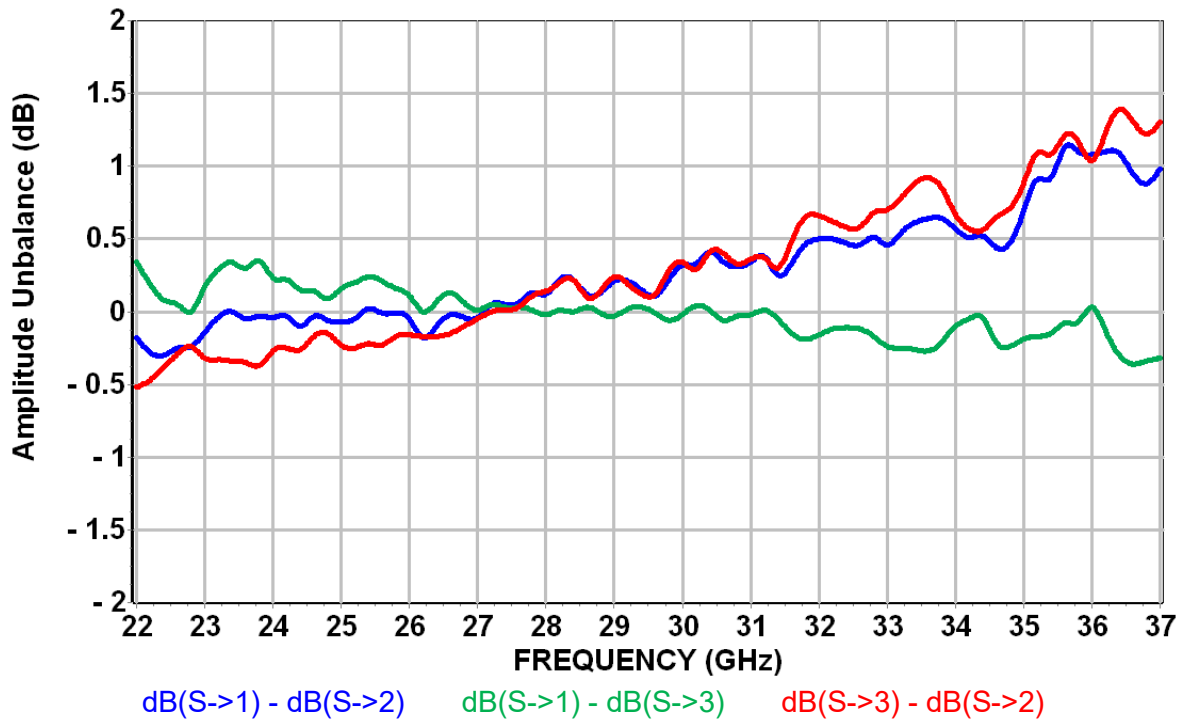
Isolation versus Frequency



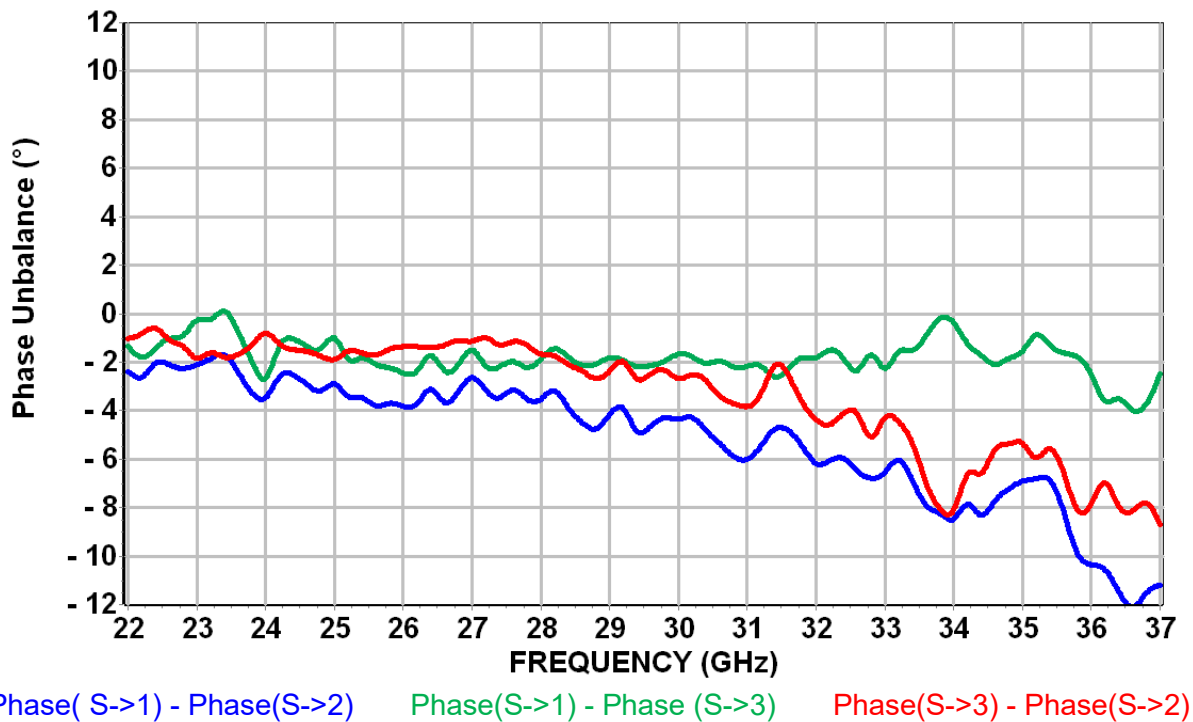
Typical on Board Measurements

Tamb.= +25°C (see “Evaluation board for measurements accuracy using RF probes”)

Amplitude Unbalance versus Frequency



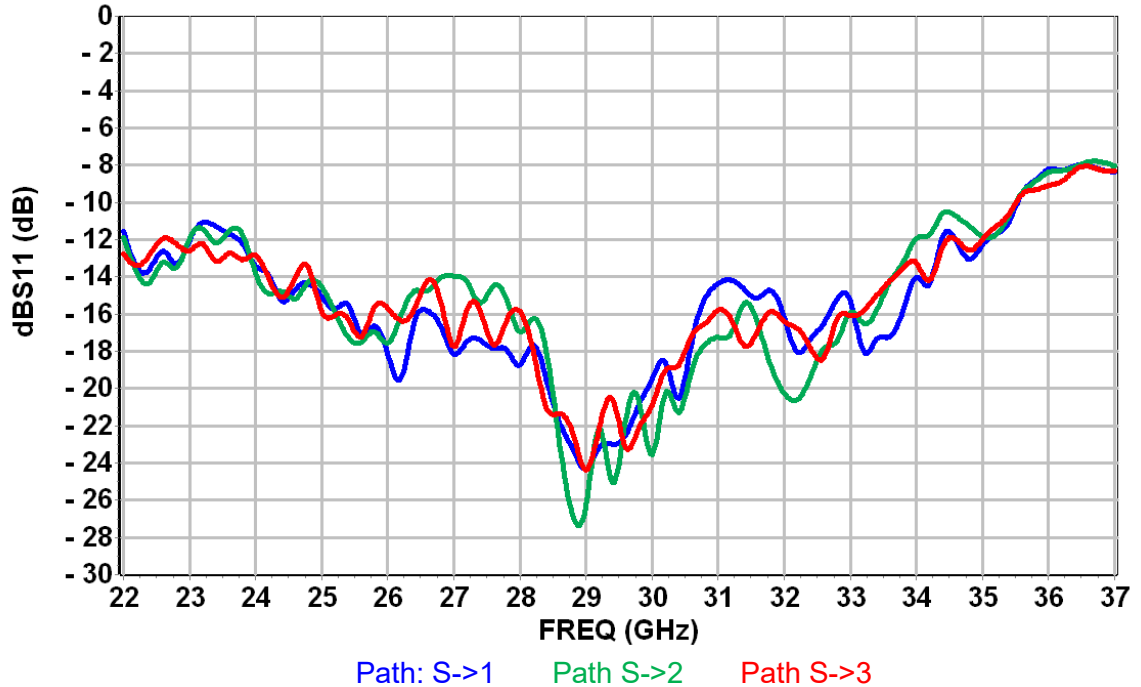
Phase Unbalance versus Frequency



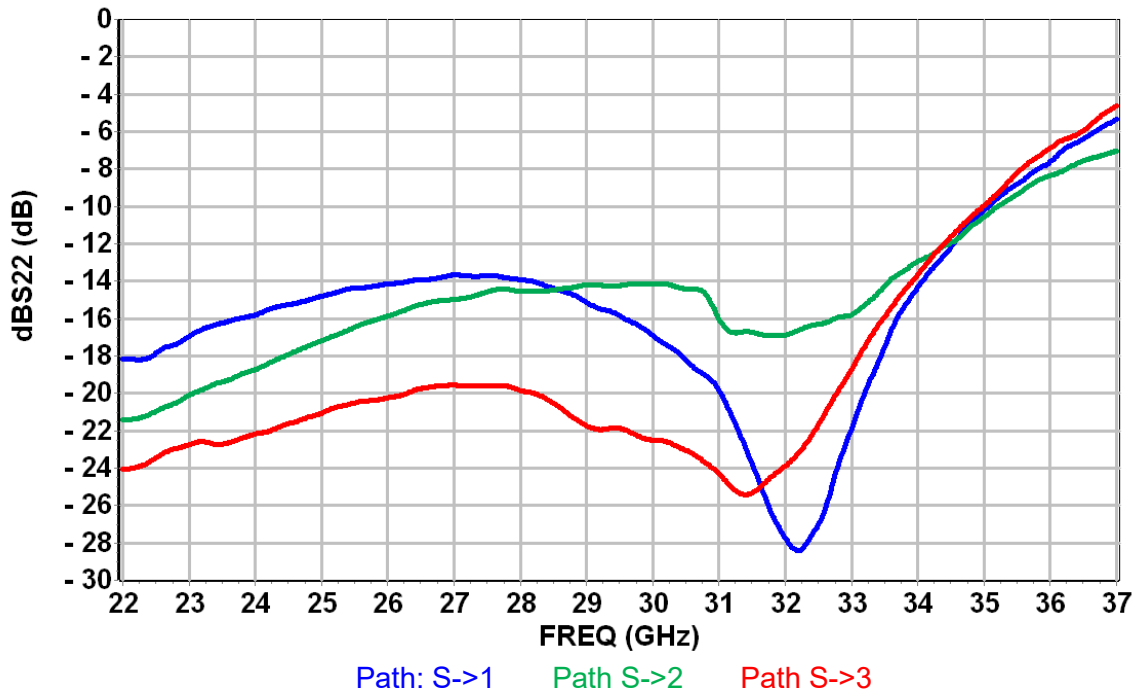
Typical on Board Measurements

Tamb.= +25°C (see "Evaluation board for measurements accuracy using RF probes")

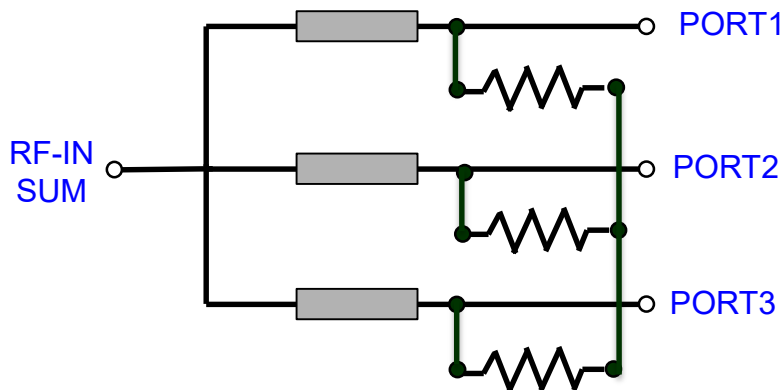
Input Return Loss (SUM) versus Frequency



Output Return Loss (Port 1,2,3) versus Frequency



Simplified Schematic for the 3-Way 0° 50 ohms Power Divider / Combiner



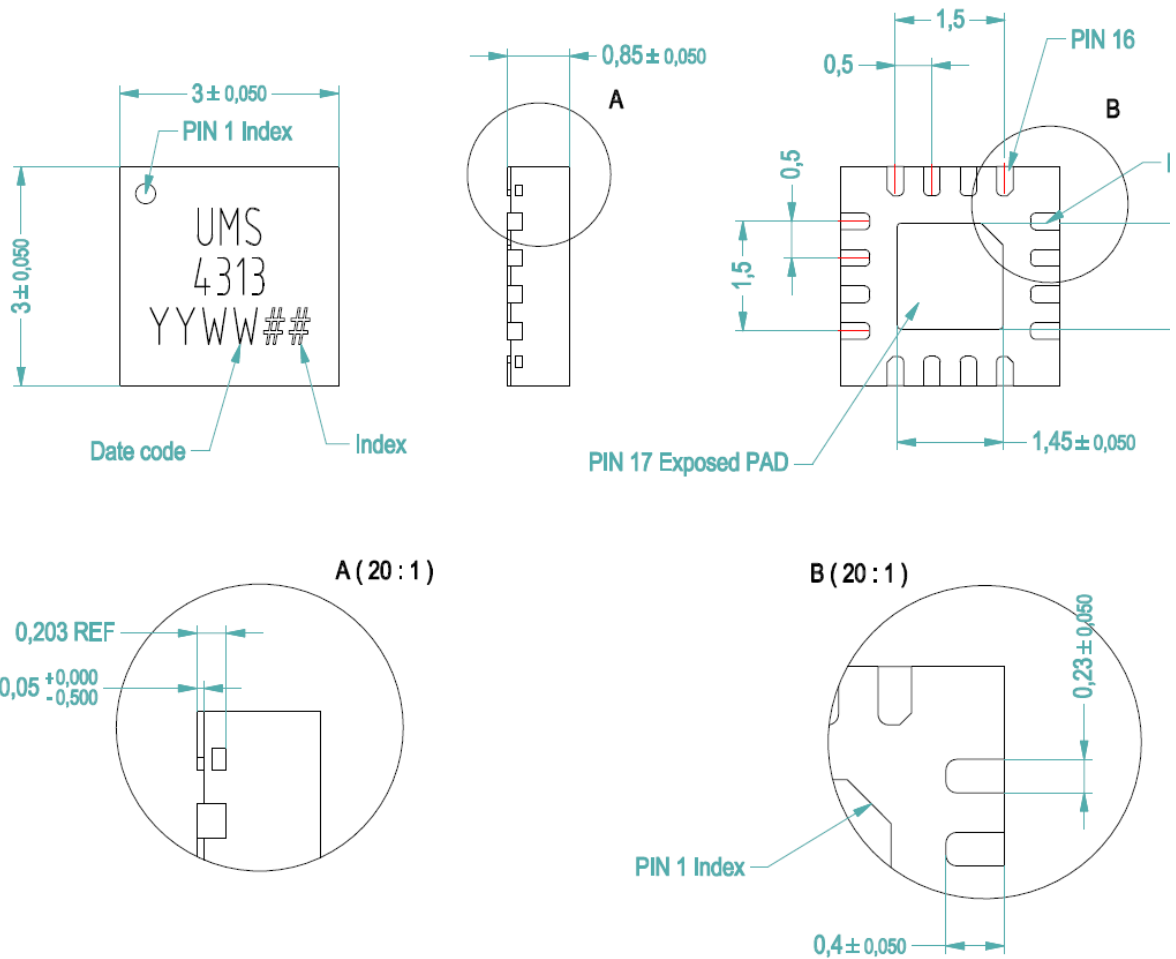
The SUM PORT has been noted S in the previous pages of this document.

Path S->1 is entering the part on the SUM port and exiting thru the PORT1 (North access of the package)

Path S->2 is entering the part on the SUM port and exiting thru the PORT2 (East access of the package)

Path S->3 is entering the part on the SUM port and exiting thru the PORT3 (South access of the package)

Package outline (1)



Lead Free	(Green)	1- GND	11- PORT2
Units :	mm	2- SUM	12- GND
From the standard :	JEDEC MO-220	3- GND	13- GND
	(VEED)	4- NC	14- PORT1
	17- GND	5- NC	15- GND
		6- GND	16- NC
		7- PORT3	
		8- GND	
		9- NC	
		10- GND	

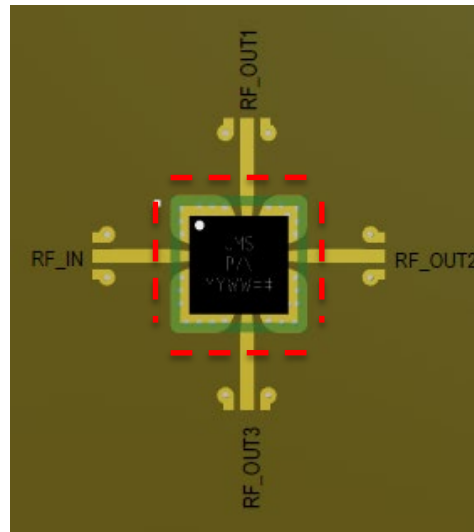
(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (<https://www.ums-rf.com>) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

Evaluation mother board for measurements accuracy (RF probes)

Losses due to board are partly de-embedded: the reference planes used for Sij measurements presented previously in this document are located at 0.8mm offset from the package edges. Reference planes are showed in red on the drawing.

Note: The given Sij parameters incorporate the land pattern of the evaluation motherboard.

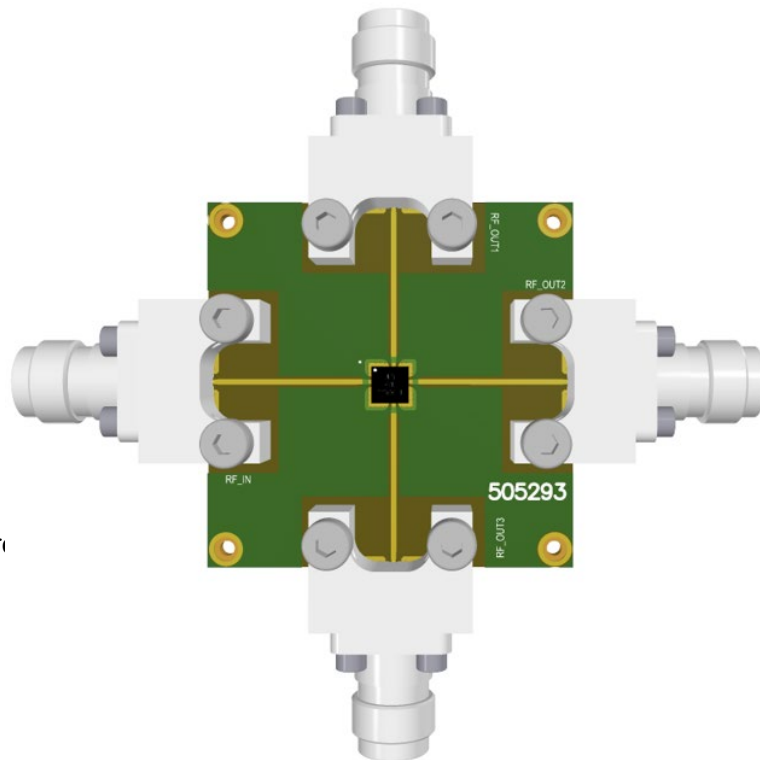


Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% matte tin (Sn)
MSL Rating	MSL1

Evaluation mother board for temperature characterization

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- See application note AN0017 for details.



Note: All board measurement operation.

Be safe

CHW4313-QAG 24-35GHz, 3-Way Power Divider/Combiner

Recommended package footprint

Refer to the application note AN0017 available at <https://www.ums-rf.com> for package footprint recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017 at <https://www.ums-rf.com>.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <https://www.ums-rf.com>.

Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com> for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 3x3 package:

CHW4313-QAG/XY

Tape & Reel: XY = 21

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