United Monolithic Semiconductors

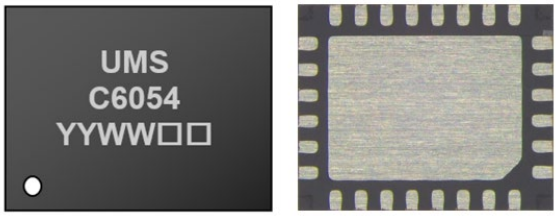
CHC6054-QQA

24.25-30.5GHz RF Front-End

GaN & GaAs Monolithic Microwave IC SMD leadless package

Description

The CHC6054-QQA is a high power front end (HPFE) incorporating transmit and receive paths and a T/R switch for telecom radio systems, operating in the 24.25-30.5GHz frequency range. It typically exhibits an Rx gain of 18dB with a low noise figure of 3.2dB, and a Tx gain of 28dB with 31dBm saturated output power. It features high linearity with an ACPR of 36dBc @23dBm average Pout. It is realized on mixed technologies 150nm Gallium Nitride on Silicon Carbide (AlGaN/GaN on SiC) and 150nm Gallium Arsenide (GaAs) and provided in a cost effective plastic QFN 4x5 mm^2 package.



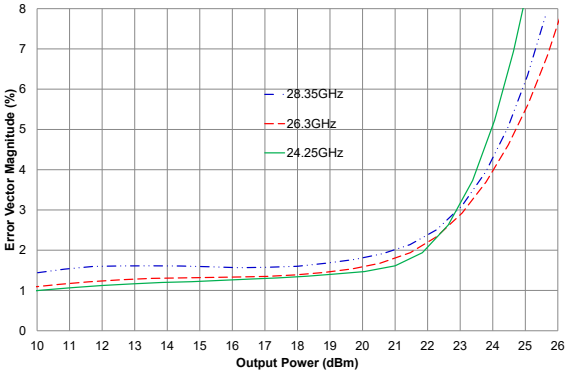
Main Features

- Frequency Range : 24.25-30.5GHz
- Tx Gain = 28dB
- Rx Gain = 18dB
- Tx Output Psat: 31dBm (@5dB gain comp)
- Rx Input P1dB: -7dBm
- EVM < 3.5% at CS = 56MHz or 112MHz, 4/16/64/128/256 and 1024QAM
- 28L-QFN 4x5mm // MSL3

Error Vector Magnitude (%) versus Output Power

Channel Spacing=56MHz

256 QAM modulation without DPD



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	24.25		30.5	GHz
Tx Gain	Linear Gain		28		dB
Tx Psat	Output power at 5dB gain compression		31		dBm
Rx Gain	Linear Gain		18		dBm

United Monolithic Semiconductors S.A.S.
Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

Electrical Characteristics – TX Mode

Tamb.= +25°C, V_{d12} = 25V, V_{g12} set in order to get I_{d12} = 40mA

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	24.25		30.5	GHz
Gain	Linear Gain		28		dB
RL_{in}	Input return loss		12		dB
RL_{out}	Output return loss		10		dB
$P_{diss.}$	Dissipated Power at P_{out} ≈23dBm		3		W
P_{5dB}	Output power at 5dB gain compression		31		dBm

These values are representative of measurements performed on evaluation board (see « Evaluation Board » section)

Electrical Characteristics – RX Mode

T_{amb}.= +25°C, V_{dL} =V_{g1L} = 4V @ I_{dL} = 60mA

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	24.25		30.5	GHz
Gain	Linear Gain		18		dB
NF	Noise Figure		3.25		dB
RL in	Input return loss		12		dB
RL out	Output return loss		17		dB
P1dB	Input power at 1dB gain comp		-7		dBm

These values are representative of measurements performed on evaluation board (see « Evaluation Board » section)

Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

Typical Bias Conditions

Symbol	Parameter	Tx mode	Rx mode	Unit
SW	Switch control voltage	0	20	V
V_{g1L}	LNA 1st stage gate voltage	0	4	V
V_{dL}	LNA drain voltage	0	4	V
V_{g1d}	Driver 1st stage gate voltage	4	0	V
V_{d1d}	Driver 1st stage drain voltage	4	0	V
V_{g2d}	Driver 2nd stage gate voltage	4	0	V
V_{d2d}	Driver 2nd stage drain voltage	4	0	V
V_{g12}	HPA gate voltage (quiescent biasing)	-3.1	0	V
V_{d12}	HPA drain voltage	25	0	V
I_s	DC Switch control current Max. Switch control current vs. Pin max.	0 1	0 1	mA
I_{gL}	DC LNA gate current (quiescent biasing) Max. Driver gate current vs. Pin max.	0 0	8 8	mA
I_{dL}	DC LNA drain current (quiescent biasing) Max. Driver drain current vs. Pin max.	0 0	60 70	mA
I_{gd}	DC Driver gate current (quiescent biasing) Max. Driver gate current vs. Pin max.	5 5	0 0	mA
I_{dd}	DC Driver drain current (quiescent biasing) Max. Driver drain current vs. Pin max.	130 175	0 0	mA
I_{g12}	DC HPA gate current (quiescent biasing) Max. HPA gate current vs. Pin max.	0.001 0.1	0 0	mA
I_{d12}	DC HPA drain current (quiescent biasing) Max. HPA drain current vs. Pin max.	40 500	0 0	mA

Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

Absolute Maximum Ratings – TX Mode (1)

Tamb.= +25°C

Symbol	Parameter	Value	Unit
V_{d12}	HPA Drain bias voltage	27	V
V_{g12}	HPA Gate bias voltage range	-7 to -2	V
I_{d12}	HPA drain current at saturated power	700	mA
V_{d1d} / V_{d2d}	Driver 1st /2nd stage drain voltage	4.5	V
V_{g1d} / V_{g2d}	Driver 1st /2nd stage gate voltage	4.5	V
I_{dd}	Driver drain current at saturated power	200	mA
SW	Switch Control voltage	0	V
P_{in}	Maximum Input power	+10	dBm
T_c	Operating temperature range	-40 to +95	°C
T_{stg}	Storage temperature range	-55 to +125	°C

(1) Operation of this device beyond any of these limits may cause permanent damage.

Absolute Maximum Ratings – RX Mode (2)

Tamb.= +25°C

Symbol	Parameter	Value	Unit
V_{dL}	Drain voltage	4.5	V
V_{g1L}	Gate voltage	4.5	V
I_{dL}	LNA drain current at saturated power	100	mA
SW	Switch Control voltage	20	V
P_{in}	Maximum Input power	-3	dBm
T_c	Operating temperature range	-40 to +95	°C
T_{stg}	Storage temperature range	-55 to +150	°C

(2) Operation of this device beyond any of these limits may cause permanent damage.

Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

Recommended Operating Parameters – TX Mode (3)

Tamb.= +25°C

Symbol	Parameter	Value	Unit
V_{d12}	HPA Drain bias voltage	18 to 25	V
V_{g12}	HPA Gate bias voltage (quiescent biasing)	-3.1	V
I_{d12}	HPA drain quiescent bias current	40	mA
V_{d1d} / V_{d2d}	Driver 1st /2nd stage drain voltage	4	V
V_{g1d} / V_{g2d}	Driver 1st /2nd stage gate voltage	4	V
I_{dd}	Driver drain quiescent bias current	130	mA
SW	Switch Control voltage	0	V
T_{rise}	Switch Rise Time	15	nS
T_{fall}	Switch Fall Time	11	nS
P_{in}	Maximum Input power	+8	dBm

(3) Electrical performances are defined for specified test conditions and are not guaranteed over all recommended operation conditions

Recommended Operating Parameters – RX Mode (4)

Tamb.= +25°C

Symbol	Parameter	Value	Unit
V_{d12}	HPA Drain bias voltage	18 to 25	V
V_{g12}	HPA Gate bias voltage	-5.0	V
V_{dL}	Drain bias voltage	4	V
V_{g1L}	Gate bias voltage	4	V
I_{dL}	LNA drain quiescent bias current	60	mA
SW	Switch Control voltage	20	V
T_{rise}	Switch Rise Time	25	nS
T_{fall}	Switch Fall Time	15	nS
P_{in}	Maximum Input power	-3	dBm

(4) Electrical performances are defined for specified test conditions and are not guaranteed over all recommended operation conditions

Temperature Ranges

T_c	Operating temperature range (QFN backside)	-40 to +85	°C
T_{stg}	Storage temperature range	-55 to +150	°C

Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

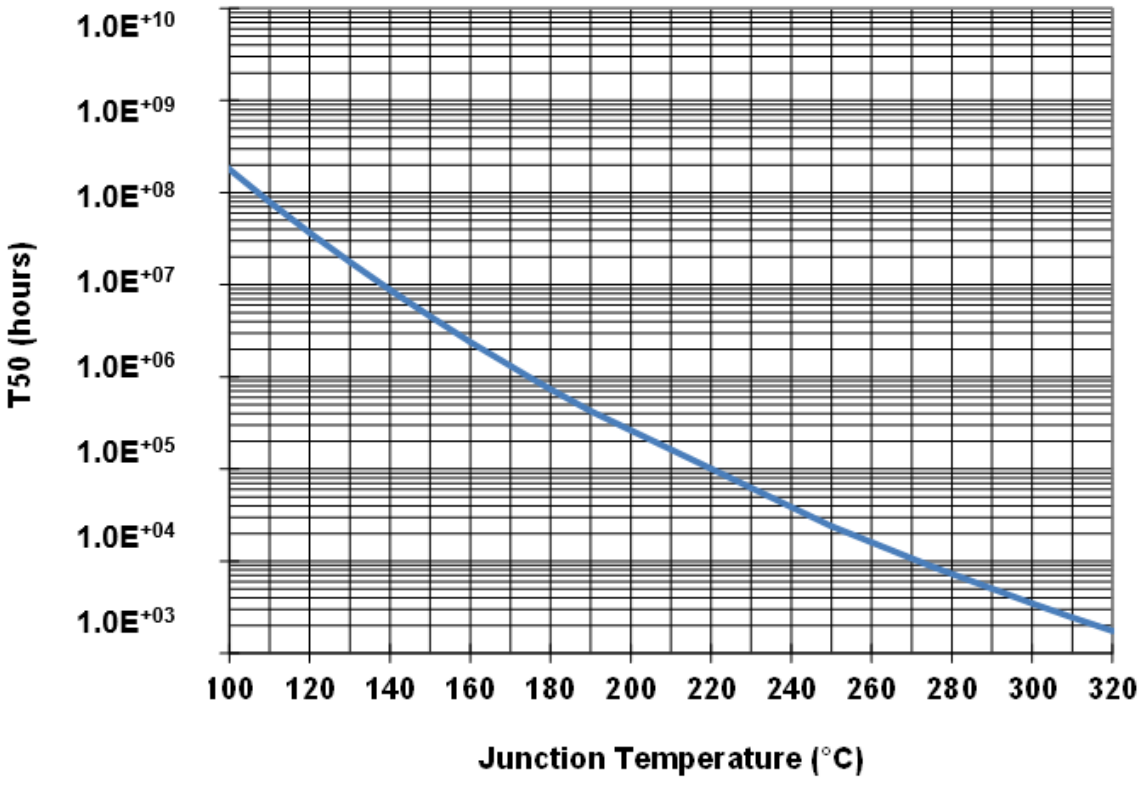
Device thermal information / TX Mode

The device thermal parameters below are based on UMS rules to evaluate the junction temperature.
This same procedure is the basis for junction temperature evaluation of the samples used to derive the median lifetime and activation energy for the particular technology on which the CHC6054-QQA Tx Mode is manufactured (GaN HEMT 0.15µm).
The temperature T_{case} is defined at the package back-side interface.
The system's maximum temperature must be adjusted in order to guarantee that $T_{junction}$ remains below the maximum value specified in the Absolute Maximum Rating table.
The PCB must be designed to meet this requirement.

Parameter	Biasing conditions	Tjunction (°C)	R_{TH} (°C/W)	T50 (hours)
R_{TH} (1) Thermal Resistance (Junction to Case)	Vd = 25V Id = 40mA P_{diss} = 3.5W	139	13.9	1.0E7

(1) Assuming 85°C T_{case}

Median Life time versus Junction Temperature



Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

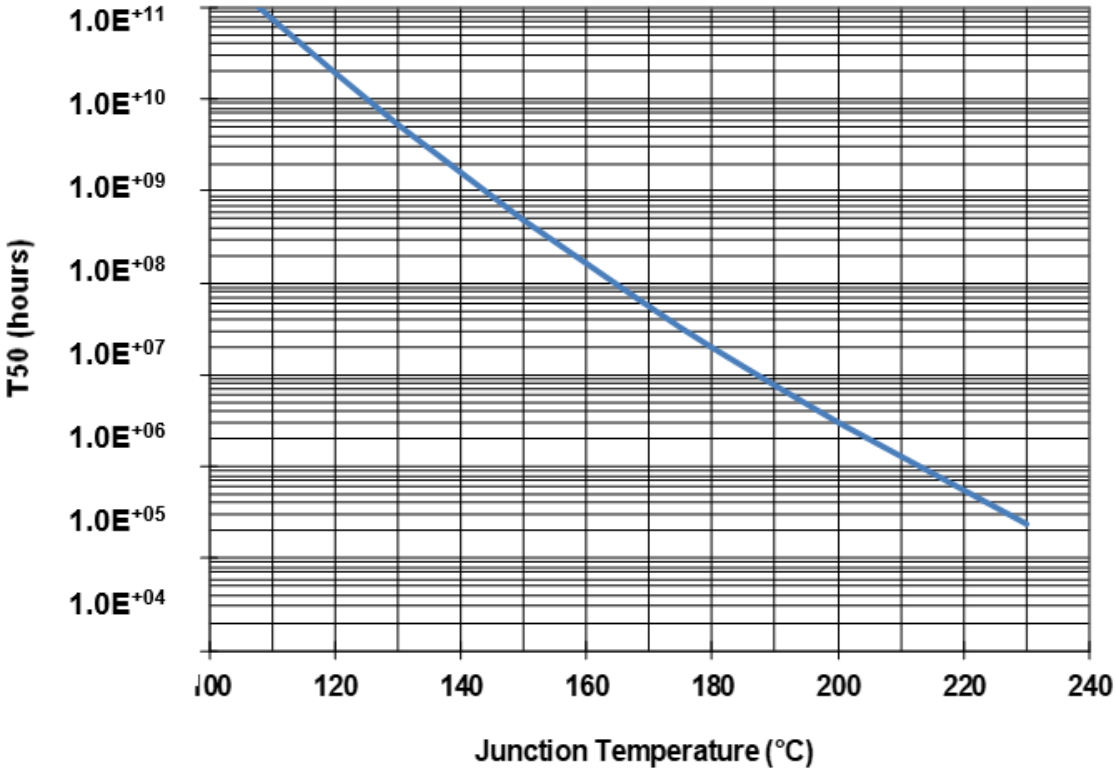
Device thermal information / RX Mode

The device thermal parameters below are based on UMS rules to evaluate the junction temperature.
This same procedure is the basis for junction temperature evaluation of the samples used to derive the median lifetime and activation energy for the particular technology on which the CHC6054-QQA Rx Mode is manufactured (GaAs HEMT 0.15µm).
The temperature T_{case} is defined as the package back-side interface.
The system's maximum temperature must be adjusted in order to guarantee that $T_{junction}$ remains below the maximum value specified in the Absolute Maximum Rating table.
The PCB must be designed to meet this requirement.

Parameter	Biasing conditions	Tjunction (°C)	R_{TH} (°C.mm/W)	T50 (hours)
R_{TH} (1) Thermal Resistance (Junction to Case)	V_d = 4V I_d = 60mA $P_{diss.}$ = 0.24W	103	79	3.6E11

(1) Assuming 85°C T_{case}

Median Life Time versus Junction Temperature



Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

Biasing Procedure

Mode 1 – Tx mode

Device Power Up sequence:

HPA & Switch

1. Ground the device: I_{D12}= 0A
2. Set V_{g12} to -5.0V: I_{D12}= 0A
3. Set V_{d12} to 0V *(pinch off test)* : I_{d12}= 0A
4. Set V_{d12} to 25V *(nominal bias voltage)* : I_{d12}= 0A
5. Set SW to 0V

Driver

1. Set V_{g1d} & V_{d1d} & V_{g2d} & V_{d2d} to 0V *(pinch off test):* I_{dd}= 0A/ I_{gd}= 0A
2. Set V_{g1d} & V_{d1d} & V_{g2d} & V_{d2d} to 4V *(nominal bias voltage):* I_{dd}=130mA/ I_{gd}= 8mA
   To avoid damaging the device, make sure the bias is applied at all 4 biasing points at the same time. Alternatively, drain biasing may be applied first and, then slowly increase V_{g1d} & V_{g2d} up to 4V
3. Increase V_{g12} until the quiescent bias drain current I_{D12} = 40mA is reached
4. Apply RF input signal

Device Power Down sequence:

1. Remove RF input signal
2. Lower V_{g12} down to -5.0V
3. Decrease V_{g1d} & V_{d1d} & V_{g2d} & V_{d2d} down to 0V
   To avoid damaging the device, make sure the bias is applied at all 4 biasing points at the same time. Alternatively, drain biasing may be applied first and, then slowly decrease V_{g1d} & V_{g2d} down to 0V
4. Remove SW
5. Decrease V_{d12} down to 0V

Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

Biasing procedure

Mode 2 – Rx mode

Device Power Up sequence:

HPA & Switch

1. Ground the device
2. Set SW to 20V
3. Set V_{g12} to -5V: I_{d12}= 0A
   V_{d12} = 25V

LNA

1. Set V_{g1L} & V_{dL} to 0V *(pinch off test)*
2. Set V_{g1L} & V_{dL} to 4V *(nominal bias voltage)*
   To avoid damaging the device, make sure the bias is applied at both biasing points at the same time. Alternatively, drain biasing V_{dL} *may be applied first and, then slowly increase* V_{g1L} *up to 4V*
3. Apply RF input signal

Device Power Down sequence:

1. Remove RF input signal
2. Decrease V_{g1L} & V_{dL} down to 0V
   To avoid damaging the device, make sure the bias is applied at both biasing points at the same time. Alternatively, drain biasing V_{dL} *may be applied first and, then slowly decrease* V_{g1L} *down to 0V*
3. Remove SW

Notes:

The testing may begin with either Mode 1 or Mode 2.
In order to minimize DC power consumption, be sure to
- in Mode 2 / Rx mode use:
  set HPA V_{g12} to -5V, decrease V_{d12} to 0V and set V_{g12} to 0V
  set Driver V_{g1d} & V_{d1d} & V_{g2d} & V_{d2d} to 0V
- in Mode 1 / Tx mode use:
  set LNA V_{g1L} & V_{dL} to 0V

CHC6054-QQA device may operate in only one mode at a given instance.

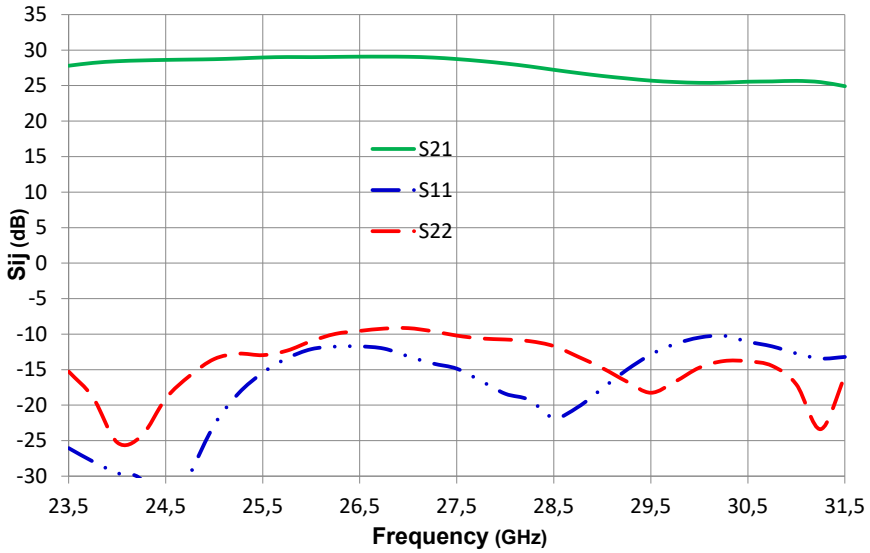
Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

Typical Board Measurements

The performance reported here was measured on the evaluation board at Tamb.= +25°C
Board losses are de-embedded, such that the reported results are for the IC package terminals

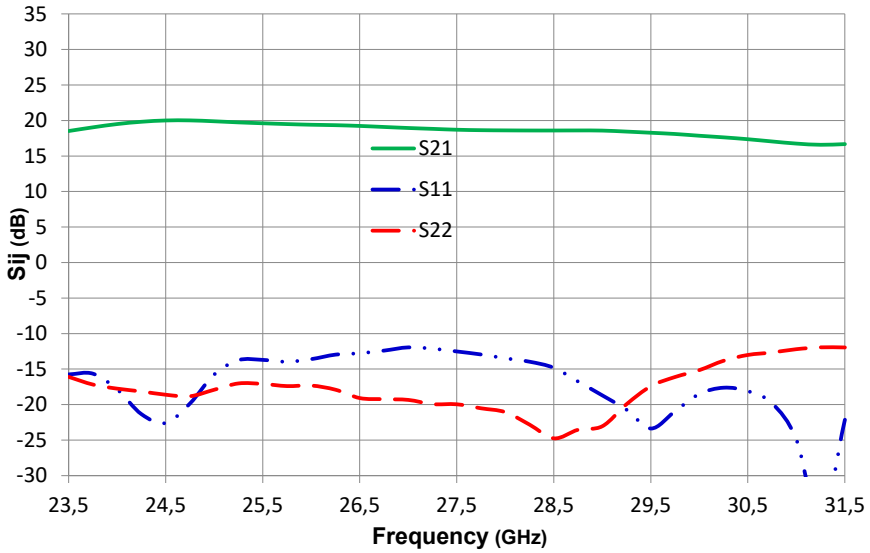
Gain & Return Losses versus Frequency – TX Mode

V_{d12} = +25V, V_{g12} set in order to get I_{d12} = 40mA
SW = 0V, V_{g1L} = V_{dL} =0V, V_{g1d} & V_{d1d} & V_{g2d} & V_{d2d} = 4V



Gain & Return Losses versus Frequency – RX Mode

V_{d12} = +25V, V_{g12} = -5V in order to ged I_{d12} = 0mA
SW = 20V, V_{g1L} = V_{dL} =4V, V_{g1d} & V_{d1d} & V_{g2d} & V_{d2d} = 0V

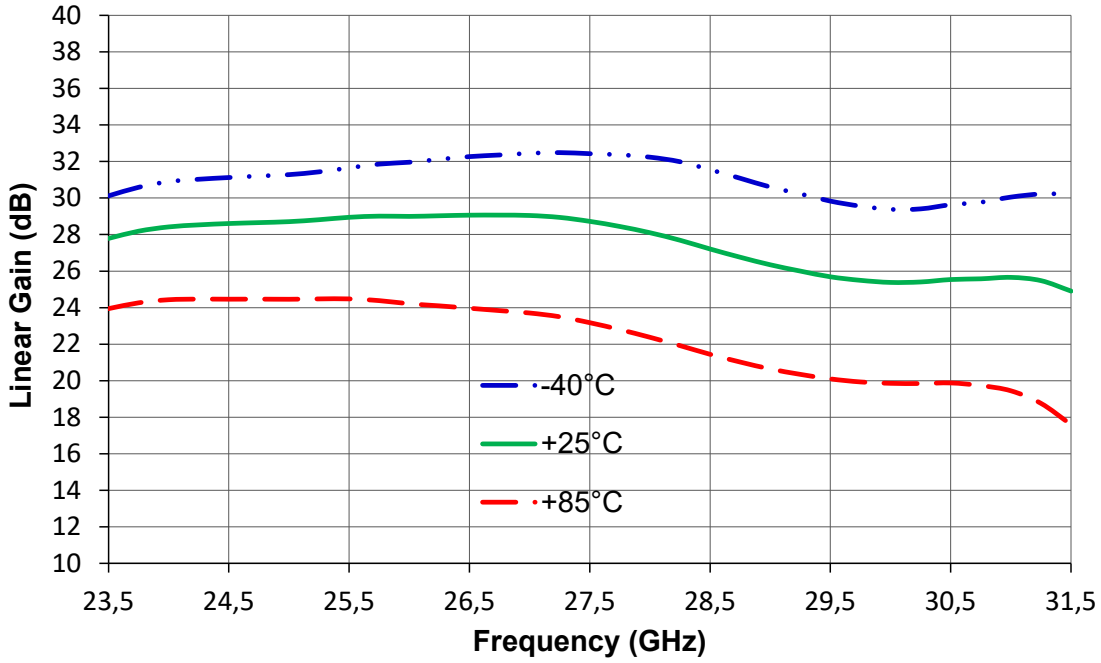


Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

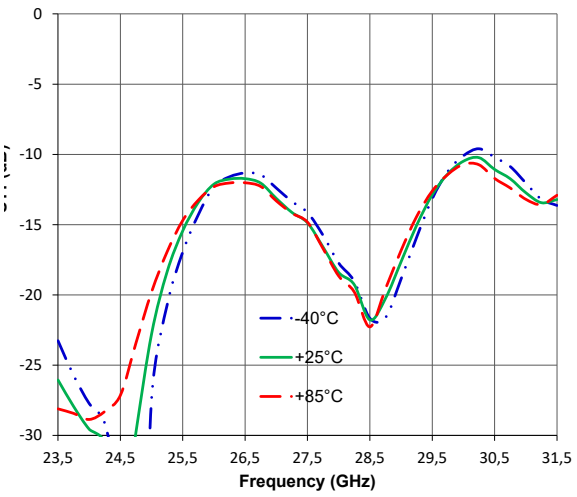
Typical Board Measurements – TX MODE

Tamb.= +25°C, SW = 0V, V_{d12} = 25V, V_{g12} set in order to get I_{d12} = 40mA
V_{g1d} & V_{d1d} & V_{g2d} & V_{d2d} = 4V, V_{g1L} = V_{dL} =0V
Board losses are de-embedded, such that the reported results are for the IC package terminals

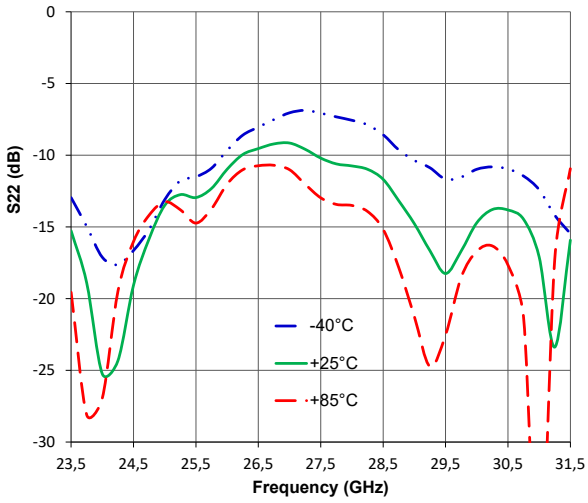
Gain versus Frequency in Temperature



Input Return Losses versus Frequency in Temperature



Output Return Losses versus Frequency In Temperature

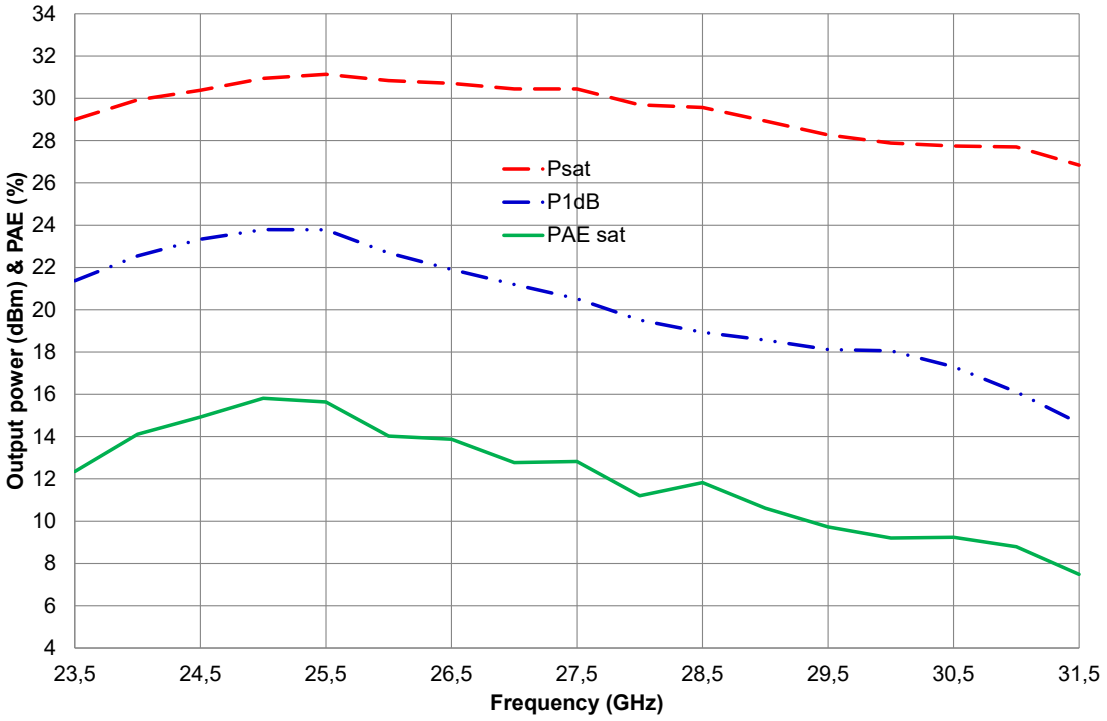


Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

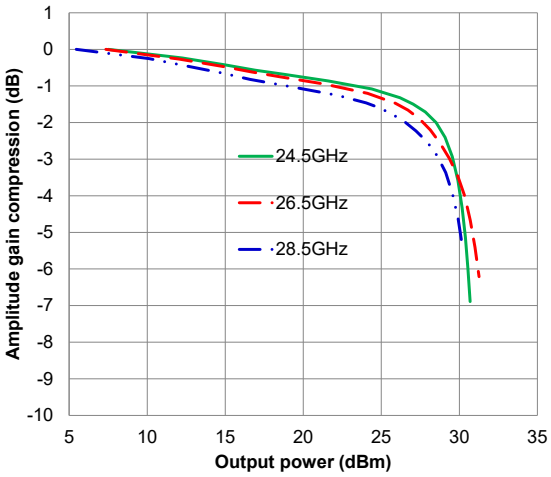
Typical Board Measurements – TX MODE

Tamb.= +25°C, SW = 0V, V_{d12} = 25V, V_{g12} set in order to get I_{d12} = 40mA
V_{g1d} & V_{d1d} & V_{g2d} & V_{d2d} = 4V, V_{g1L} = V_{dL} =0V
Board losses are de-embedded, such that the reported results are for the IC package terminals

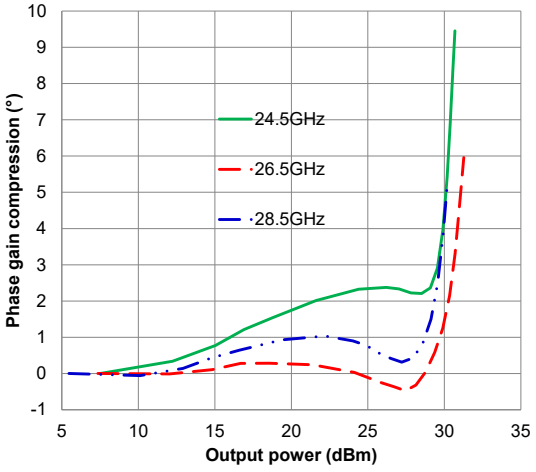
Output Power & PAE versus Frequency



Gain Amplitude versus Output Power



Gain Phase versus Output Power

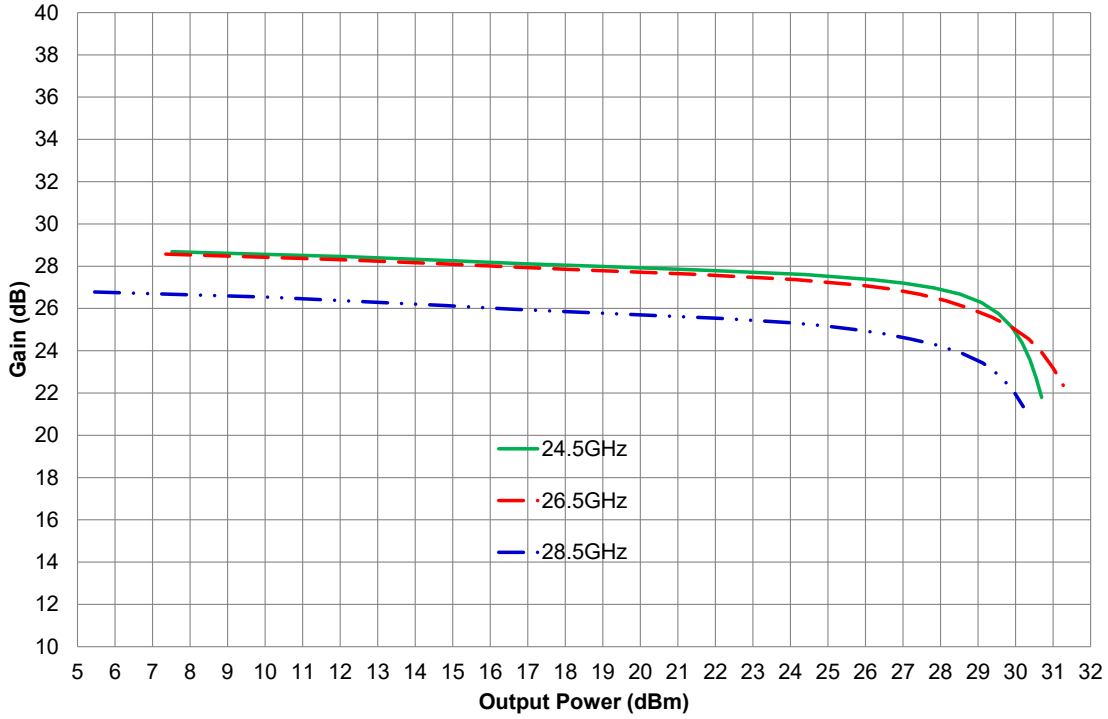


Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

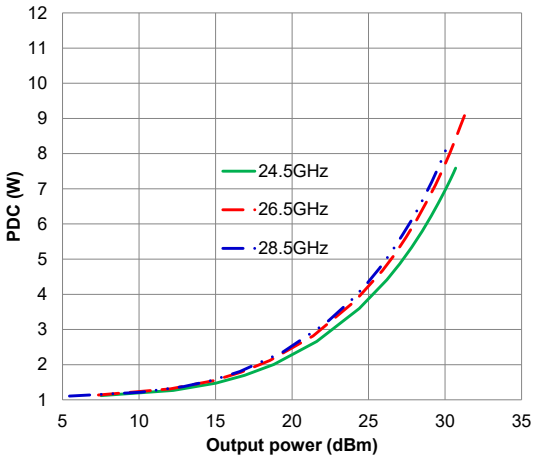
Typical Board Measurements – TX MODE

Tamb.= +25°C, SW = 0V, V_{d12} = 25V, V_{g12} set in order to get I_{d12} = 40mA
V_{g1d} & V_{d1d} & V_{g2d} & V_{d2d} = 4V, V_{g1L} = V_{dL} =0V
Board losses are de-embedded, such that the reported results are for the IC package terminals

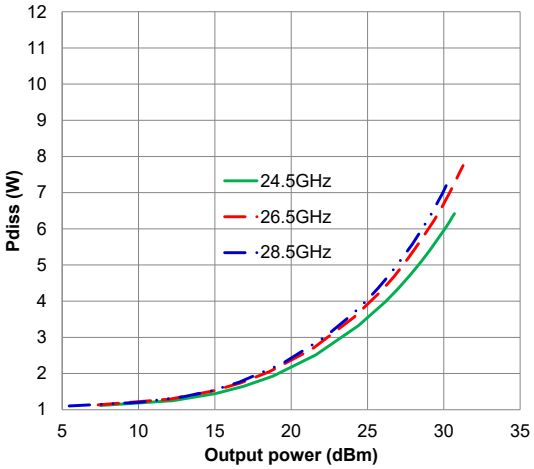
Gain versus Output Power



DC Power Consumption versus Output Power



Dissipated Power versus Output Power

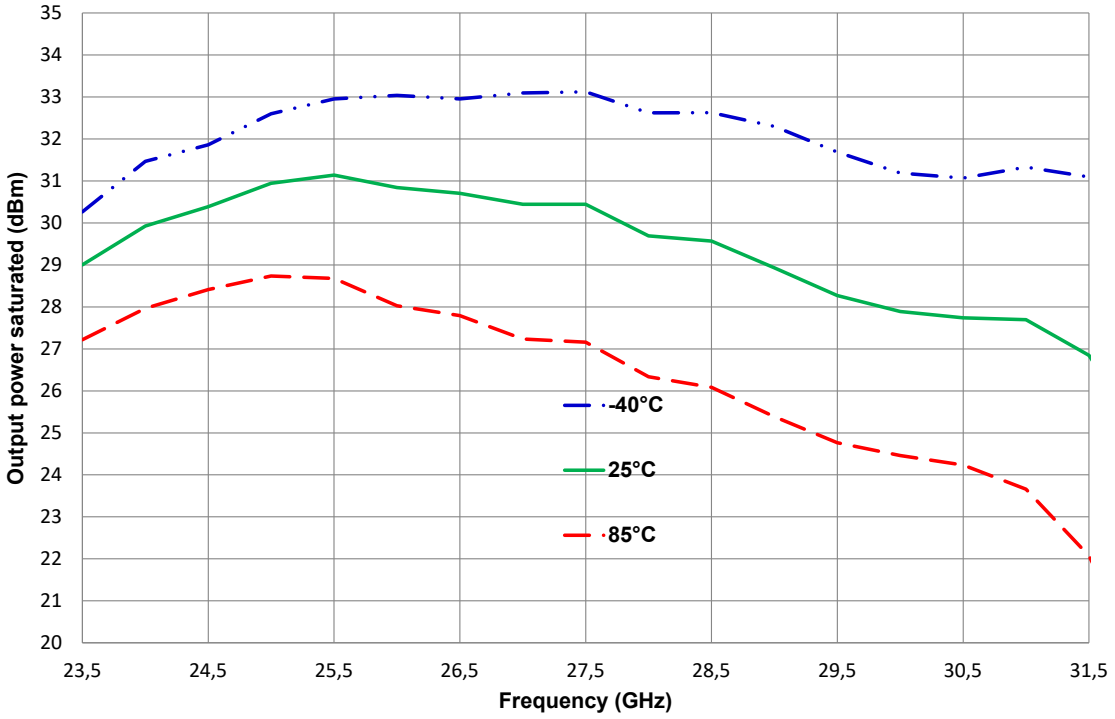


Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

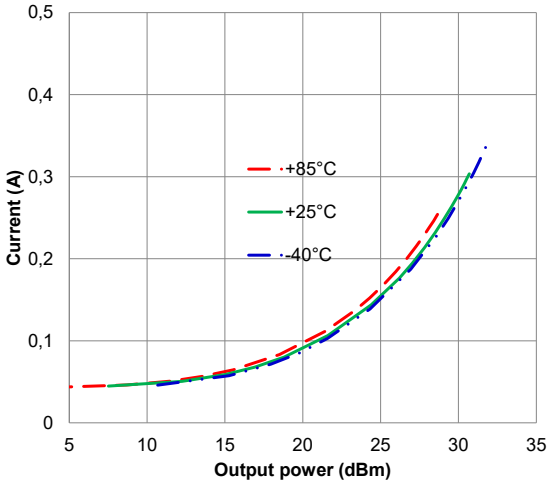
Typical Board Measurements – TX MODE

SW = 0V, V_{d12} = 25V, V_{g12} set in order to get I_{d12} = 40mA
V_{g1d} & V_{d1d} & V_{g2d} & V_{d2d} = 4V, V_{g1L} = V_{dL} =0V
Board losses are de-embedded, such that the reported results are for the IC package terminals

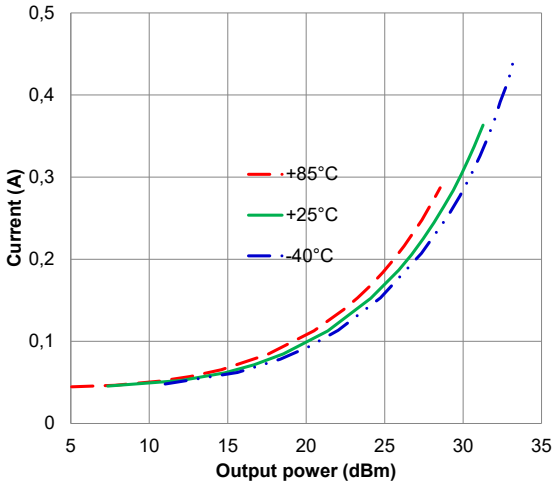
Output Power saturated versus Frequency in Temperature



HPA Drain Current versus Output Power @24.5GHz



HPA Drain Current versus Output Power @26.5GHz

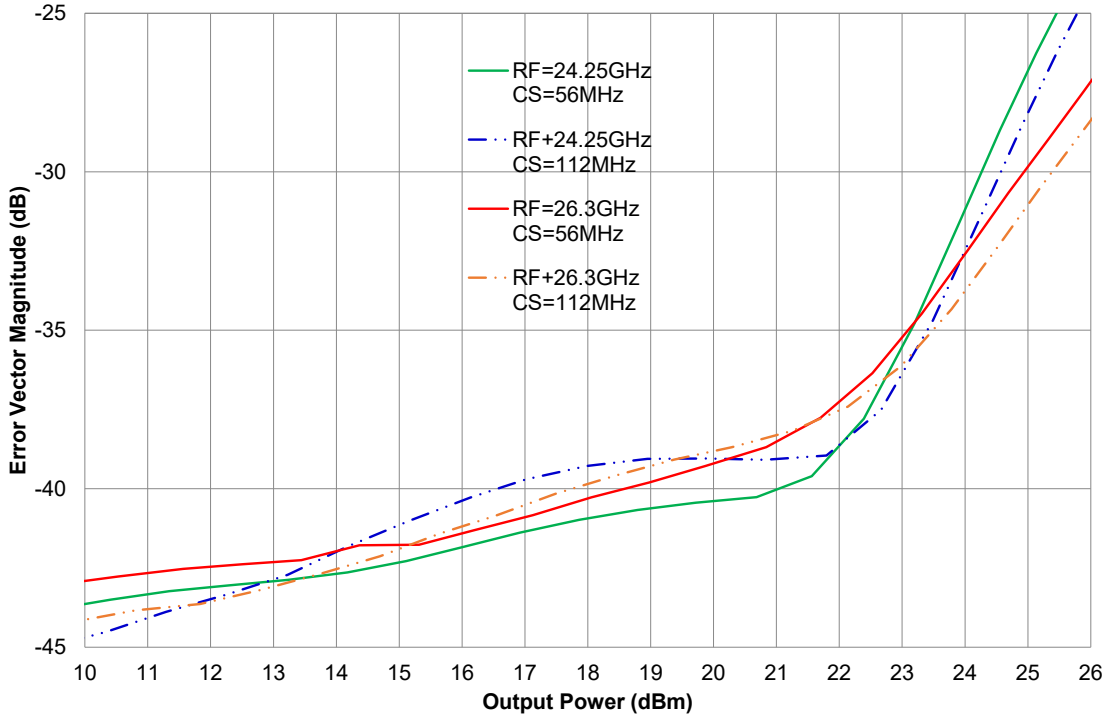


Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

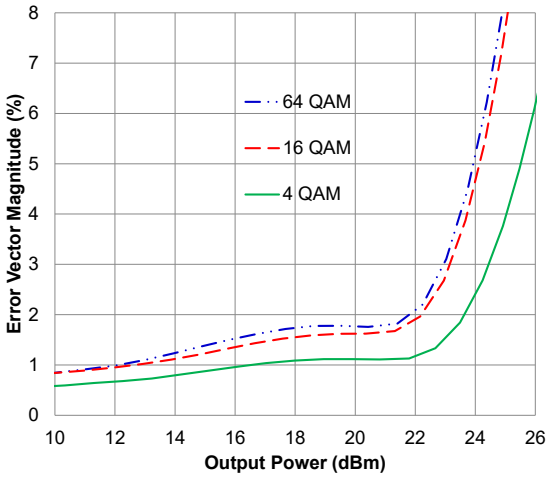
Typical Board Measurements – TX MODE

Tamb.= +25°C, SW = 0V, V_{d12} = 25V, V_{g12} set in order to get I_{d12} = 40mA
V_{g1d} & V_{d1d} & V_{g2d} & V_{d2d} = 4V, V_{g1L} = V_{dL} =0V ; QAM Modulation **without DPD**
Board losses are de-embedded, such that the reported results are for the IC package terminals

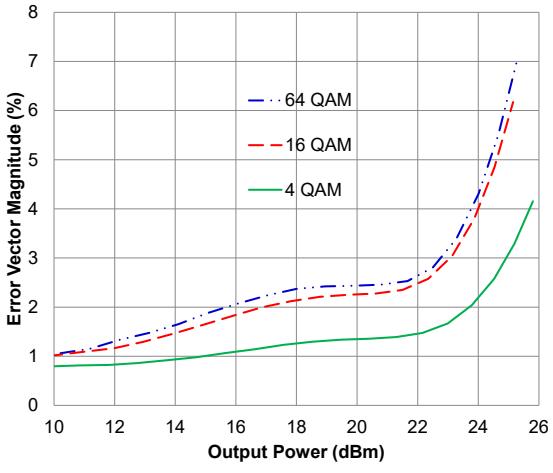
Error Vector Magnitude versus Output Power
RF_Freq = 24.25 & 26.3GHz ; Channel Spacing =56 & 112MHz, 4QAM



Error Vector Magnitude (%) versus Output Power @24.25GHz
Channel Spacing =112MHz



Error Vector Magnitude (%) versus Output Power @28.35GHz
Channel Spacing =112MHz

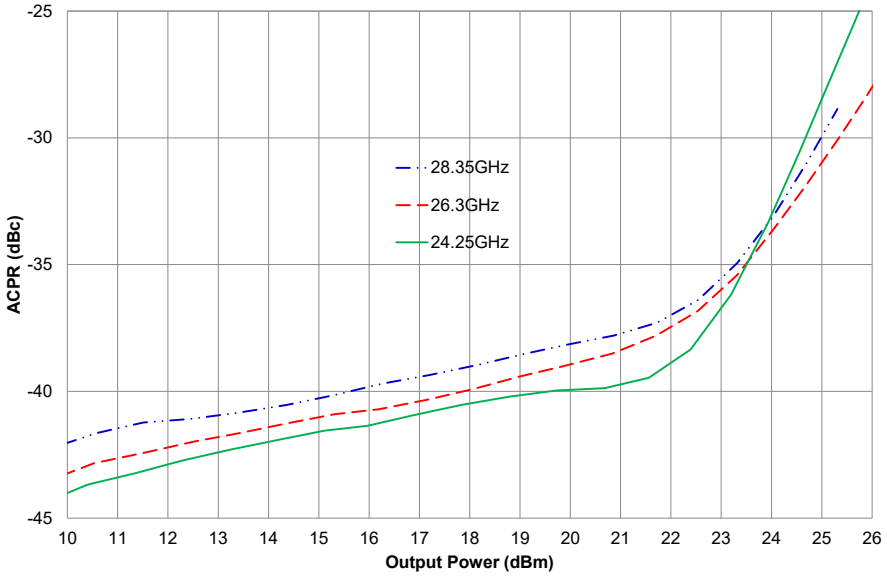


Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

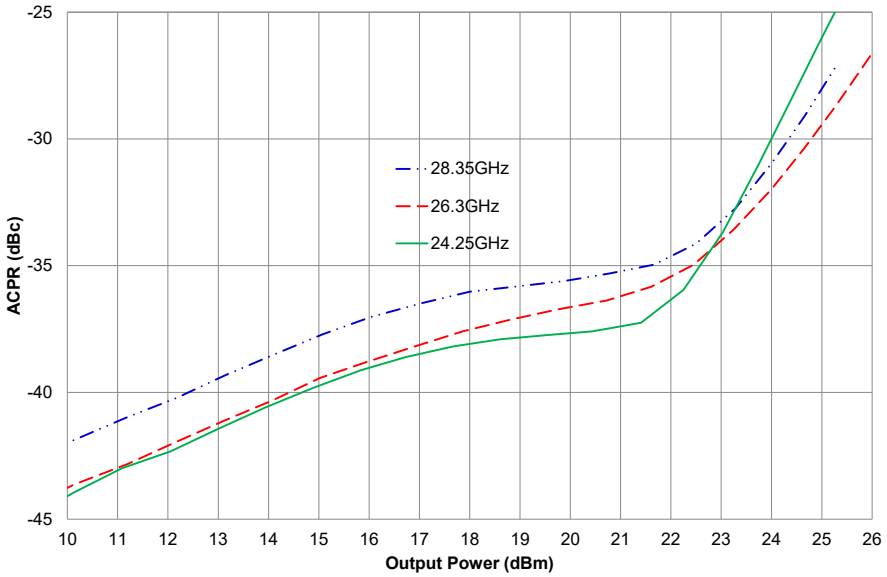
Typical Board Measurements – TX MODE

Tamb.= +25°C, SW = 0V, V_{d12} = 25V, V_{g12} set in order to get I_{d12} = 40mA
V_{g1d} & V_{d1d} & V_{g2d} & V_{d2d} = 4V, V_{g1L} = V_{dL} =0V ; QAM Modulation **without DPD**
Board losses are de-embedded, such that the reported results are for the IC package terminals

ACPR versus Output Power and RF Frequency
Channel Spacing =56MHz, 4QAM



ACPR versus Output Power and RF Frequency
Channel Spacing =112MHz, 64QAM

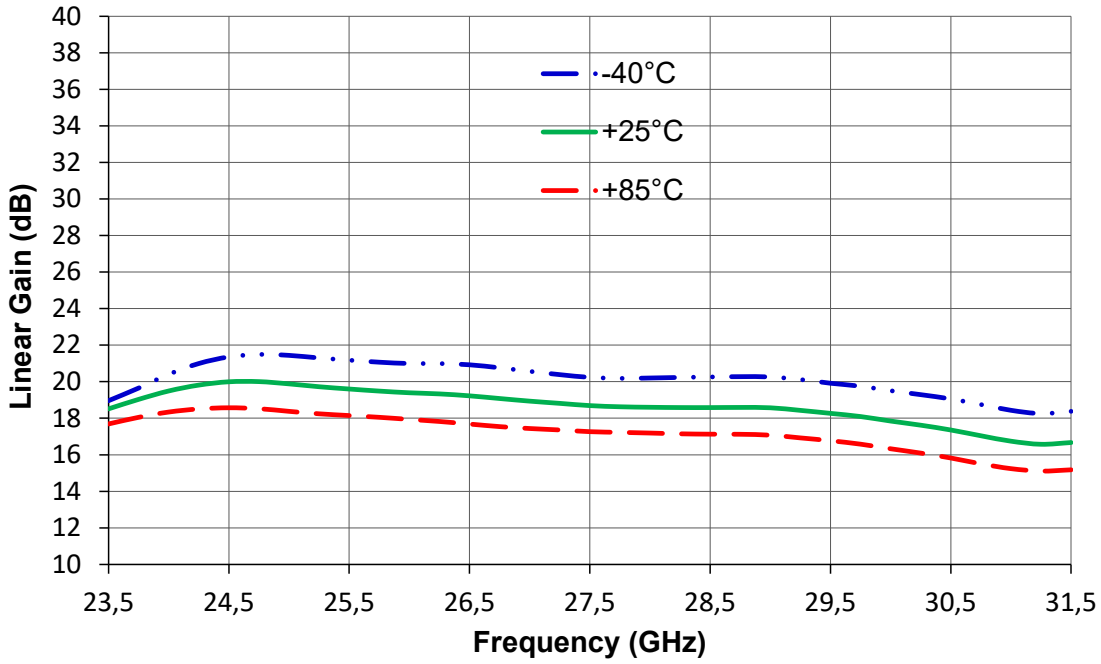


Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

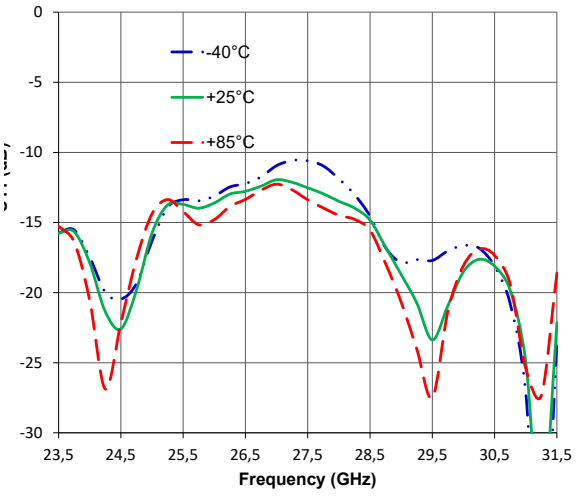
Typical Board Measurements – RX MODE

SW = +20V, V_{d12} = 25V, V_{g12} = -5V in order to get I_{d12} = 0mA
V_{g1d} & V_{d1d} & V_{g2d} & V_{d2d} = 0V, V_{g1L} = V_{dL} =4V
Board losses are de-embedded, such that the reported results are for the IC package terminals

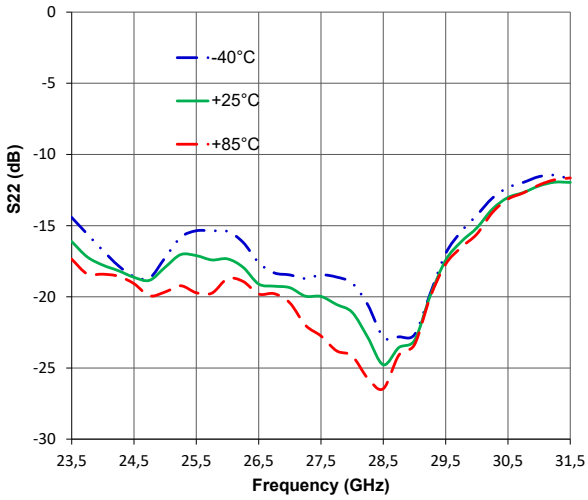
Gain versus Frequency in Temperature



Input Return Losses versus Frequency In Temperature



Output Return Losses versus Frequency In Temperature

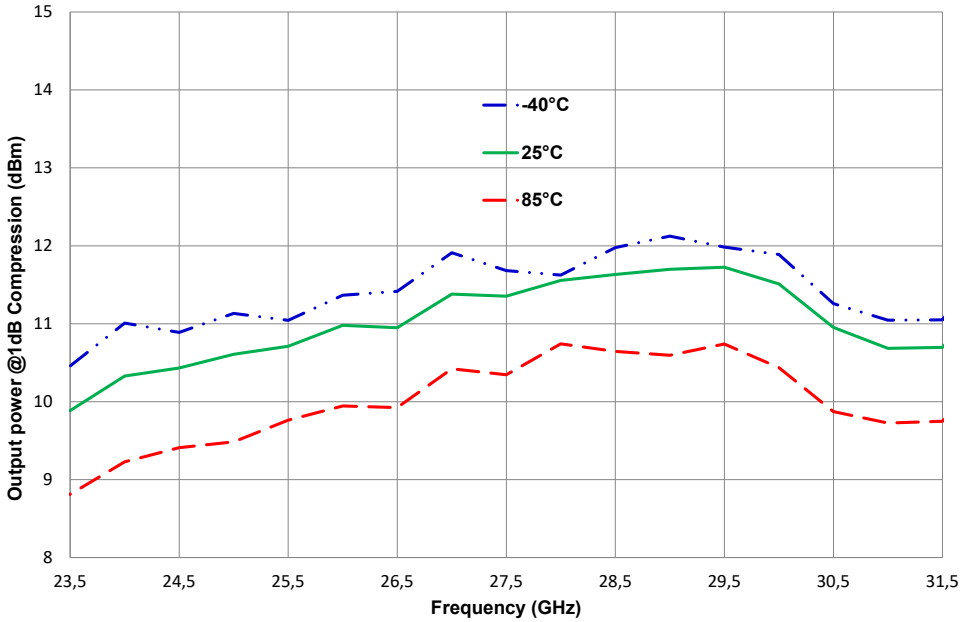


Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

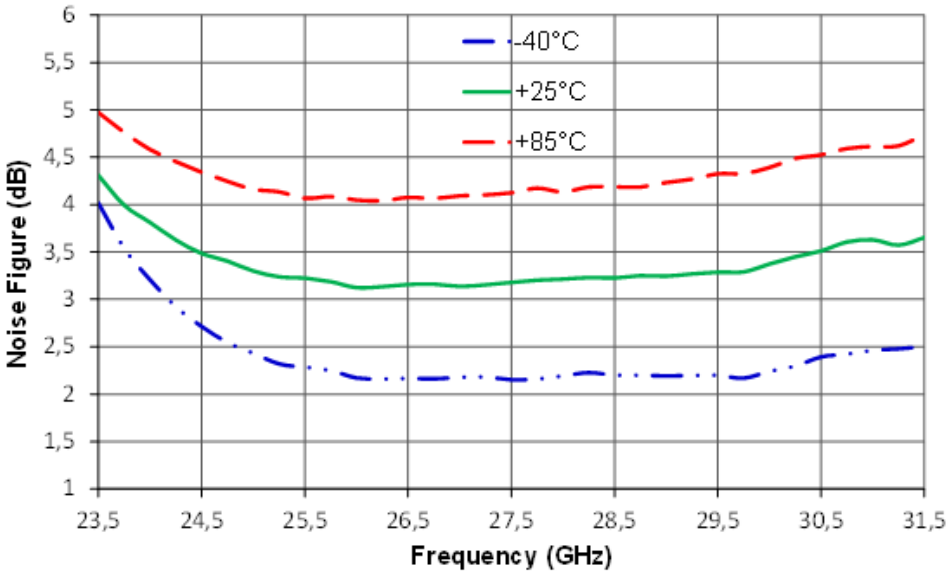
Typical Board Measurements – RX Mode

SW = +20V, V_{d12} = 25V, V_{g12} = -5V in order to get I_{d12} = 0mA
V_{g1d} & V_{d1d} & V_{g2d} & V_{d2d} = 0V, V_{g1L} = V_{dL} =4V
Board losses are de-embedded, such that the reported results are for the IC package terminals

Output Power at 1dB compression versus Frequency in Temperature

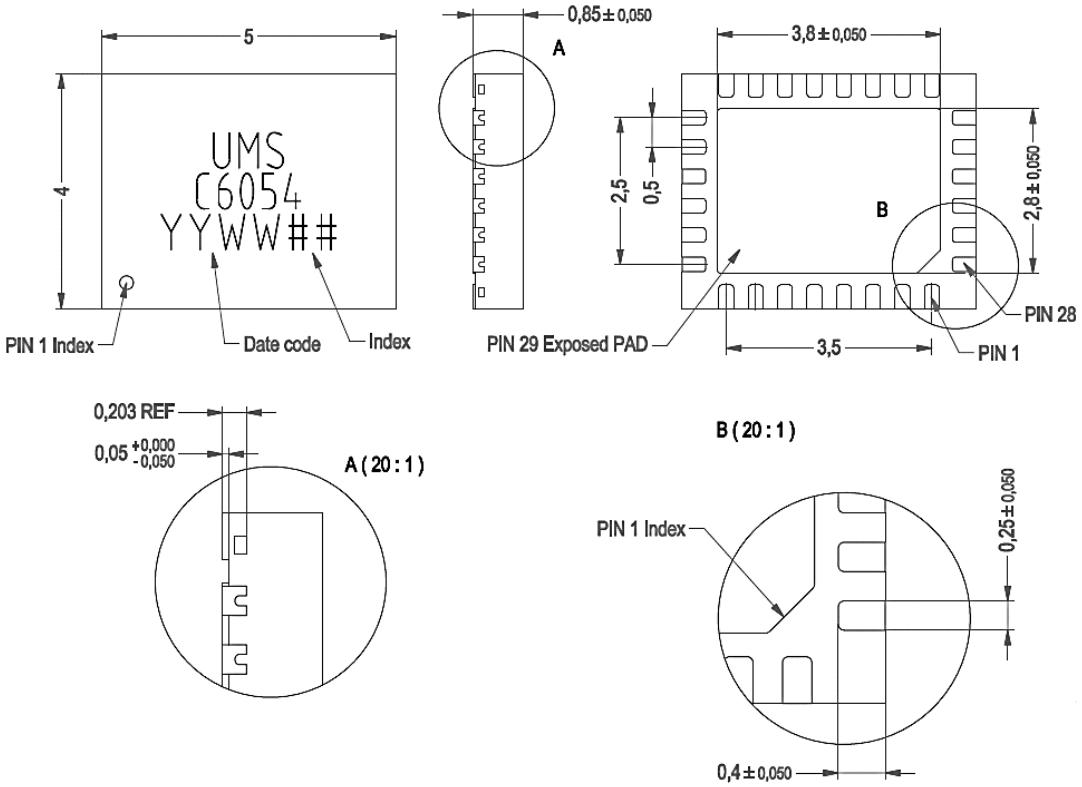


Noise Figure versus Frequency in Temperature



Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

Package outline (1)



Matte tin, Lead Free (Green)	1- GND(2)	11- GND(2)	21- Vg12
Units : mm	2- Nc	12- GND(2)	22- Vd12
From the standard : JEDEC MO-220	3- SW	13- Input TX	23- GND(2)
	4- GND(2)	14- GND(2)	24- Nc
(VGGD)	5- Vg1L	15- Vg1d	25- GND(2)
29- GND	6- VdL	16- Vd1d	26- GND(2)
	7- GND(2)	17- Vg2d	27- Common
	8- Nc	18- Vd2d	28- GND(2)
	9- GND(2)	19- GND(2)	
	10- Output RX	20- GND(2)	

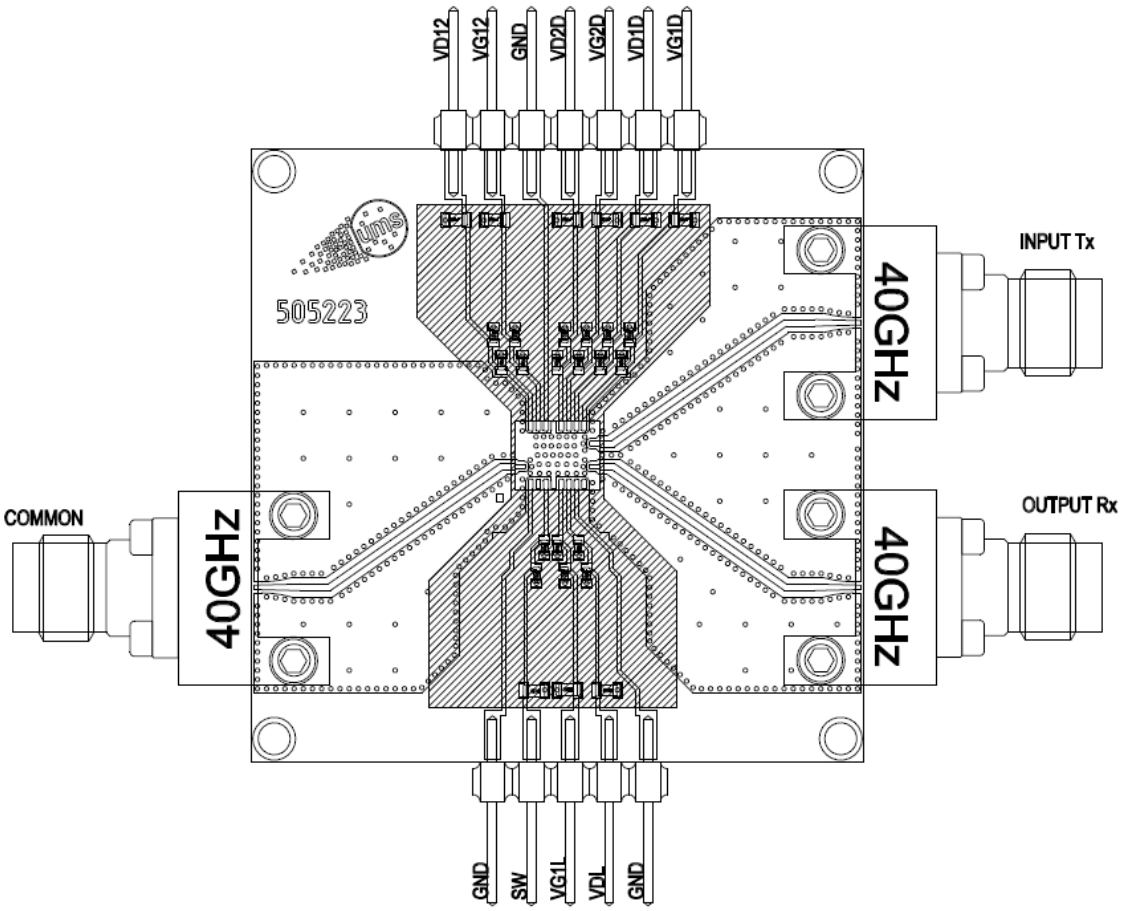
(1) The package outline drawing included to this document is given for indication. Refer to the application note AN0017 (https://www.ums-rf.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “GND” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

Evaluation board

Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors: 100pF ±5%, 10nF ±10% and 1µF ±10% are recommended for all DC accesses.
- See application note AN0017 for details.



Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.

Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

ESD Notes

ESD – Human Body Model (HBM)
Class 1A / 250 volts to < 500 volts (1) (2)

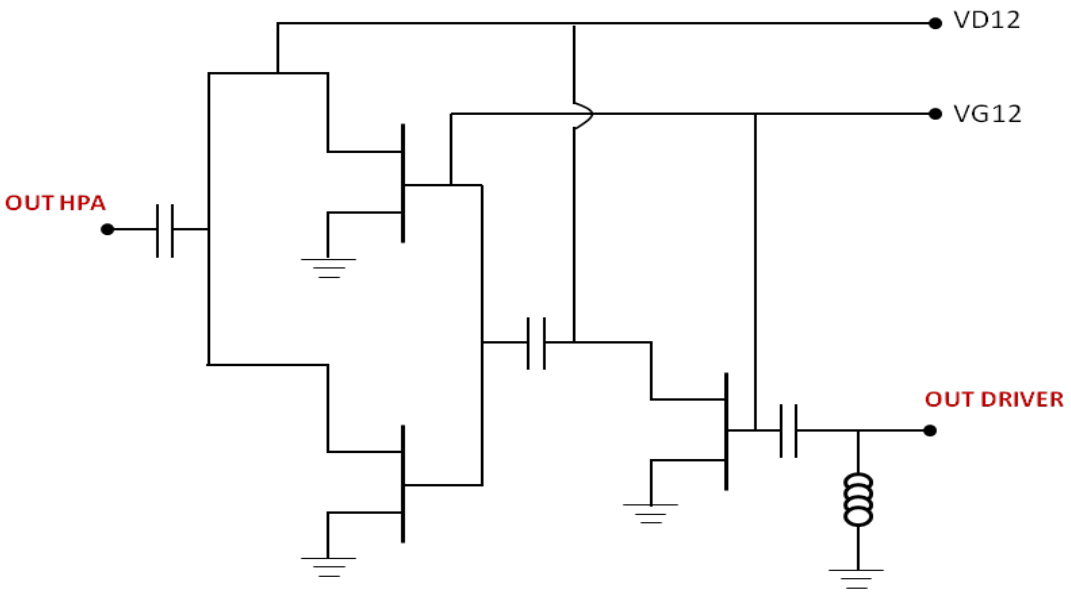
ESD – Machine Model (MM)
Class M1 / < 100 volts (1)
Class M2 / 100 volts up to 200 volts (2)

(1) from pin #22 (V_{d12}) ESDA / JEDEC JESD22-A114
(2) from pin #10 (Output_RX) ESDA / JEDEC JESD22-A115

The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (100pF mandatory and 10nF & 1µF if possible) on the PC board, as close as possible to the package.

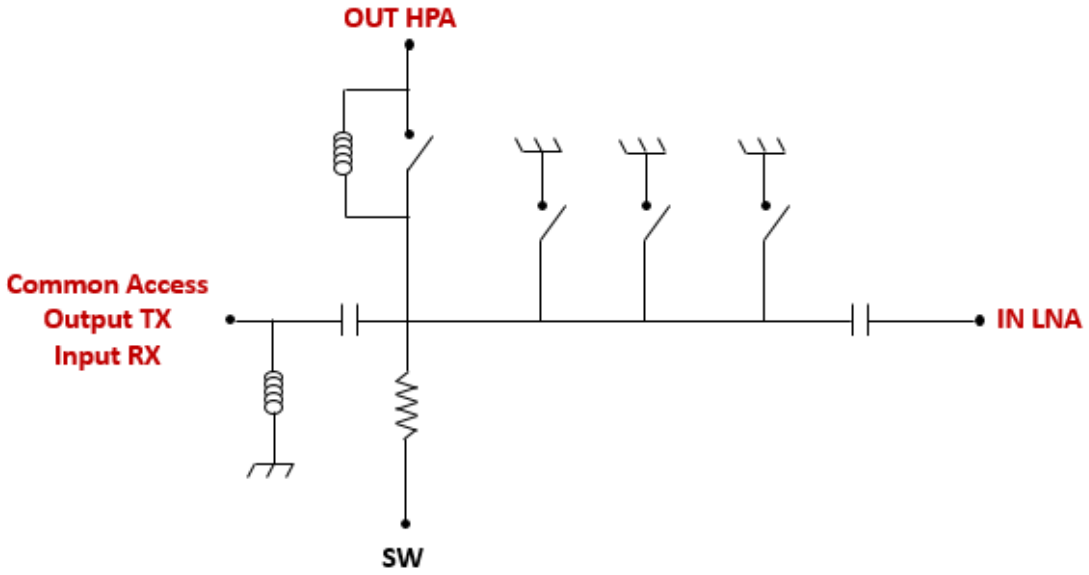
Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

HPA DC Schematic



V_{g12} # -3.1V, V_{d12} = 25V, I_{d12} = 40mA

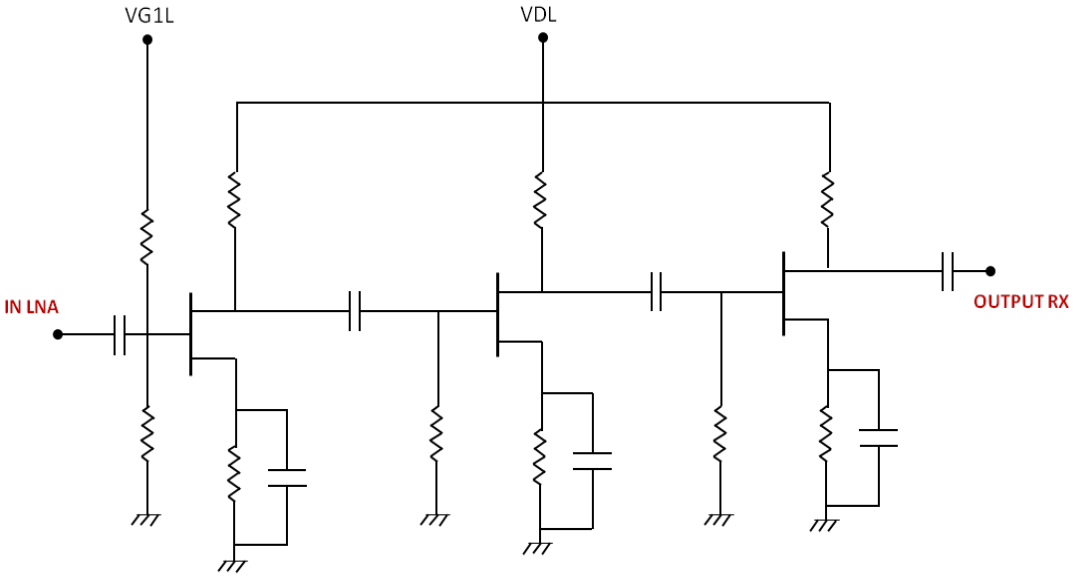
Switch DC Schematic



TX mode: SW = 0V
RX mode: SW = +20V

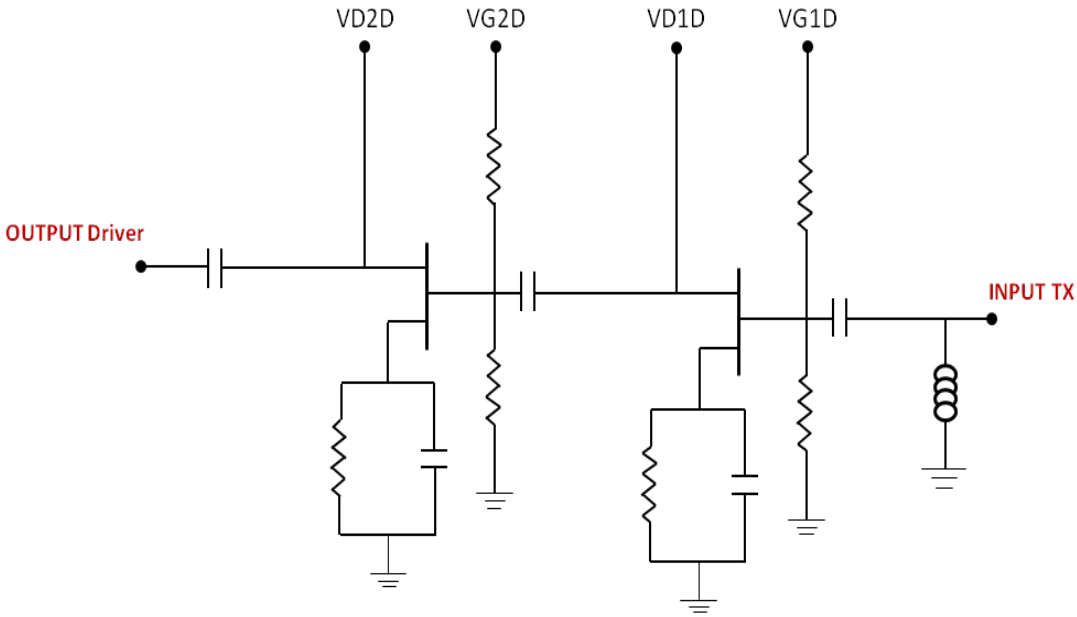
Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

LNA DC Schematic



V_{g1L} = 4V, V_{dL} = 4V, I_{dL} = 60mA

Driver DC Schematic



V_{d1d} = V_{d2d} = 4V, V_{g1d} = V_{g2d} = 4V, I_{dd} = 130mA

Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com

Recommended package footprint

Refer to the application note AN0017 available at https://www.ums-rf.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017 at https://www.ums-rf.com.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x5 package:	CHC6054-QQA/XY	
	Stick: XY = 20	Tape & reel: XY = 21

Bât. Charmille - Parc Mosaic - 10, Avenue du Québec - 91140 VILLEBON-SUR-YVETTE - France
Tel.: +33 (0) 1 69 86 32 00 - Fax: +33 (0) 1 69 86 34 34 - www.ums-rf.com