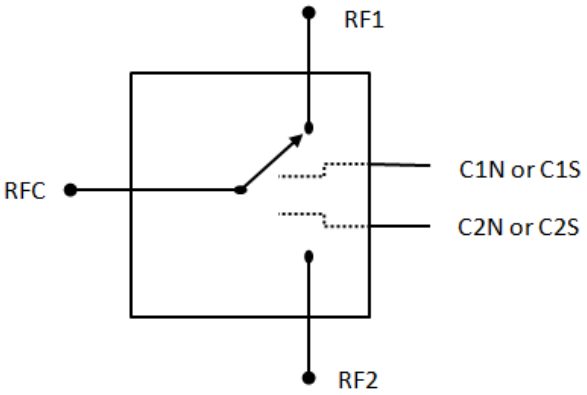
6-18GHz Reflective SPDT

GaN Monolithic Microwave IC

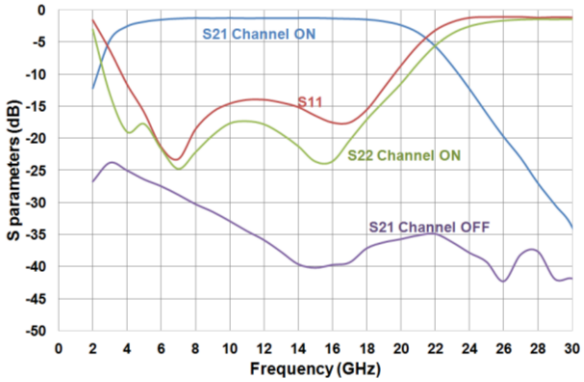
Description

The CHS8618-99F is a monolithic FET based reflective switch in the 6-18GHz frequency band.
It is designed for a wide range of applications, from military to commercial communication systems.
It is developed on a robust 0.25µm gate length GaN/SiC HEMT process and is available as bare die.



Main Features

- Broadband performances: 6-18GHz
- Insertion Loss: 1.3dB
- Isolation: 34dB
- Input power at 1dB IL compression: 42dBm
- Switching time: 30ns
- Control: -25V / 0V
- Chip size 1.65x2.18x0.1mm



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	6		18	GHz
IL	On state insertion loss		1.3		dB
ISOL	Off state isolation		34		dB
Ton / Toff	Switching time 50% control to 90% RF, and 50% control to 10% RF		30		ns

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Electrical Characteristics (1)

Tamb.= +25°C, VL = -25V / VH = 0V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	6		18	GHz
IL	On state insertion loss		1.3		dB
ΔIL/ΔT	Variation rate of insertion loss with temperature		-0.007		dB/°C
ISOL	Off state isolation		34		dB
RL_RFC_ON	On state return losses on RFC access		16		dB
RL_RFi_ON	On state return losses on RF1 or RF2 access		20		dB
RL_OFF	Off state output return losses		2.5		dB
VH	Control voltage high level		0		V
VL	Control voltage low level		-25		V
IP1dB	Input Power @1dB gain compression.		42		dBm
Ton / Toff	Switching time (2) 50% control to 90% RF, and 50% control to 10% RF		30		ns
Ic	Consumption on the control supply voltage at 1dB gain compression		0.5		mA

(1) These values are representative of measurements done in test fixture with a bonding wire of typically 0.35 to 0.4nH. Reference planes of on-board measurements are defined in the paragraph S-parameters reference planes

(2) for RF power up to Pin=40dBm

SPDT truth table

PAD C1N or C1S	PAD C2N or C2S	Electrical path RFC to RF1	Electrical path RFC to RF2
VH	VL	ON	OFF
VL	VH	OFF	ON

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
VL	Control voltage low level	-40	V
Pin	Maximum peak input power overdrive	42.7	dBm
Tj	Junction temperature	230	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Temperature Range

Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

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Typical on-wafer Sij parameters

Tamb.= +25°C, C1N/C1S = 0V, C2N/C2S = -25V, on-state RFC-RF1 path

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
1	-0.2	-34.0	-29.7	-167.7	-29.7	-168.0	-0.3	-41.0
2	-1.4	-73.7	-12.3	147.7	-12.3	147.7	-2.7	-91.7
3	-6.2	-108.4	-4.5	85.5	-4.5	85.5	-12.5	-137.2
4	-11.1	-112.8	-2.4	37.5	-2.4	37.5	-17.4	-75.7
5	-13.6	-112.9	-1.7	3.9	-1.7	3.8	-14.7	-92.6
6	-16.0	-111.8	-1.4	-23.0	-1.4	-23.0	-15.9	-122.0
7	-18.1	-101.0	-1.2	-46.5	-1.2	-46.4	-19.1	-161.1
8	-17.8	-82.2	-1.2	-67.8	-1.1	-67.6	-22.3	136.9
9	-15.7	-75.3	-1.2	-87.7	-1.1	-87.6	-20.0	70.2
10	-13.8	-76.8	-1.3	-106.5	-1.2	-106.6	-16.6	30.1
11	-12.0	-83.2	-1.3	-125.1	-1.3	-125.2	-14.1	2.2
12	-11.0	-91.8	-1.5	-143.1	-1.4	-143.8	-12.7	-21.2
13	-9.7	-98.4	-1.6	-159.6	-1.6	-160.1	-11.2	-46.8
14	-9.3	-110.4	-1.6	-177.8	-1.5	-178.2	-11.1	-71.6
15	-9.2	-120.1	-1.6	164.6	-1.6	164.3	-11.1	-96.6
16	-10.2	-127.5	-1.5	144.4	-1.5	144.6	-12.0	-132.2
17	-11.5	-126.5	-1.6	122.9	-1.5	123.1	-14.2	-176.2
18	-12.0	-115.8	-1.9	99.6	-1.7	99.4	-15.0	115.7
19	-10.2	-100.2	-2.4	74.1	-2.2	73.3	-11.3	48.4
20	-6.8	-97.4	-3.7	44.8	-3.5	43.4	-7.7	-0.1
21	-3.4	-109.1	-6.1	19.0	-5.9	16.9	-5.8	-36.7
22	-1.8	-126.7	-8.9	-0.6	-9.1	-2.8	-4.3	-61.7
23	-1.2	-141.6	-11.5	-18.1	-11.6	-19.6	-3.0	-87.8
24	-0.9	-153.7	-14.1	-36.0	-14.3	-36.2	-2.5	-112.1
25	-0.8	-163.9	-17.2	-51.6	-17.2	-52.3	-2.6	-133.1
26	-0.7	-173.1	-20.4	-64.3	-20.3	-65.3	-2.6	-152.4
27	-0.7	178.6	-23.4	-76.4	-23.3	-77.4	-3.1	-169.3
28	-0.7	170.8	-26.7	-88.9	-26.7	-91.5	-3.7	177.9
29	-0.7	163.6	-30.2	-105.6	-30.0	-107.6	-4.7	162.6
30	-0.7	156.9	-37.8	-136.9	-37.8	-136.0	-5.5	148.2
31	-0.7	150.5	-49.5	-170.4	-49.0	-174.4	-7.1	141.0
32	-0.7	144.3	-47.1	77.6	-47.5	75.8	-9.3	138.3
33	-0.7	138.3	-43.2	53.2	-43.7	48.9	-9.6	146.1
34	-0.7	132.2	-38.8	47.5	-39.1	42.9	-8.7	150.1
35	-0.7	126.1	-37.6	22.3	-37.6	18.3	-8.8	153.1
36	-0.6	120.0	-36.8	27.4	-37.6	32.9	-6.3	154.0

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Typical on-wafer Sij parameters

Tamb.= +25°C, C1N/C1S = -25V, C2N/C2S = 0V, off-state RFC-RF1 path

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
1	-0.2	-34.0	-38.8	130.8	-38.6	131.4	-0.1	-38.3
2	-1.5	-73.6	-27.3	75.1	-27.3	75.0	-0.4	-72.2
3	-5.8	-107.7	-24.4	17.2	-24.4	16.9	-0.8	-100.3
4	-10.3	-113.0	-25.5	-25.6	-25.6	-25.5	-1.1	-122.4
5	-14.5	-115.5	-26.7	-47.7	-26.7	-47.5	-1.4	-140.5
6	-17.0	-97.2	-27.9	-65.7	-27.9	-65.2	-1.5	-155.6
7	-19.3	-83.5	-29.4	-74.7	-29.4	-74.1	-1.7	-169.0
8	-16.6	-81.1	-30.6	-96.2	-30.5	-95.6	-1.9	-179.9
9	-13.4	-81.8	-32.6	-96.3	-32.5	-95.7	-2.0	169.5
10	-11.6	-85.5	-31.9	-96.6	-31.8	-95.8	-2.3	160.9
11	-12.8	-86.1	-32.6	-92.7	-32.4	-91.8	-2.2	151.6
12	-10.7	-105.7	-27.1	-113.6	-26.9	-112.8	-2.4	142.4
13	-10.4	-104.6	-31.5	-175.6	-31.4	-175.1	-2.5	140.0
14	-10.7	-100.1	-33.1	-143.1	-32.8	-142.3	-2.3	129.7
15	-13.2	-118.5	-38.6	138.8	-38.5	138.9	-2.4	124.8
16	-10.6	-133.5	-38.9	-153.8	-38.7	-151.8	-2.4	116.1
17	-9.8	-111.4	-36.9	-125.1	-36.4	-124.8	-2.4	110.6
18	-8.4	-107.4	-32.8	-146.4	-32.5	-145.8	-2.5	103.0
19	-10.6	-110.8	-34.5	162.3	-34.0	161.5	-2.7	96.2
20	-8.0	-109.0	-39.0	-59.9	-38.9	-61.4	-3.1	88.6
21	-3.7	-109.5	-29.9	-165.4	-29.2	-167.4	-3.5	85.4
22	-2.0	-125.4	-35.3	152.6	-34.8	151.4	-3.8	83.3
23	-1.3	-141.4	-34.9	149.9	-34.7	145.2	-3.3	81.1
24	-0.9	-153.4	-36.7	139.5	-36.3	137.4	-2.9	75.2
25	-0.8	-163.6	-36.9	133.6	-36.8	131.1	-2.8	67.9
26	-0.7	-172.9	-38.0	123.4	-37.4	121.8	-2.8	62.5
27	-0.7	178.5	-39.8	120.7	-39.4	118.0	-2.7	56.1
28	-0.7	170.8	-41.1	117.0	-40.6	114.0	-2.8	49.7
29	-0.7	163.6	-41.9	127.8	-42.2	117.9	-2.9	44.2
30	-0.7	156.9	-41.1	123.3	-41.3	115.3	-2.8	38.0
31	-0.7	150.5	-41.9	121.1	-42.4	119.8	-2.9	32.3
32	-0.7	144.3	-41.8	128.3	-41.9	127.5	-2.8	25.7
33	-0.7	138.2	-40.4	128.4	-40.4	130.2	-2.9	17.9
34	-0.7	132.3	-40.1	119.4	-40.9	116.9	-3.2	11.4
35	-0.7	126.2	-41.8	97.1	-42.2	97.8	-3.3	4.8
36	-0.6	120.0	-42.9	111.6	-44.1	110.9	-3.4	-2.5

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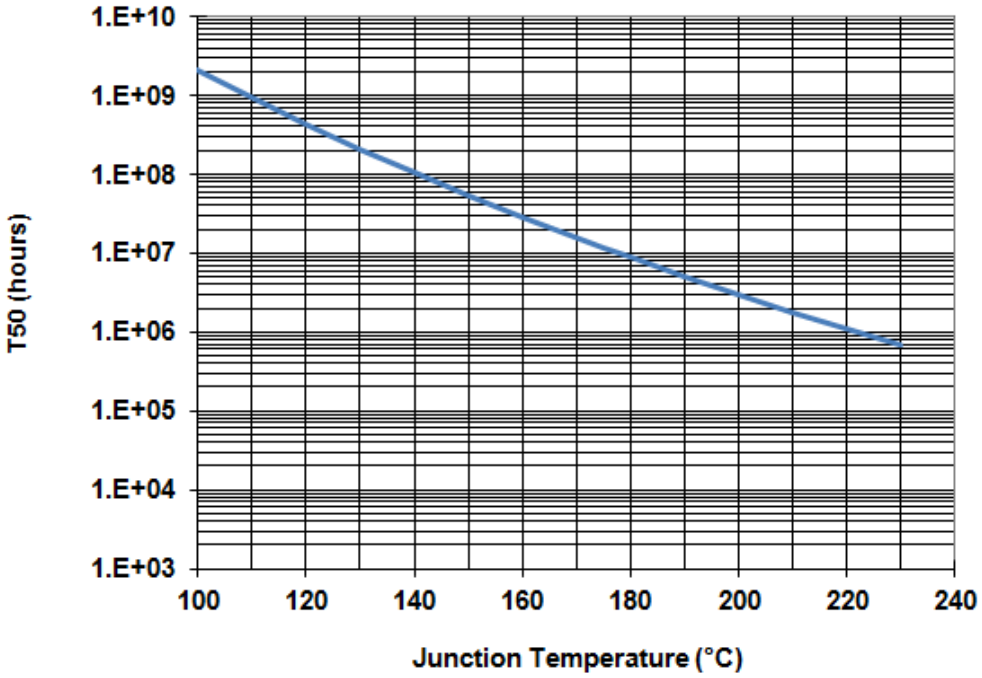
Device thermal information

The device thermal performances given below are based on UMS rules to evaluate the junction temperature.
This same procedure is the basis for junction temperature evaluation of the samples used to derive the Median lifetime and activation energy for the particular technology on which the CHS8618-99F is fabricated (GaN Power HEMT 0.25µm).
The temperature Tb is defined as the chip back side temperature
The thermal resistance (Rth_eq) is given for the full circuit, and assumes CW operation mode.

Thermal Resistance(1)	Rth_eq	Tb=85°C, VH=0V/VL=-25V, Pin=16.6W Pout=9.8W **Pdiss=6.8W CW**	17.0	°C/W
Junction Temperature	Tj		200	°C
Median Life	T50		$2.94x10^6$	Hrs

(1) Thermal analysis is highly recommended, more details are available on request.

Median Life Time versus Junction Temperature



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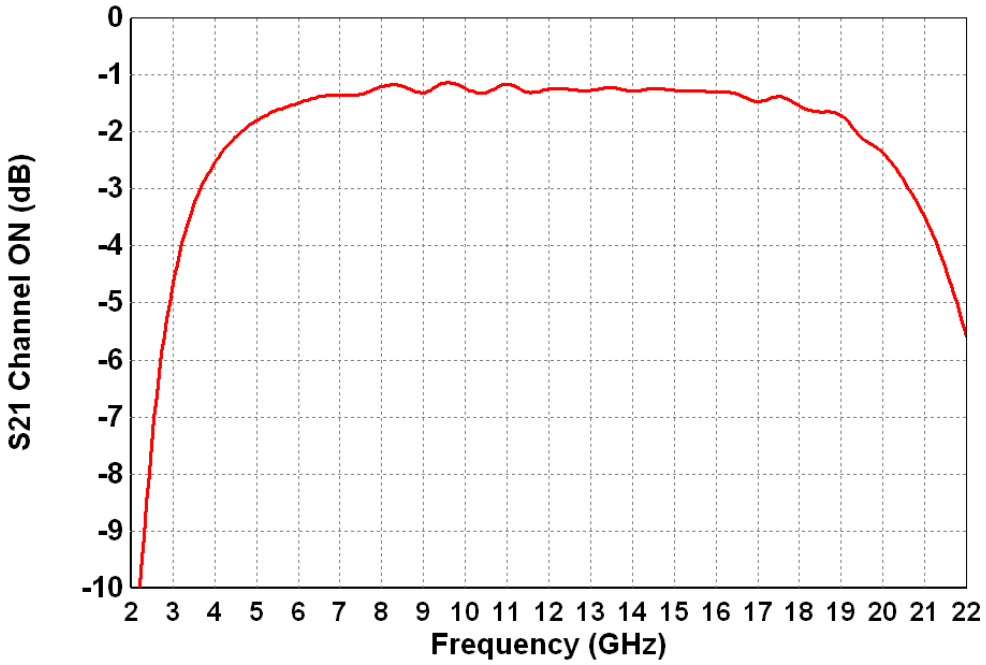
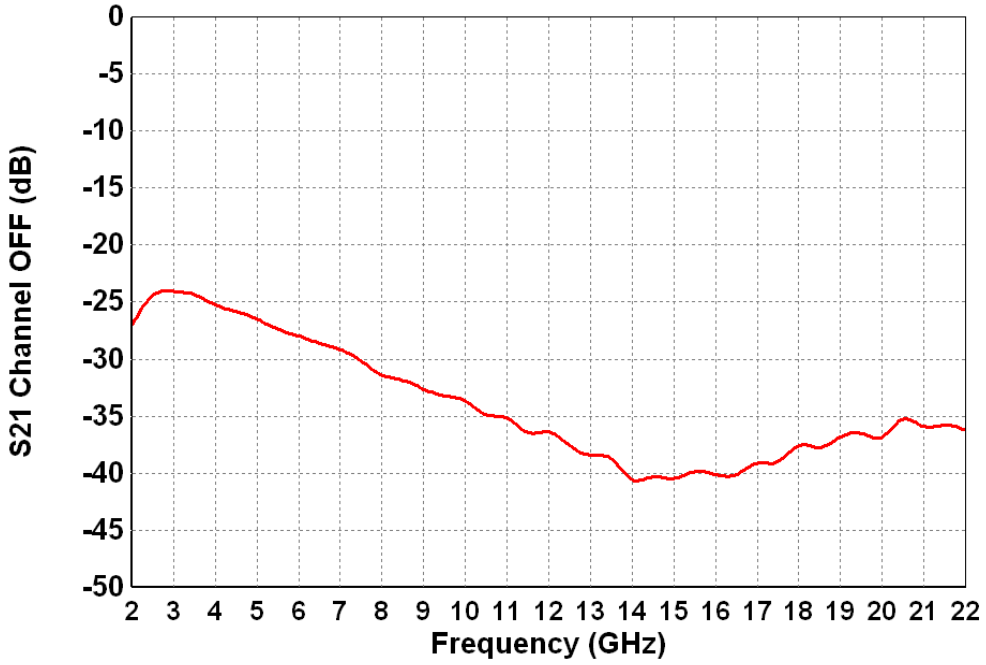
Typical Board Measurements

Tamb.= +25°C, VL = -25V, VH = 0V

ON state RFC-RF1 path : S21 versus Frequency (C1N/C1S = 0V, C2N/C2S = -25V)



OFF state RFC-RF1 path: S21 versus Frequency (C1N/C1S = -25V, C2N/C2S = 0V)



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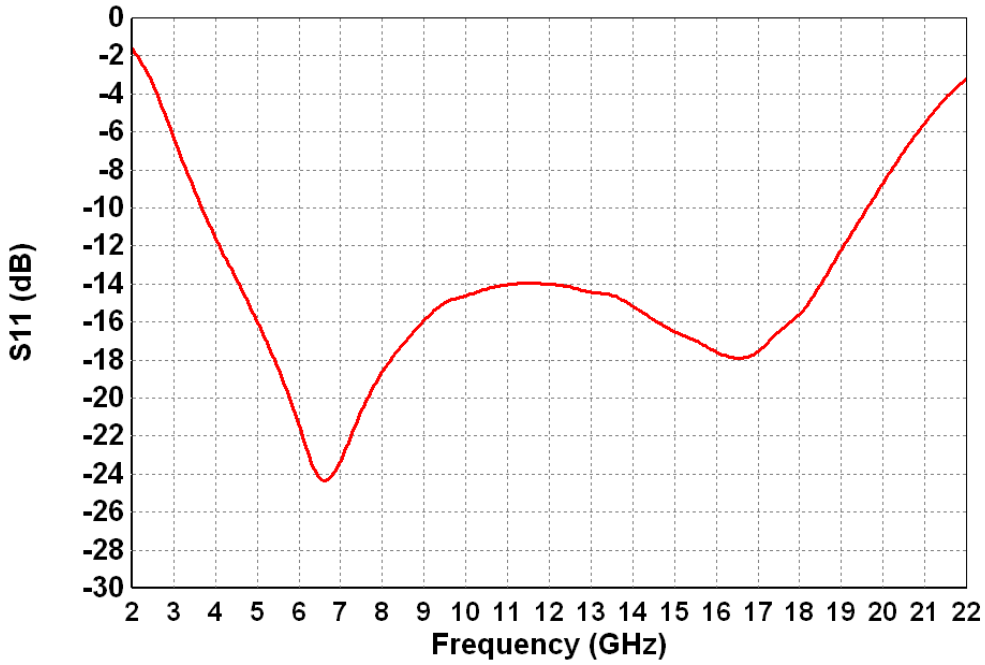
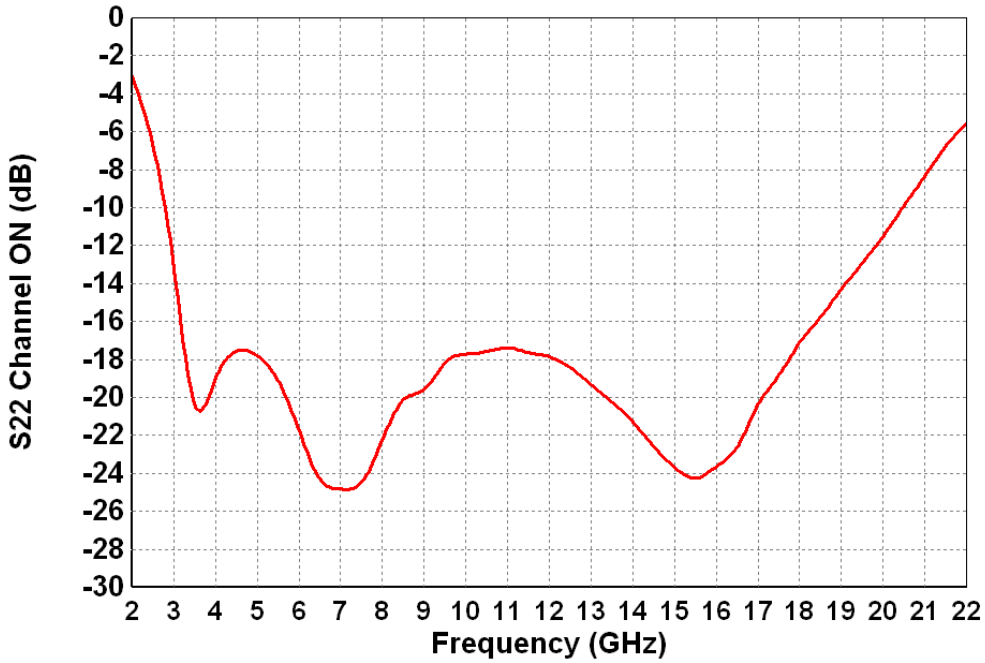
Typical Board Measurements

Tamb.= +25°C, VL = -25V, VH = 0V

ON state RFC-RF1 path: S11 versus Frequency (C1N/C1S = 0V, C2N/C2S = -25V)



ON state RFC-RF1 path: S22 versus Frequency (C1N/C1S = 0V, C2N/C2S = -25V)



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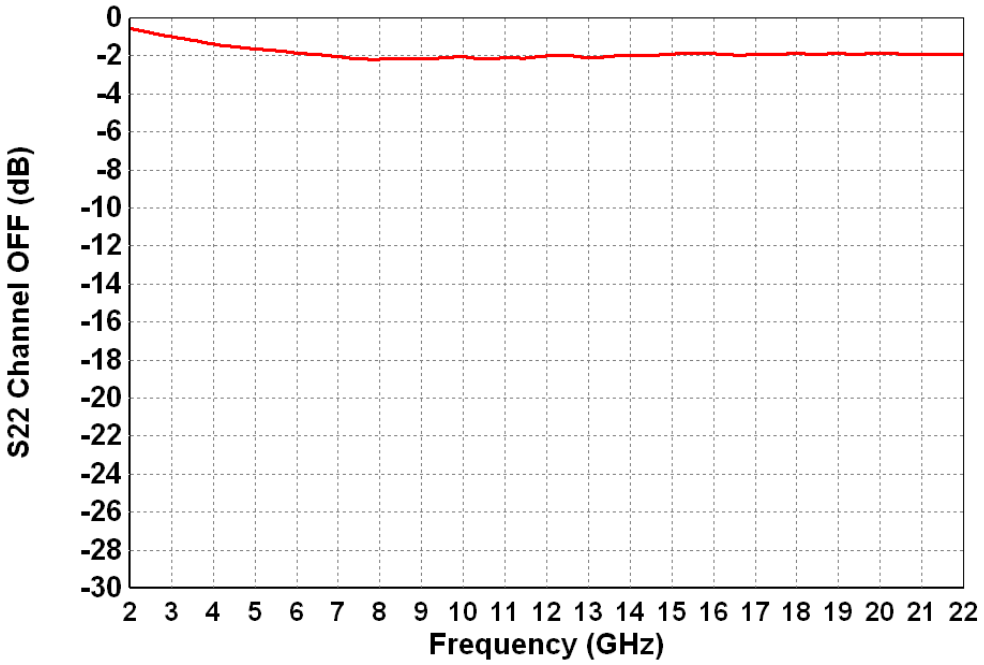
Typical Measurements In Test Fixture

Tamb.= +25°C, VL = -25V, VH = 0V

OFF state RFC-RF1 path: S22 versus Frequency (C1N/C1S = -25V, C2N/C2S = 0V)



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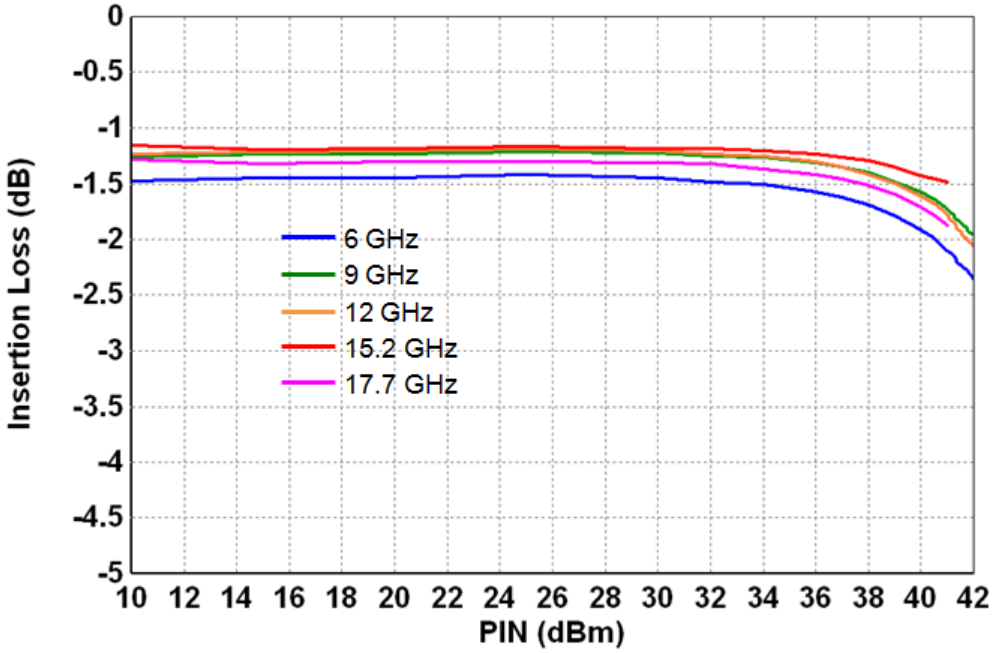
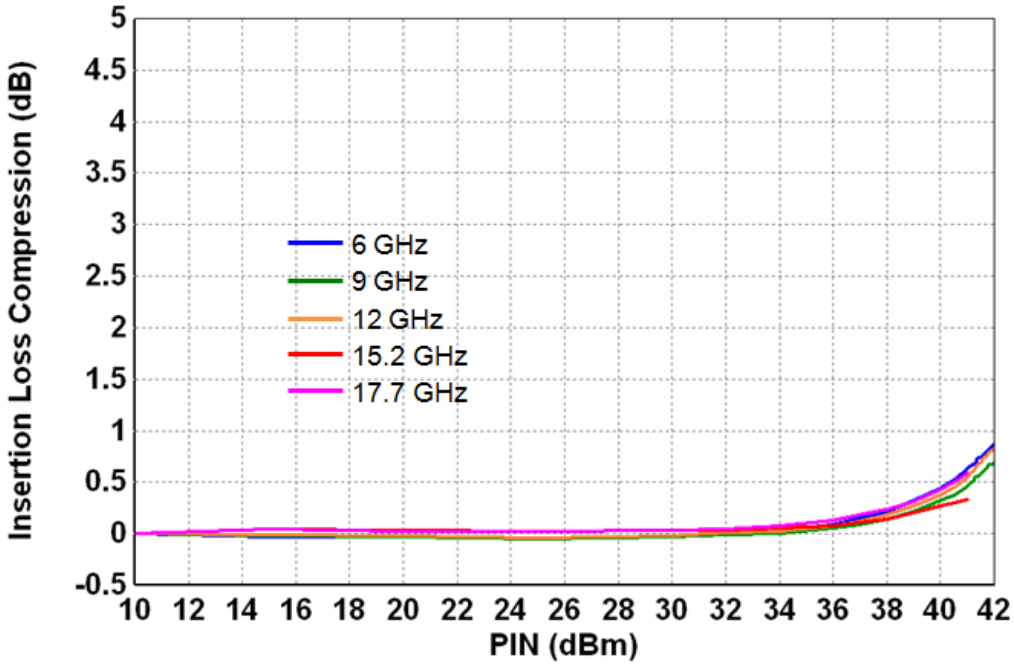
Typical Measurements In Test Fixture

Tamb.= +25°C, VL = -25V, VH = 0V

Insertion Loss RFC-RF1 path versus Input Power
(C1N/C1S = 0V, C2N/C2S = -25V)



Insertion Loss RFC-RF1 path Compression versus Input Power
(C1N/C1S = 0V, C2N/C2S = -25V)



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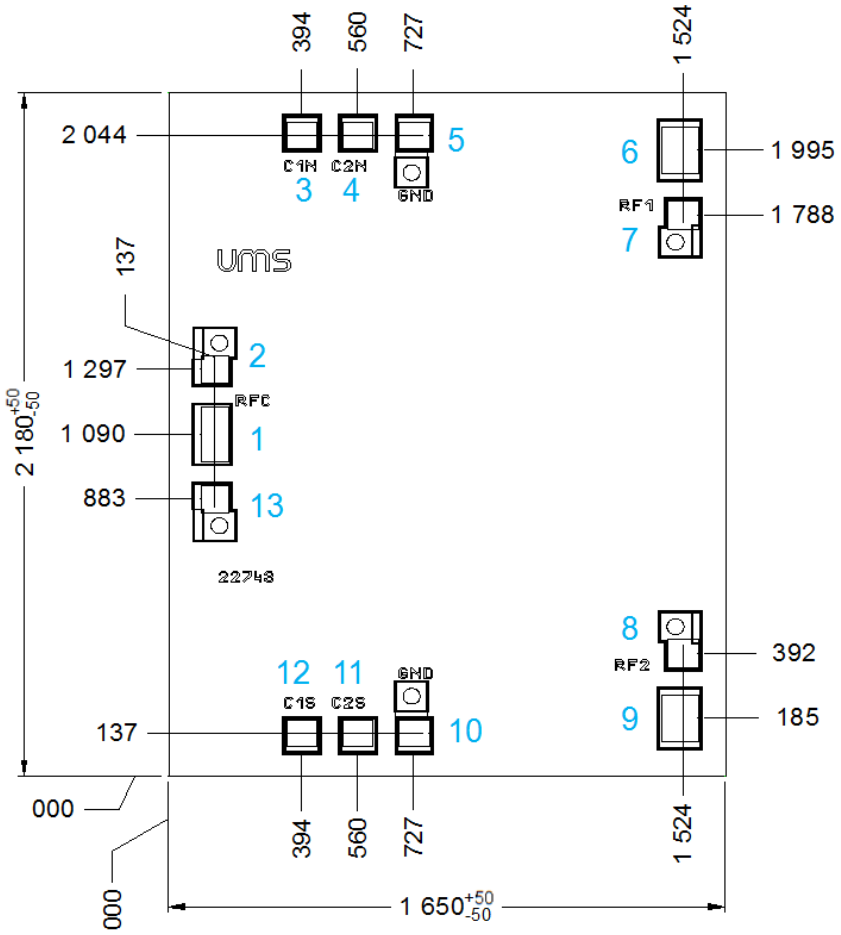
Mechanical data



All dimensions are in micrometers
Chip size = 1650µm x 2180µm (with dicing streets) ±50µm
Chip thickness = 100µm
RF pads (1) = 196 x 115µm²
RF pads (6,9) = 196 x 130µm²
DC pads (3,4,11,12) = 117 x 112µm²

PAD Number	Name	Description
1	RFC	Input RF port RFC
6	RF1	Output RF port 1
9	RF2	Output RF port 2)
3,12	C1N / C1S	Control voltage of path RFC-RF1
4,11	C2N / C2S	Control voltage of path RFC-RF2
2,5,7,8,10,13	GND	Ground (Not connected)

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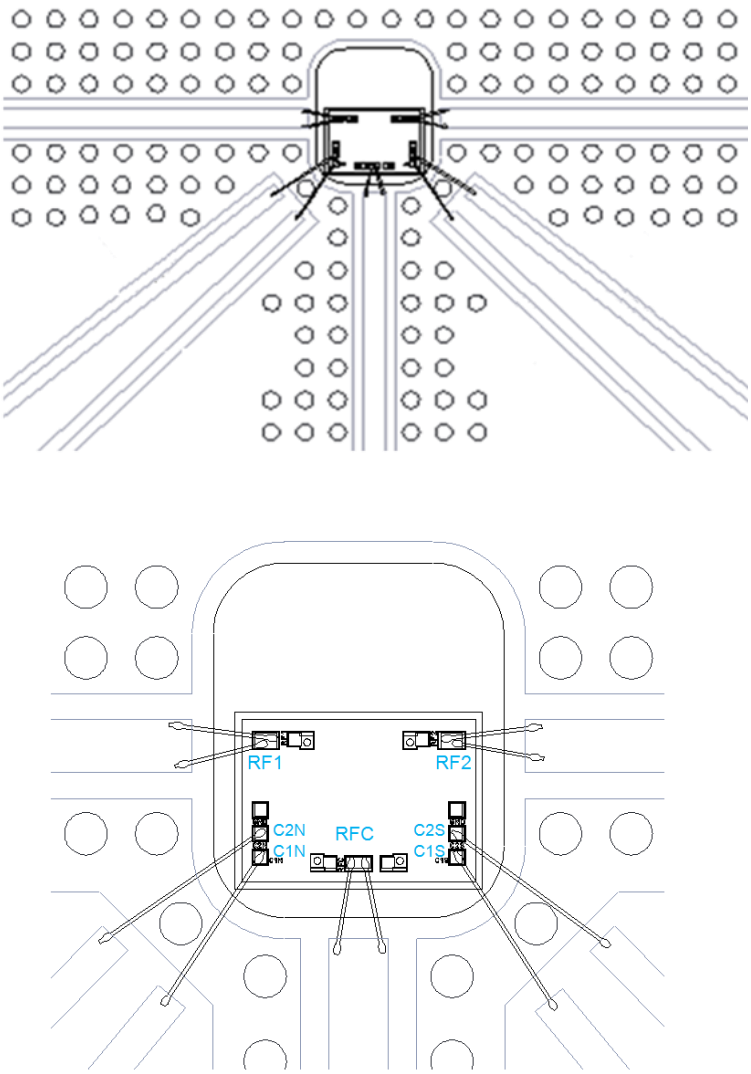
Recommended assembly plan



Recommended RF bonding wires: length<0.7mm / Ø25µm

Recommended circuit bonding table

Label	Type	Decoupling	Comment
C1N or C1S C2N or C2S	Control voltage	Not required	SPDT switch pad control
RFC, RF1, RF2	RF access	Not required	2 wires with a of diameter 25 µm length <700µm

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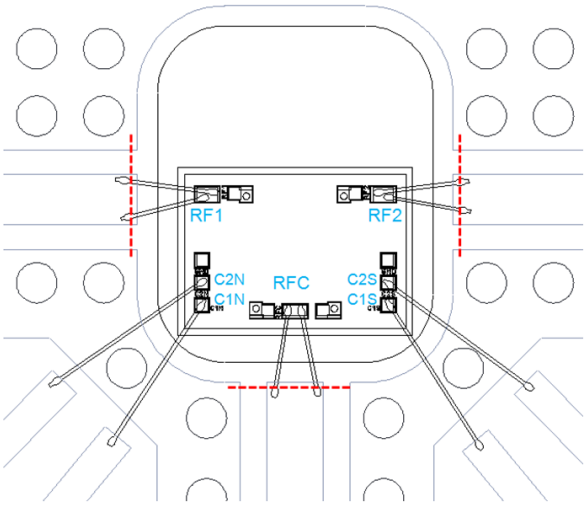
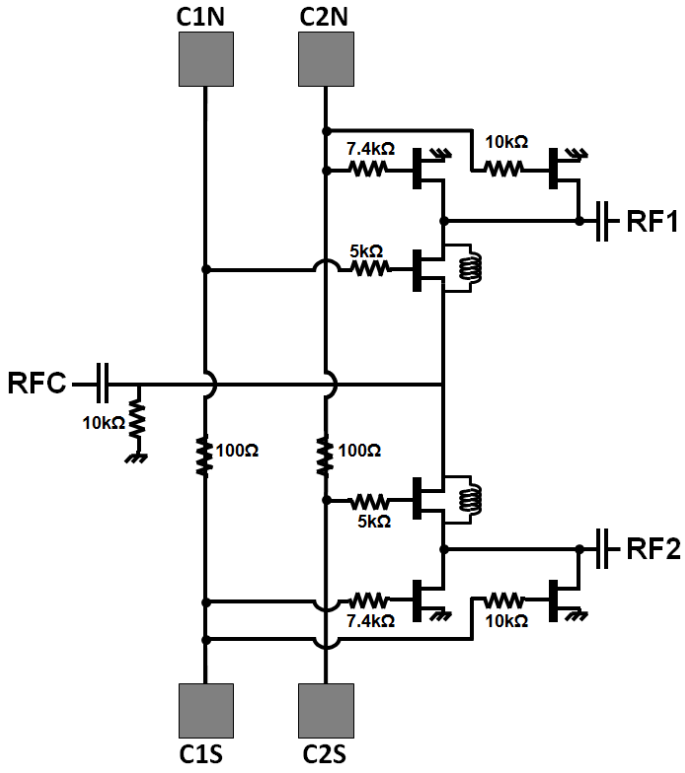
Definition of the Sij reference planes

The reference planes used for Sij and power measurements given above are shown in the figure opposite



DC Schematic



Use either PAD C1N or PAD C1S to control RFC-RF1 path.

Use either PAD C2N or PAD C2S to control RFC-RF2 path.

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Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS products.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended handling and assembly methodology

Refer to the application note AN0026 available at http://www.ums-gaas.com for assembly recommendations for the UMS products based on GaN on SiC technology.

Ordering Information

Chip form:	CHS8618-99F/00

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