QPA9426

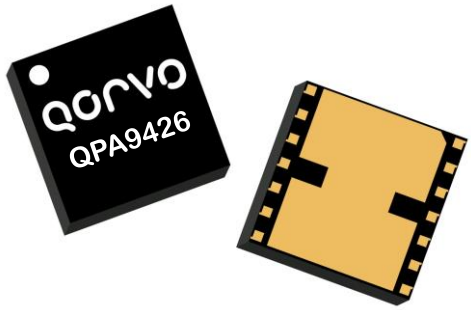
High Linearity ½ W Small Cell PA

General Description

The QPA9426 is a high-linearity two-stage power amplifier in a low-cost surface-mount package with on-chip bias control and temperature compensation circuits, suitable for small cell base station applications.

QPA9426 provides 34 dB gain and +27 dBm linear power over the 2.5 – 2.7 GHz frequency range which includes 3GPP bands 7, 38 & 41. The amplifier is able to achieve −47 dBc ACLR at +27 dBm output power using 20 MHz LTE signal.

The QPA9426 integrates two high performance amplifier stages onto a module to allow for a compact system design and requires very few external components for operation. The amplifier is bias adjustable allowing the amplifier's power consumption to be optimized. The QPA9426 is available in a lead-free/RoHS-compliant 7 x 7 mm surface mount package.

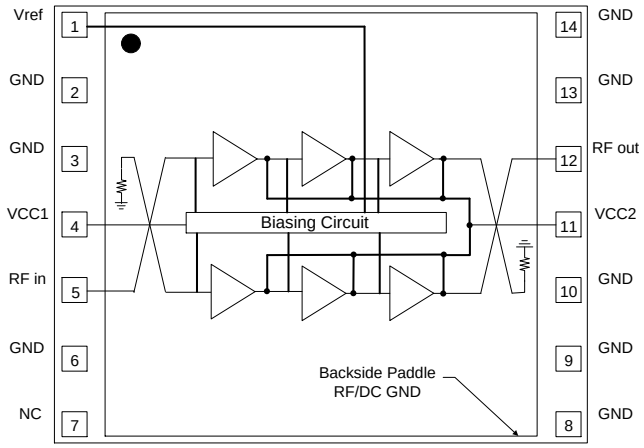


7 x 7 mm Leadless SMT Package

Product Features

- 2.5 – 2.7 GHz Frequency Range
- Fully Integrated, 2 Stage Power Amplifier
- Internally Matched 50 Ω Input/Output
- −47 dBc ACLR at Pavg = +27 dBm
- 34 dB Gain
- 14% PAE at +27 dBm
- 420 mA Quiescent Current
- On-chip Bias Control and Temp. Comp. Circuit

Functional Block Diagram



Top View

Applications

- Small Cell / Picocell
- Bands 7, 38, 41
- Enterprise Femtocell
- Customer Premises Equipment (CPE)
- Data Cards and Terminals
- Distributed Antenna Systems (DAS)
- Booster Amps, Repeaters

Ordering Information

Part No.	Description
QPA9426SR	100pcs on 7" reel
QPA9426TR13	2,500pcs on a 13" reel (standard)
QPA9426PCB401	2.5 – 2.7 GHz Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−55 to +150 °C
Supply Voltage (V_{CC})	+6 V
V_{ref}	+3.5 V
RF Input Power, CW, 50Ω, T=25°C	+10 dBm

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{CC1}, V_{cc2}	+3.6	+4.5	+5.25	V
V_{ref}	+2.75	+2.85	+2.95	V
T_{CASE}	−40		+85	°C
Tj at T_{CASE} max			+156	°C

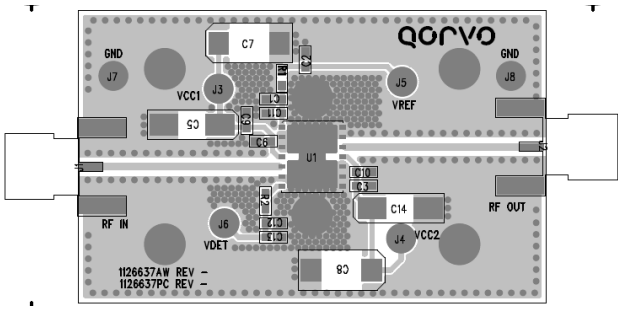
Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

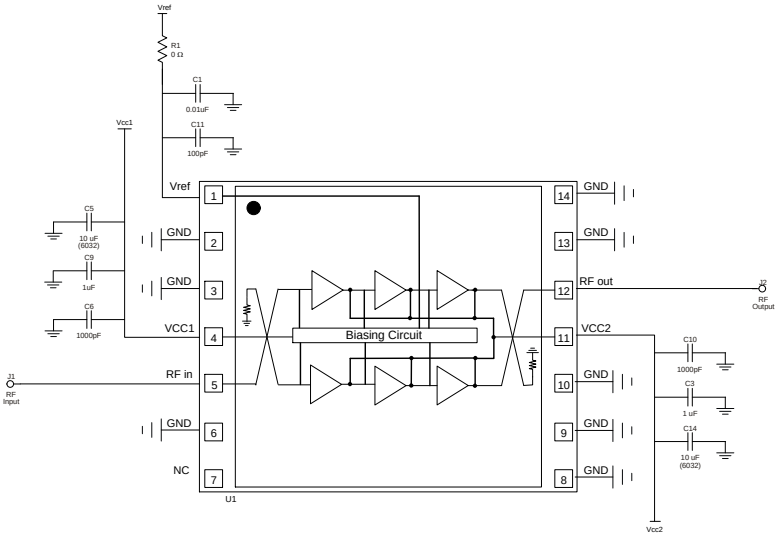
Electrical Specifications

Parameter	Conditions(1)	Min	Typ	Max	Units
Operational Frequency Range		2.5		2.7	GHz
Test Frequency			2.6		GHz
Gain		30.5	33	35	dB
Input Return Loss			20		dB
Output Return Loss			20		dB
P1dB			35.5		dBm
ACLR	P_{OUT} = +27dBm, 20 MHz LTE E-TM1.1, 9.5dB PAR	-45	−47		dBc
Power Added Efficiency	P_{OUT} = +27dBm, 20 MHz LTE E-TM1.1, 9.5dB PAR	12	14		%
Quiescent Current, I_{CQ}[2]	V_{CC1} + V_{CC2}	330	420	500	mA
Leakage Current	V_{CC} = +4.5 V, V_{ref} = 0 V		3	10	µA
Reference Current , I_{ref}	V_{ref} = +2.85V		15	19	mA
Operational Current, I_{CC}	Pout = +27 dBm		805	900	mA
Switching Speed	Rise time (10%-90%)		650		ns
	Fall time (90%-10%)		500		ns
Spurious Output Level	Pout ≤ +27dBm, In & Out of band load VSWR ≤ 10:1		-60		dBc
VSWR survivability	No permanent degradation or failure	10:1			-
Harmonics	$2F_0$ (Pout = 27 dBm)		-32	-28	dBc
	$3F_0$ (Pout = 27 dBm)		-34	-30	dBc
	$4F_0$ (Pout = 27 dBm)		-64	-60	dBc
Thermal Resistance, θ_{jc}	Module (junction to case)			17.4	°C/W

Notes:
1. Test conditions unless otherwise noted: V_{CC1} = V_{cc2} = +4.5 V, V_{ref} = +2.85V, Temp = +25 °C, 50 Ω system.
2. Current through Vcc1 does not vary with power. Vcc1 provides the bias voltage to the current mirror circuit along with Vref to set the bias point for the whole amplifier.

Evaluation Board Layout and Schematic





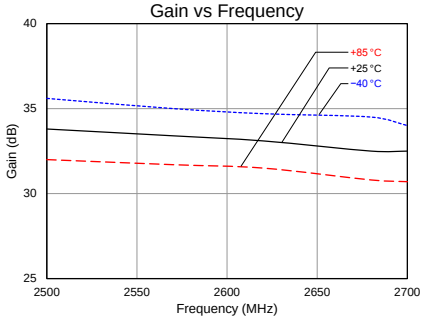
Bill of Material – Evaluation Board

Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board		
U1	n/a	High Linearity 0.5 W Power Amplifier	Qorvo	QPA9426
R1	0 Ω	Resistor, Chip, 0603, 5%	various	
C1	0.01 uF	Capacitor, Chip, 0603, 5%	various	
C11	100 pF	Capacitor, Chip, 0603, 5%	various	
C3, C9	0.1 uF	Capacitor, Chip, 0603, 5%	various	
C5, C14	10 uF	Capacitor , Chip, 6032, 10%, Tantalum	various	
C6, C10	1000 pF	Capacitor , Chip, 0603, NPO/COG, 5%	various	

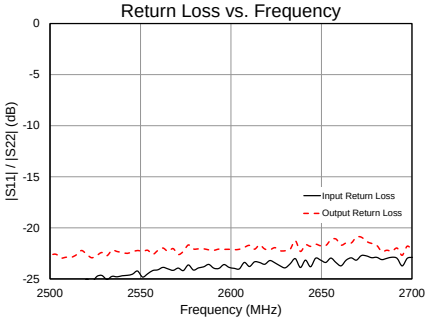
Performance Plots

Test conditions unless otherwise noted: V_{CC1} = V_{CC2} = +4.5V, Vref = +2.85 V, Temp.= +25 °C

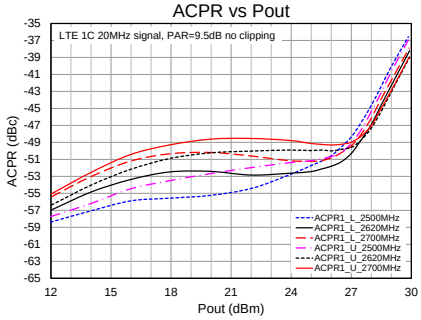
Gain vs Frequency



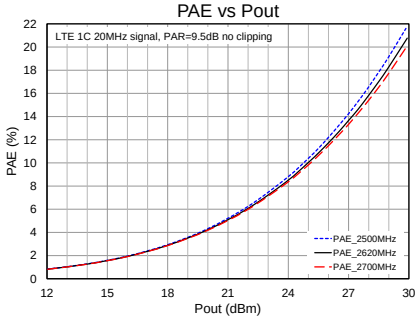
Return Loss vs. Frequency



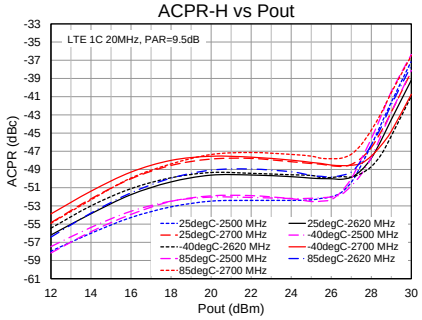
ACPR vs Pout



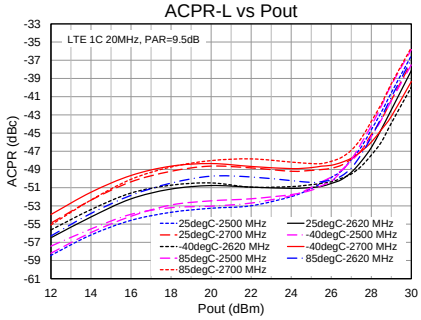
PAE vs Pout



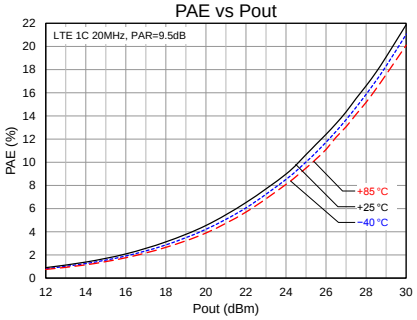
ACPR-H vs Pout



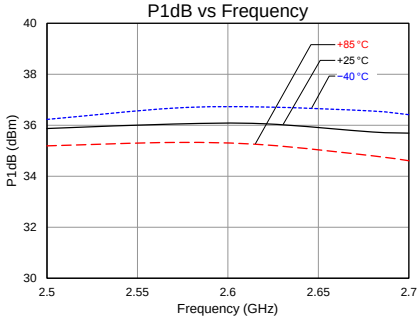
ACPR-L vs Pout



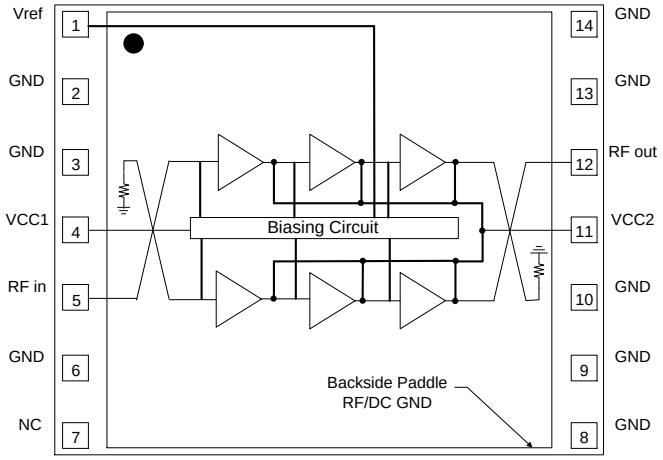
PAE vs Pout



P1dB vs Frequency



Pin Configuration and Description

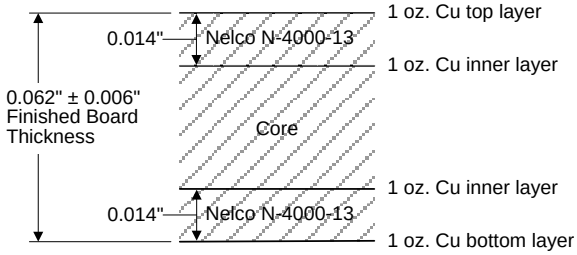


Top View

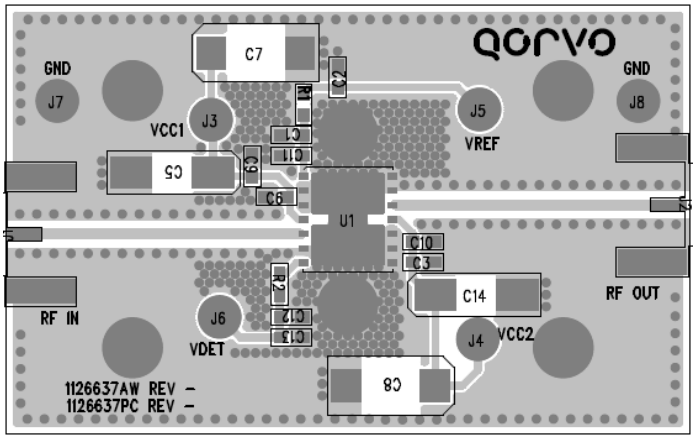
Pad No.	Label	Description
1	Vref	Provides reference voltage for internal active biasing circuit
2, 3, 6, 8, 9, 10, 13, 14	GND	RF and DC ground.
4	VCC1	Bias voltage for current mirror in combination with Vref to set the bias point.
5	RFin	RF input pin. The DC is internally blocked at this pin.
7	NC	No internal connection. Can be left open or grounded for mounting integrity.
11	VCC2	Supply to all stages.
12	RFout	RF output pin. The DC is internally blocked at this pin.
Backside Paddle	RF/DC GND	RF/DC ground. See PCB Mounting Pattern for suggested footprint.

Evaluation Board PCB Information

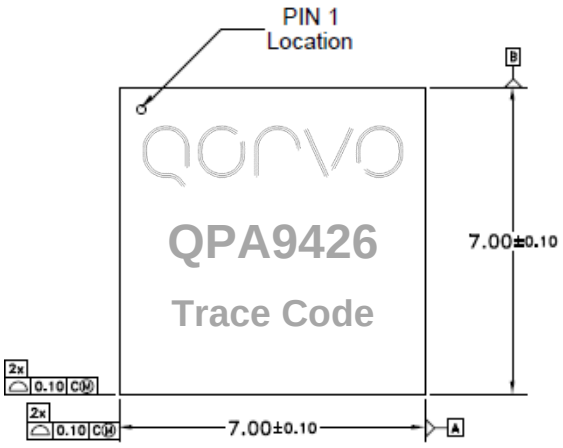
Qorvo PCB 1126637 Material and Stack-up

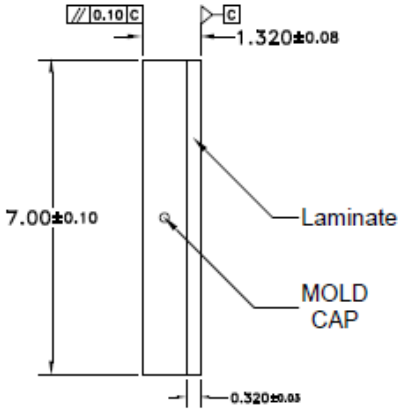


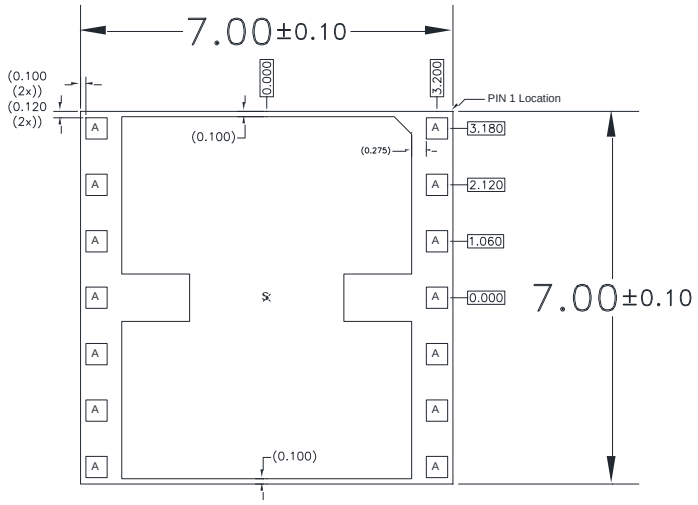
50 ohm line dimensions: width = .028”
spacing = .028”.

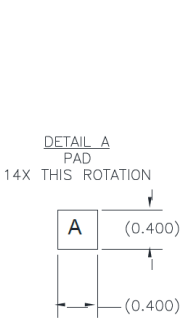


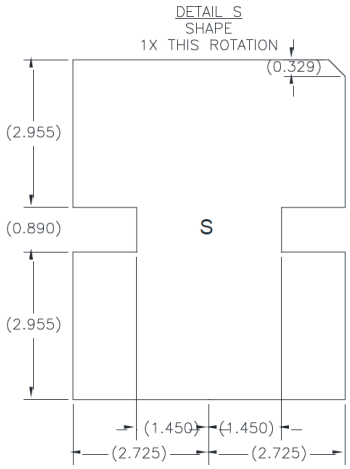
Package Marking and Dimensions





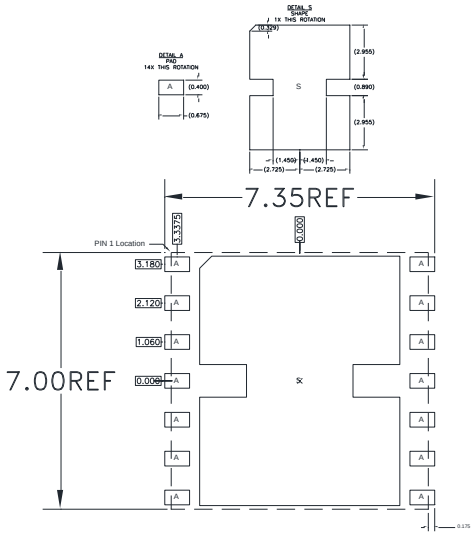




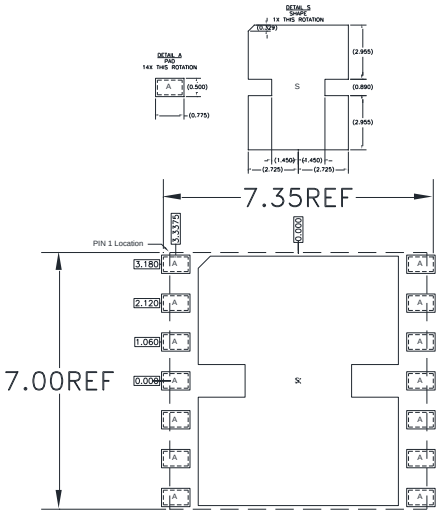


Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



RECOMMENDED
LAND PATTERN



RECOMMENDED
LAND PATTERN MASK

Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 2	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: Electrolytic plated Au over Ni

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU. This product also has the following attributes:

- Product uses RoHS Exemption 7c-I to meet RoHS Compliance requirements.
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Tel: **1-844-890-8163**

Web: **www.qorvo.com**

Email: **customer.support@qorvo.com**

For technical questions and application information: **Email:** **sjcapplications.engineering@qorvo.com**

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