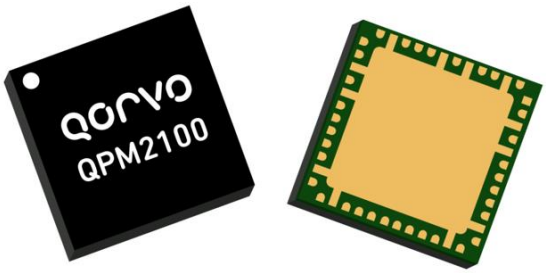
QPM2100

2.5 – 4.0 GHz Multi-Chip T/R Module

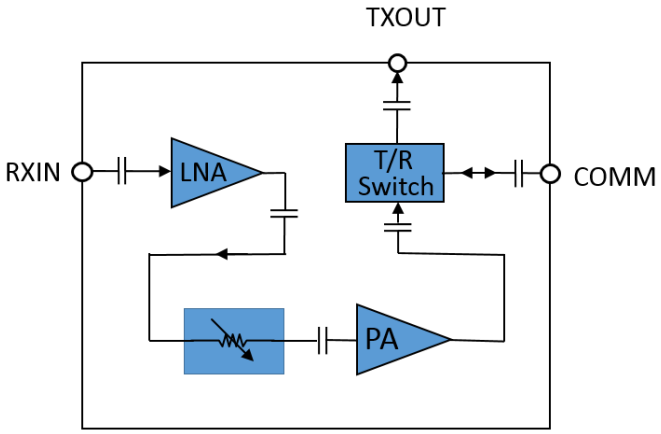
Product Description

The QPM2100 is a GaAs multi chip module (MCM) designed for S-Band radar applications within the 2.5-4.0 GHz range. The device consists of a T/R switch, a transmit path which is a low loss pass through, and a receive path consisting of a low-noise amplifier, a digital attenuator and a driver amplifier. The receive path offers 30 dB of small signal gain and 1.2 dB noise figure. It includes a 6 bit digital step attenuator (DSA) with 31.5 dB gain control range. It can deliver 14.5 dBm of power at P1dB with 34 dBm of output TOI. All functional MMIC blocks can be enabled or DC powered off with internal control circuitry. All control signals use CMOS compatible logic. The response time of signal control is less than 15 nS.

The QPM2100 chips are fabricated on Qorvo's GaAs 0.25um process. The 7 x 7 OVM QFN surface mount package, coupled with a proprietary die-attach process, allows the QPM2100 to perform well at extreme temperature ambient. Its compact size supports tight lattice spacing requirements needed for S - Band phased array radar applications.



Functional Block Diagram



Product Features

- Frequency Range: 2.5 – 4.0 GHz
- RX Noise Figure: 1.2 dB
- RX Small Signal Gain: 30 dB
- RX Power at 1dB compression: 14.5 dBm
- RX OTOI : 34 dBm
- 6 Bit DSA Attenuation Range: 31.5 dB
- TX insertion loss: 1.2 dB
- Fast switching time: < 15 nS
- No need of negative bias
- Package Dimensions: OVM 7 x 7 x 0.8 mm

Performance is typical at room temperature.
Please reference electrical specification table and data plots for more details.

Applications

- Commercial and Military Radar
- Electronics Warfare (EW)
- Communications

Ordering Information

Part No.	Description
QPM2100SR	Tape and Reel, Qty 100
QPM2100EVB02	QPM2100 Evaluation Board

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Normal Operating Conditions

Parameter [1]	Min	Typ	Max	Units
RX Drain Voltage (VD1, VD3)	3.0	3.3	3.6	V
RX LNA Quiescent Current (ID1) [2]	125	140	160	mA
RX Buffer Amplifier Drain Quiescent Current (ID3) [2]	35	40	50	mA
Device Enabling Control Current		4		mA
DSA Logic Control Power Supply (VDSA) [4]	2.5	3.3	5	V
DSA Logic Control Power Supply Current		6		mA
Logic Control Voltage High (VH)	2.5	3.3	5	V
Logic Control Voltage Low (VL)	0	0	0.4	V
DSA Logic Control Bit Current (total)			1.0	mA
Switch Control Voltage (TRSW, Switched to RX) [3]		VL		V
Switch Control Voltage (TRSW, Switched to TX) [3]		VH		V
Device Enable Control (STBY, LNA and PA ON) [3]		VL		V
Device Enable Control (STBY, LNA and PA OFF) [3]		VH		V
Switch Control Current		2		mA
Operating Temperature Range	−55	25	95	°C

1 *Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.*
2. *LNA and buffer amp (PA) are self-biased, current shown are typical.*
3. *TRSW, STBY can use CMOS logic levels, "0" = "VL", "1" = "VH".*
4. *VDSA will draw current, it can use separate power supply or the same supply as VD1 and VD3 if used the same voltage as VH. It needs to be on for switch and DSA controls.*

Attenuation States Control Bits Truth Table

Logic "0" = VL, Logic "1" = VH

States	VDSA	B6	B5	B4	B3	B2	B1
0 dB (Reference)	1	1	1	1	1	1	1
0.5 dB	1	1	1	1	1	1	0
1 dB	1	1	1	1	1	0	1
2 dB	1	1	1	1	0	1	1
4 dB	1	1	1	0	1	1	1
8 dB	1	1	0	1	1	1	1
16 dB	1	0	1	1	1	1	1
31.5 dB	1	0	0	0	0	0	0

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Electrical Specifications

Test conditions unless otherwise noted: VD = 3.3 V, ID1 = 140 mA, ID3 = 40 mA, VH= 3.3 V, VL = 0 V, VDSA = 3.3 V, 25 °C
Data de-embedded to device reference plane

Parameter	Min	Typical	Max	Units
Frequency	2.5		4.0	GHz
RX Small Signal Gain [1]		30		dB
RX Noise Figure		1.2		dB
RX Output Power		14.5		dBm
RX Input Return Loss		10		dB
RX Output Return Loss		13		dB
RX Output TOI [2]		34		dBm
RX Attenuation Step (6 Bit)		0.5		dB
RX Attenuation Range		31.5		dB
RX Gain Temperature Coefficient		−0.016		dB/°C
TX Insertion Loss		1.2		dB
TX Input Return Loss		17		dB
TX Output Return Loss		16		dB
Switching Speed between RX and TX using TRSW [3]		10	15	nS
Response time with STBY control [3]		10	15	nS
Channel Isolation (Receive On, TX Off) [4]		35		dBc
Power Handling (RX Mode, LNA input port) [5]			-15	dBm
Power Handling (TX Mode, COMM port) [5]			20	dBm

1. *Reference state (no attenuation).*
2. *At -29dBm Pin, 10 MHz tone spacing, reference states.*
3. *From 50% trig signal to 10% RF rising response or 90% RF falling response.*
4. *Leakage of switch when channel is off.*
5. *Linear operating power level.*

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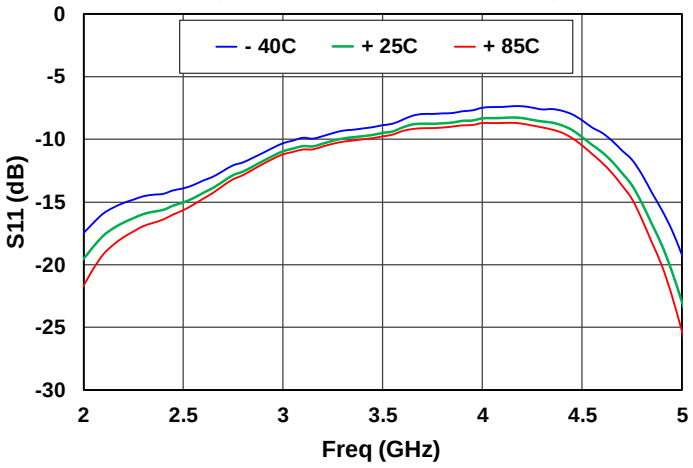
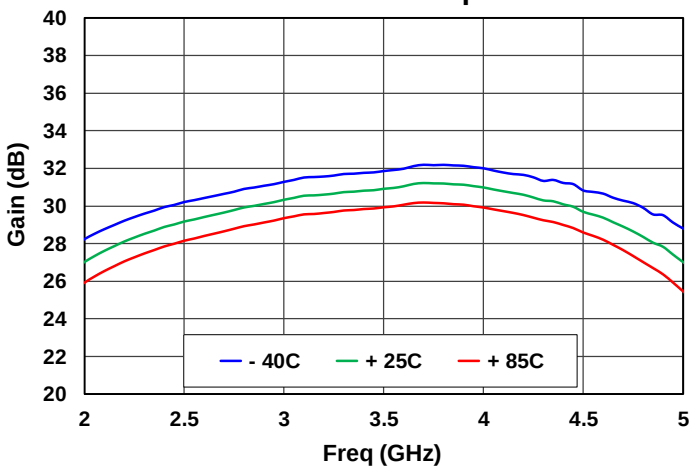
Small Signal, Receive Channel

Test Conditions unless otherwise stated:
VD1 = VD3 = 3.3 V, ID1 = 140 mA, ID3 = 40 mA, VH= 3.3 V, VL = 0 V, VDSA = 3.3 V, Reference State, 25 °C

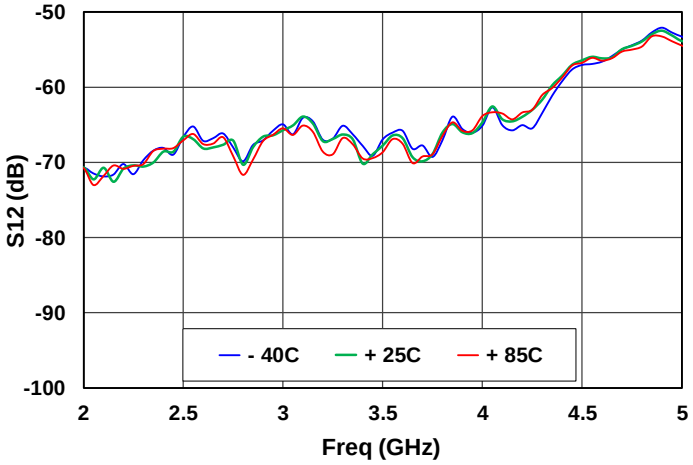
Input Return Loss vs Temp



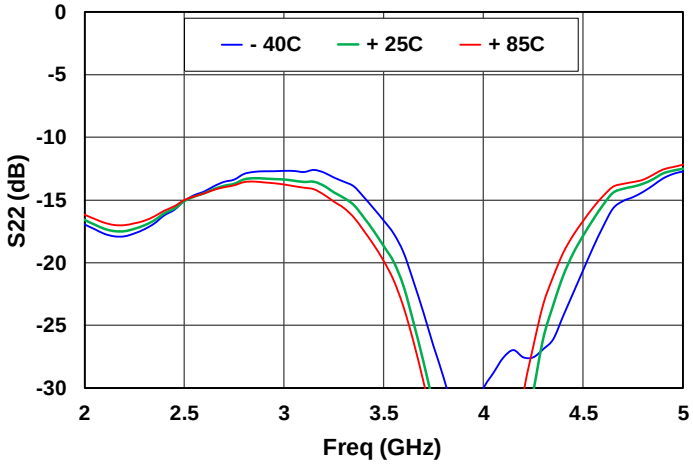
Gain vs Temp



Reverse Isolation vs Temp



Output Return Loss vs Temp



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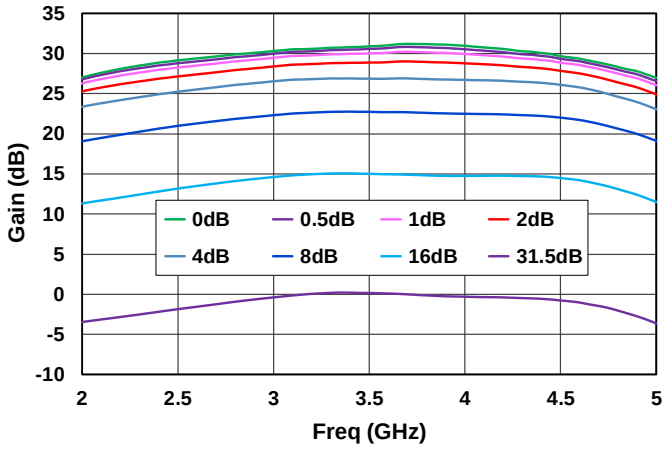
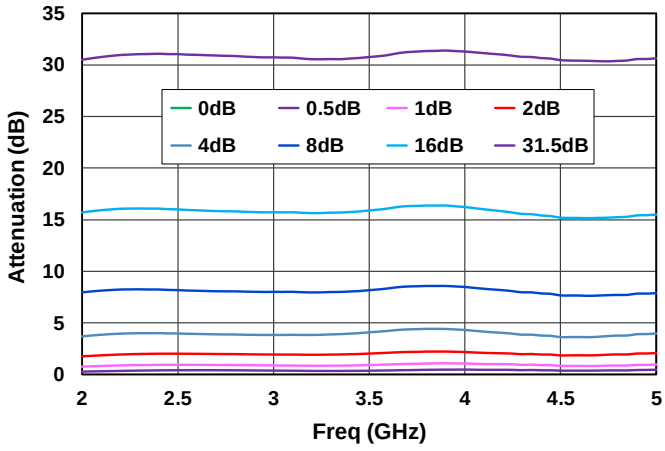
Small Signal, Receive Channel

Test Conditions unless otherwise stated:
VD1= VD3 = 3.3 V, ID1 = 140 mA, ID3 = 40 mA, VH= 3.3 V, VL = 0 V, VDSA = 3.3 V, 25 °C

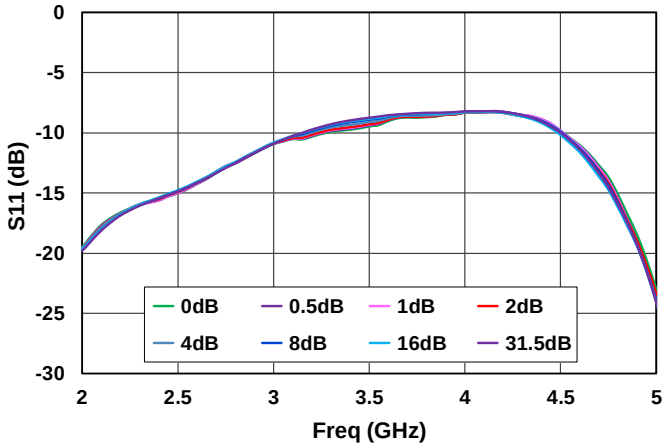
Gain vs Attenuation States



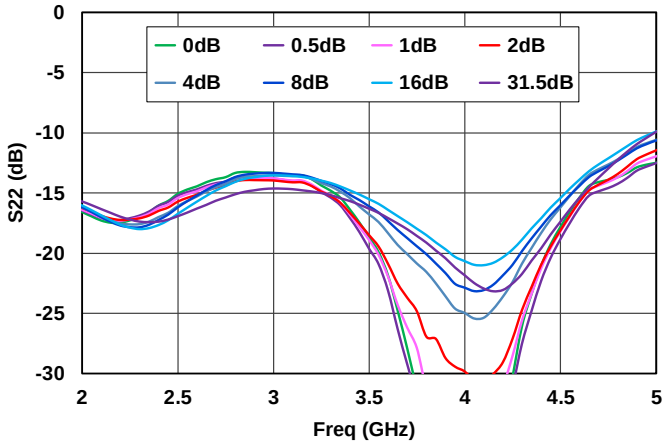
Attenuation vs States



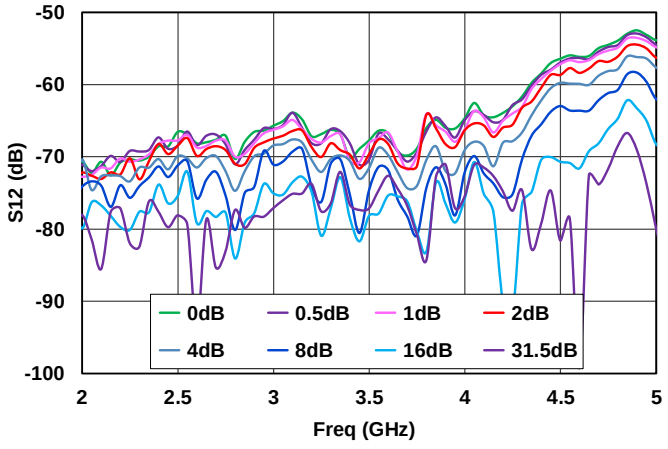
Input Return Loss vs Attenuation States



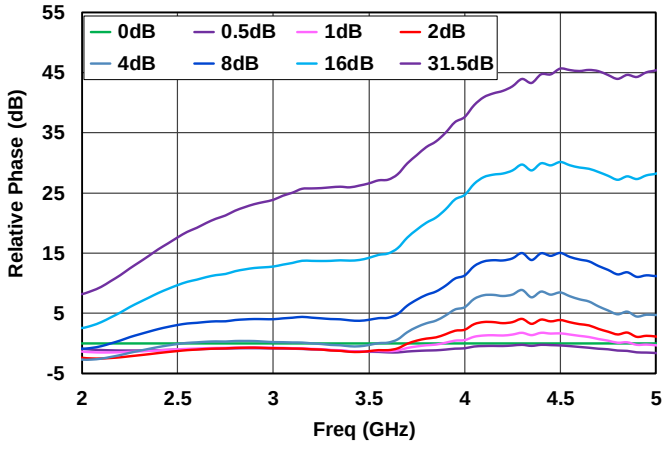
Output Return Loss vs Attenuation States



Isolation vs Attenuation States



Relative Phase vs Attenuation States



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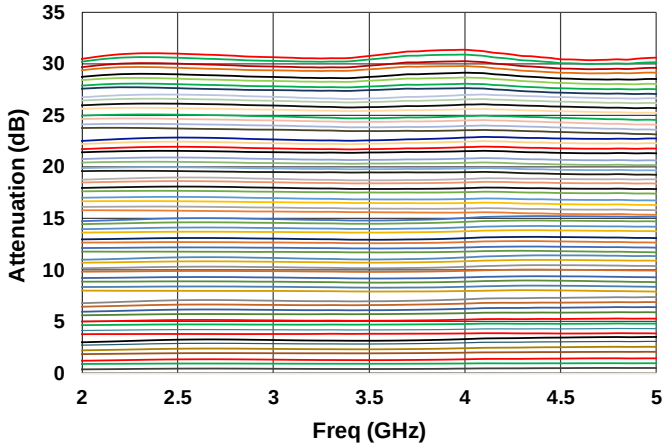
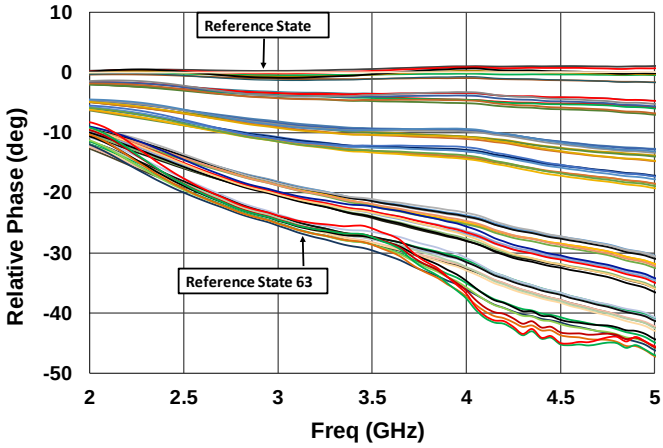
Performance Plots, Receive Channel

Test Conditions unless otherwise stated:
VD1 = VD3 = 3.3 V, ID1 = 140 mA, ID3 = 40 mA, VH= 3.3 V, VL = 0 V, VDSA = 3.3 V, 25 °C

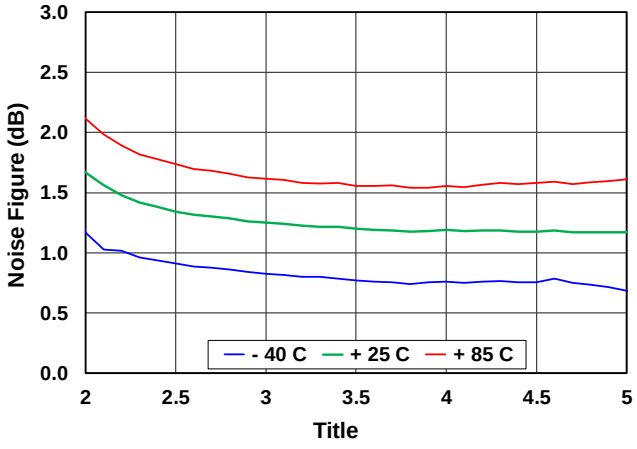
Attenuation vs All States



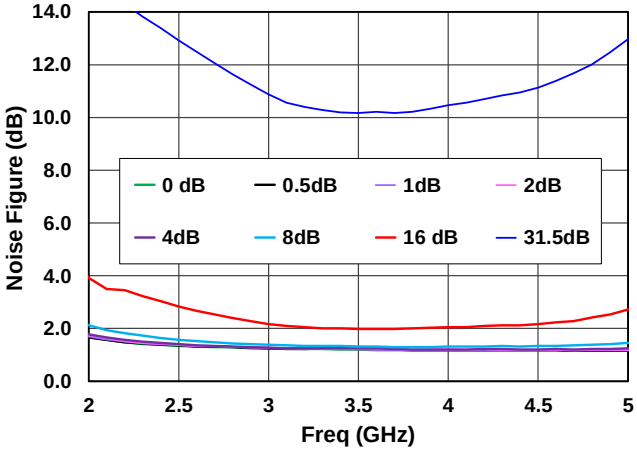
Relative Phase vs All States



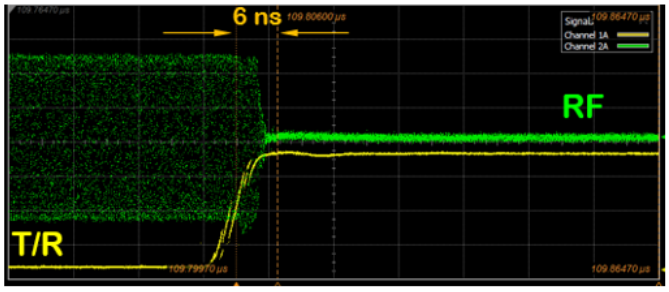
NF vs Temperature



NF vs Attenuation States

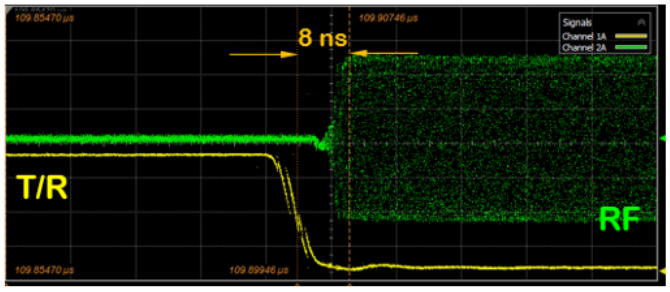


Response Time



Receive Path Falling Edge
Time base = 10 nS/div, RF power: -30 dBm, 3GHz

Response Time



Receive Path Rising Edge
Time base = 10 nS/div, RF power: -30 dBm, 3 GHz

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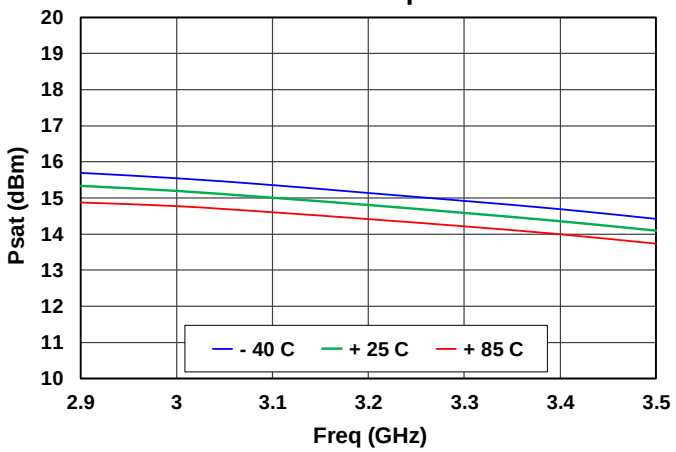
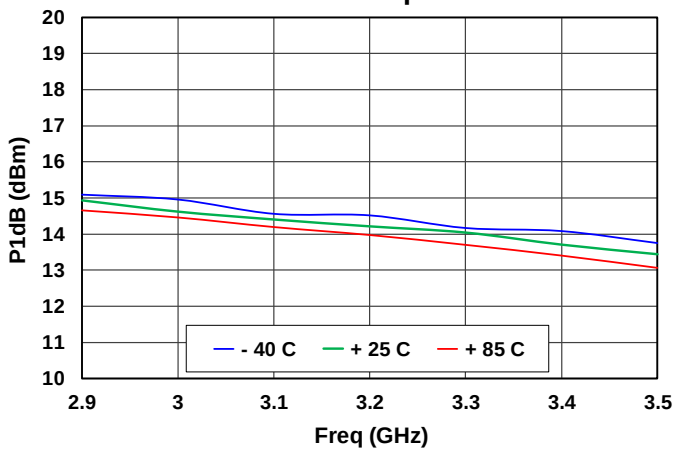
Large Signal, Receive Channel

Test Conditions unless otherwise stated:
VD1 = VD3 = 3.3 V, ID1 = 140 mA, ID3 = 40 mA, VH= 3.3 V, VL = 0 V, VDSA = 3.3 V, Reference State, 25 °C

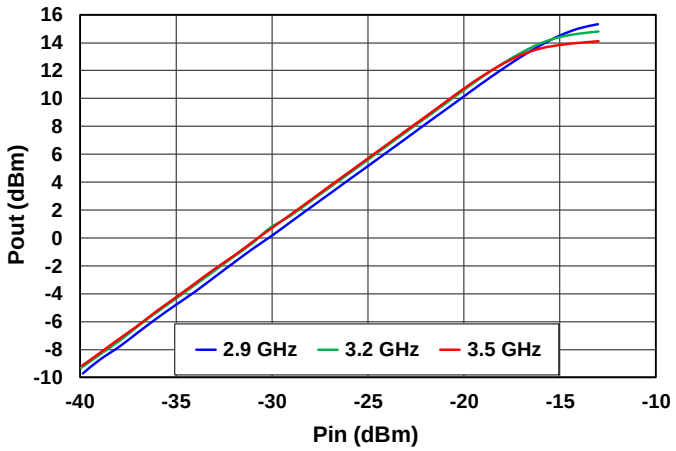
Psat vs Temperature



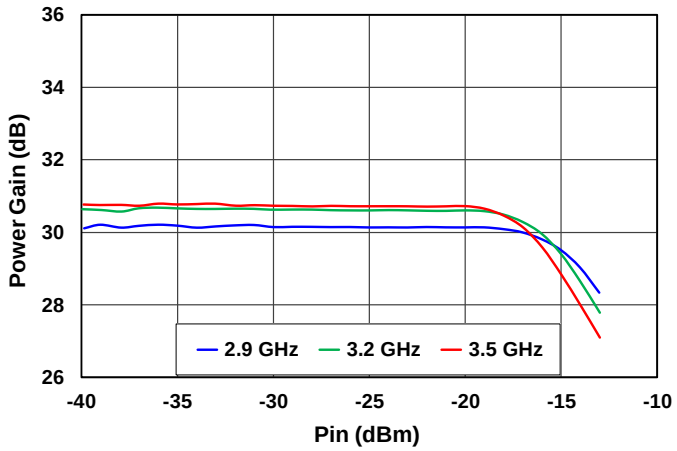
P1dB vs Temperature



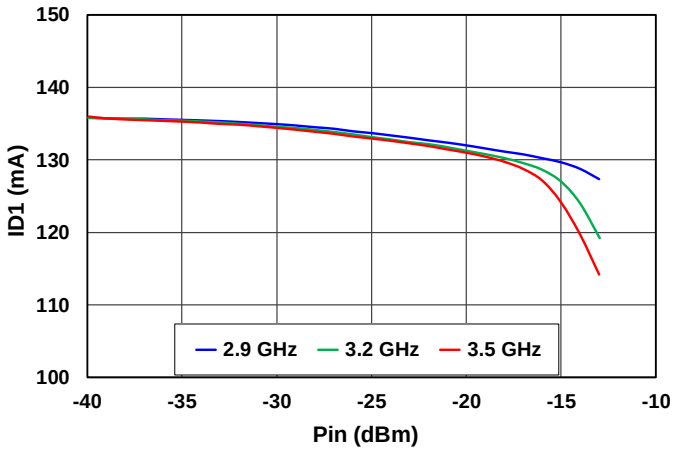
Pout vs Pin



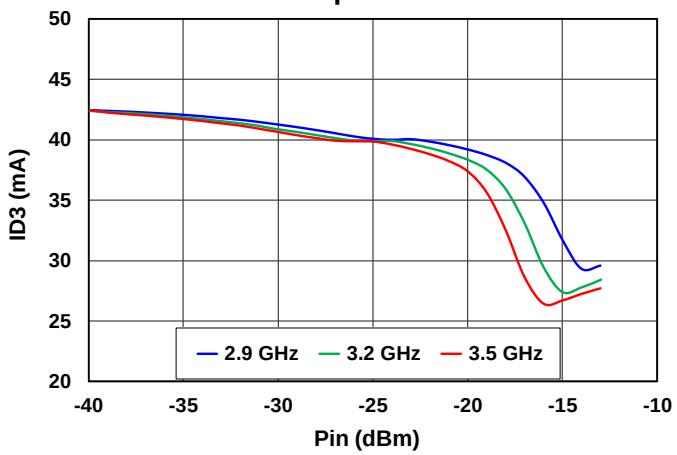
Power Gain vs Pin



LNA Current vs Pin



Buffer Amp Current vs Pin



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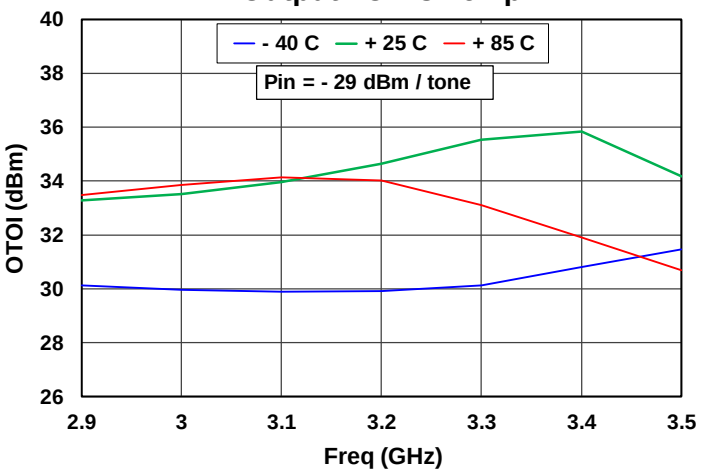
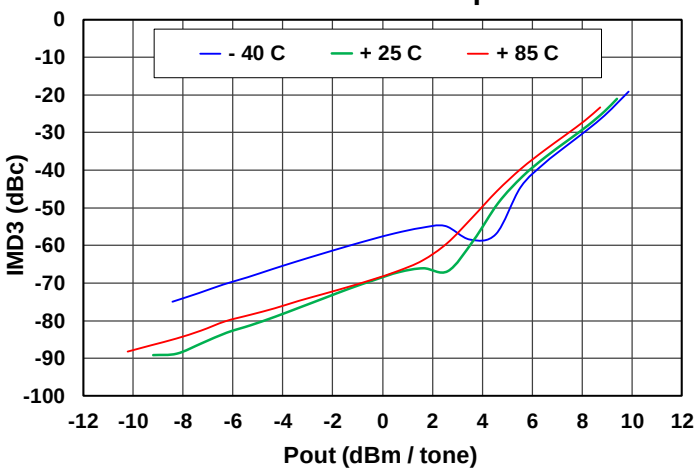
Linearity, Receive Channel

Test Conditions unless otherwise stated: Reference State, 25 °C
VD1 = VD3 = 3.3 V, ID1 = 140 mA, ID3 = 40 mA, VH= 3.3 V, VL = 0 V, VDSA = 3.3 V, Tone spacing: 10 MHz

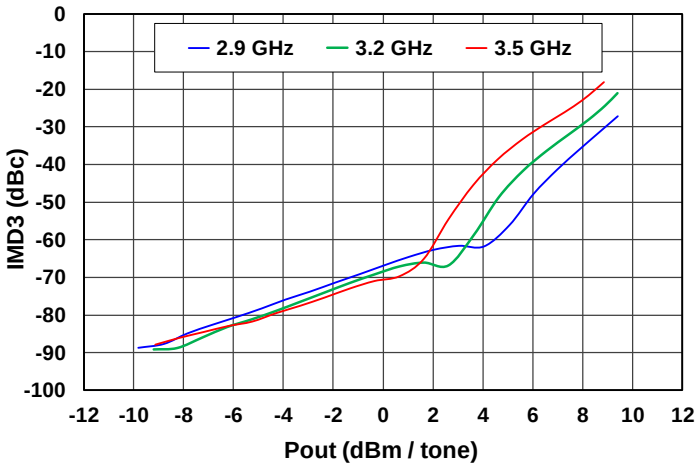
Output TOI vs Temp



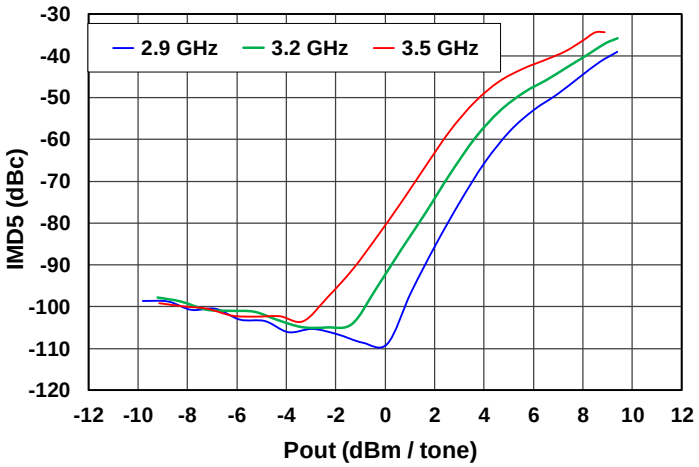
IMD3 vs Temp



IMD3 vs Pout



IMD5 vs Pout



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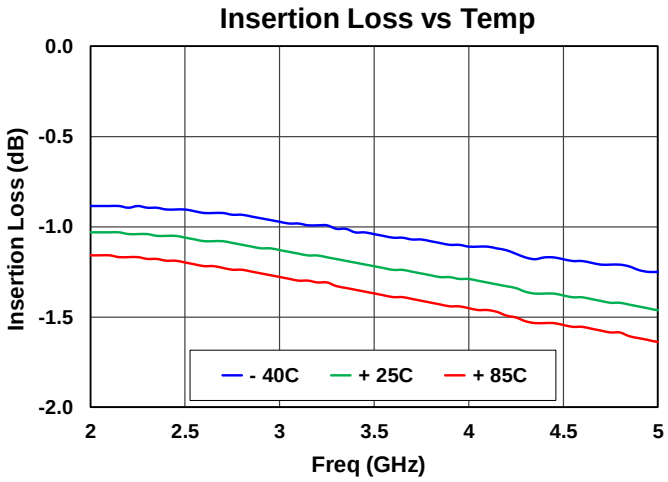
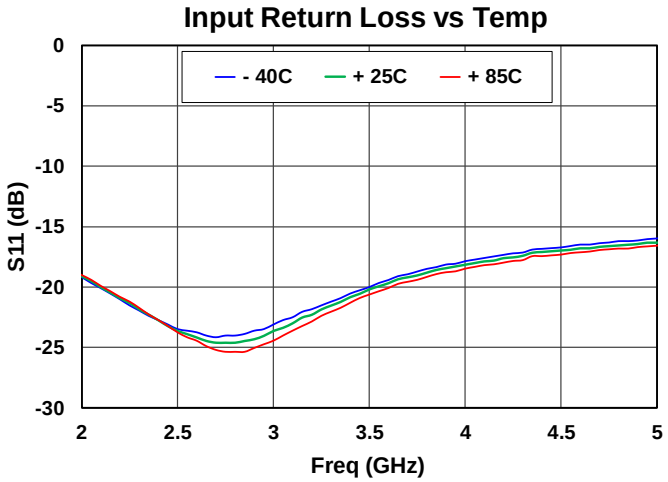
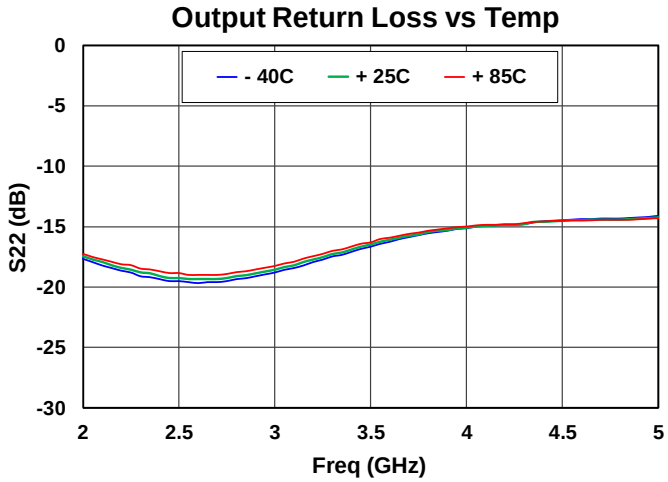
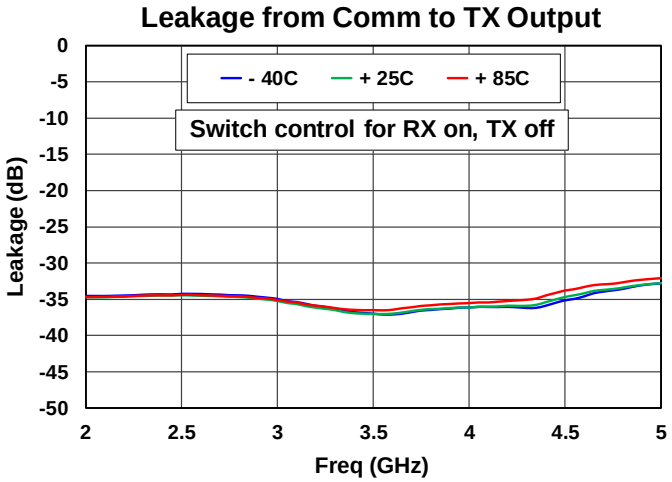
Small Signal, Transmit Channel

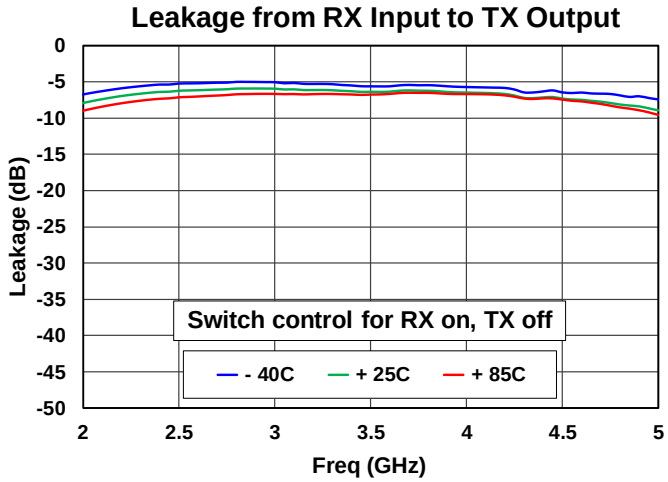
Test Conditions unless otherwise stated: STBY = “1”, TRSW = “1”, 25 °C.











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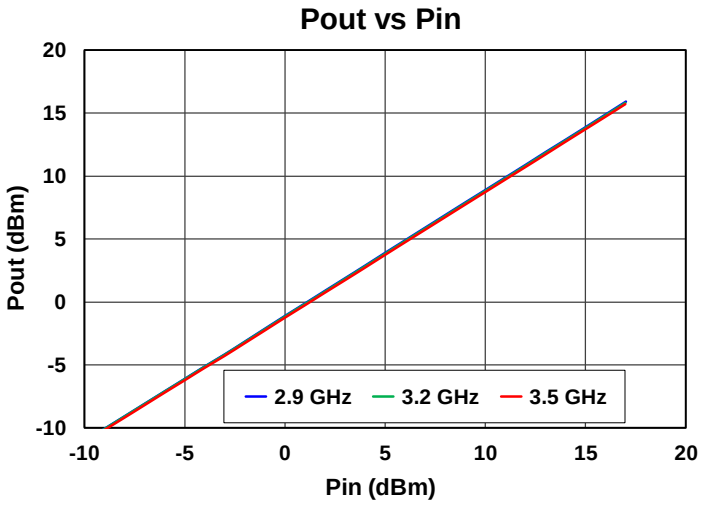
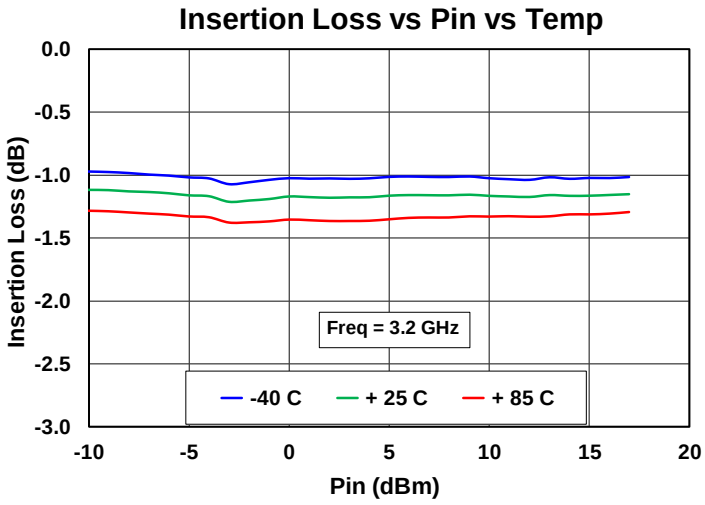
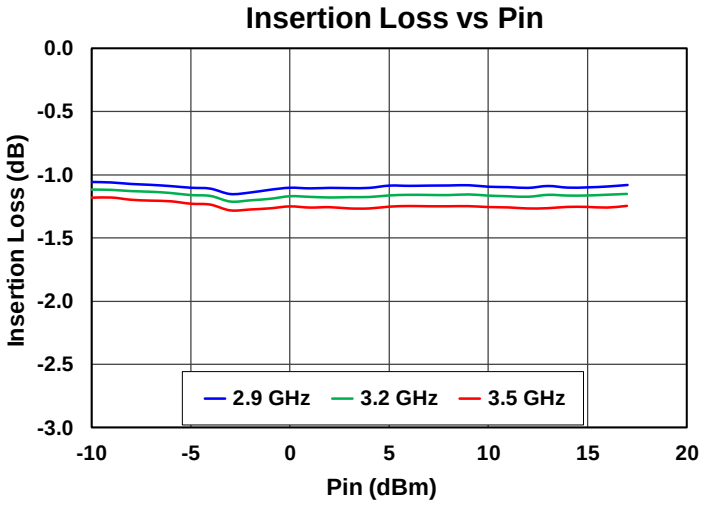
Large Signal, Transmit Channel

Test Conditions unless otherwise stated: STBY = “1”, TRSW = “1”, 25 °C







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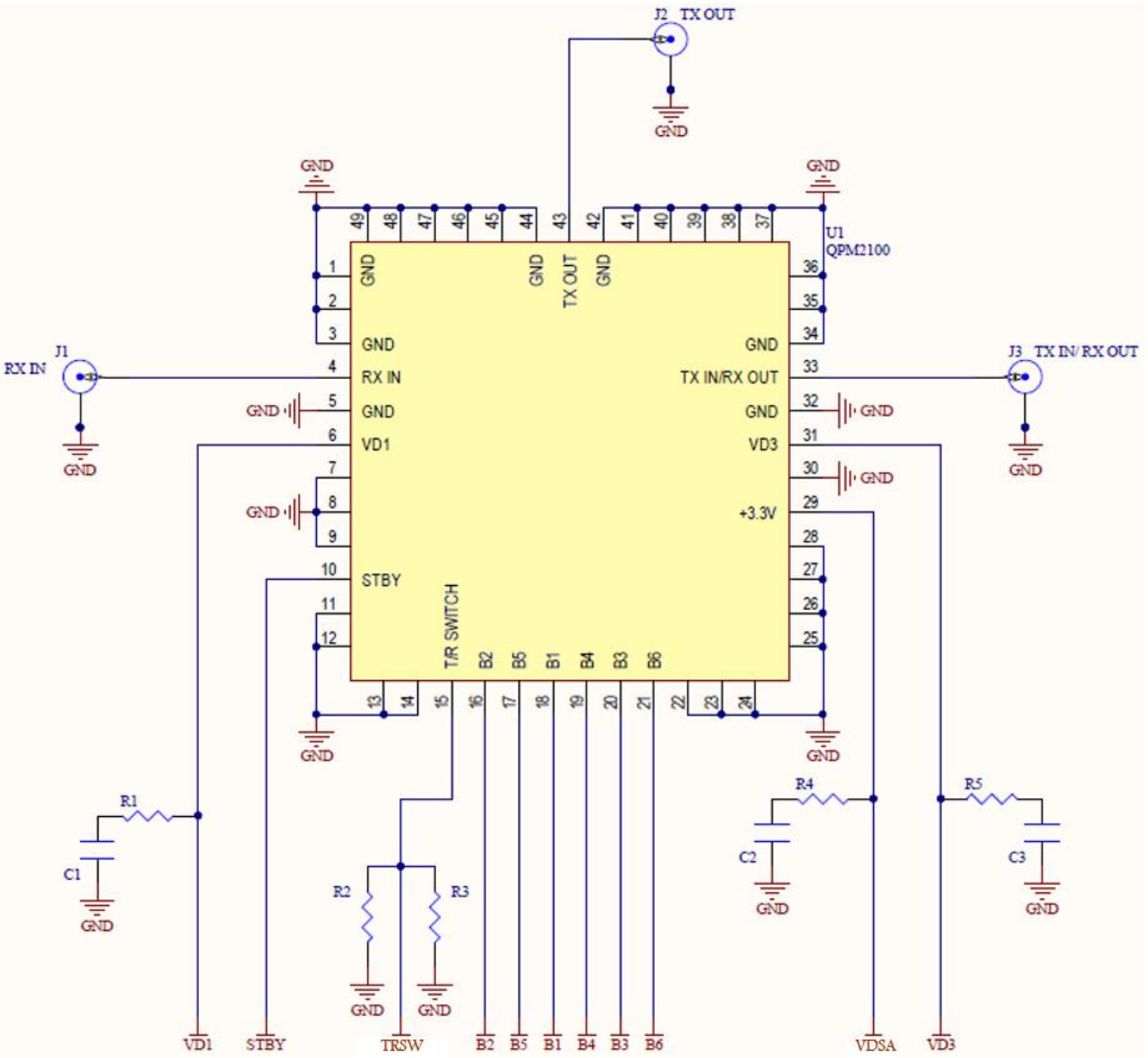
Application Circuit



Bias-up Procedure

1. Set VD1 current limit to 200 mA, VD3 current limit to 100 mA. STBY current limit to 10 mA, DSA control bits limit to 10 mA total, switch control current limit to 10 mA, VDSA limit to 20mA.
2. Set VD1 and VD3 to 3.3 V, VDSA to 3.3V
3. Set TRSW = 0 V for RX mode (or 3.3 V for TX mode)
4. Set DSA bit control to required values
5. Set STBY to 0 V to enable device (if RX mode)
6. Apply RF signal

Bias-down Procedure

1. Turn off RF signal
2. Set STBY = 3.3 V
3. Set VD1 = 0 V, VD3 = 0 V, VDSA = 0 V
4. Turn off drain supply
5. Turn off TRSW and STBY
6. Turn off VDSA Bias

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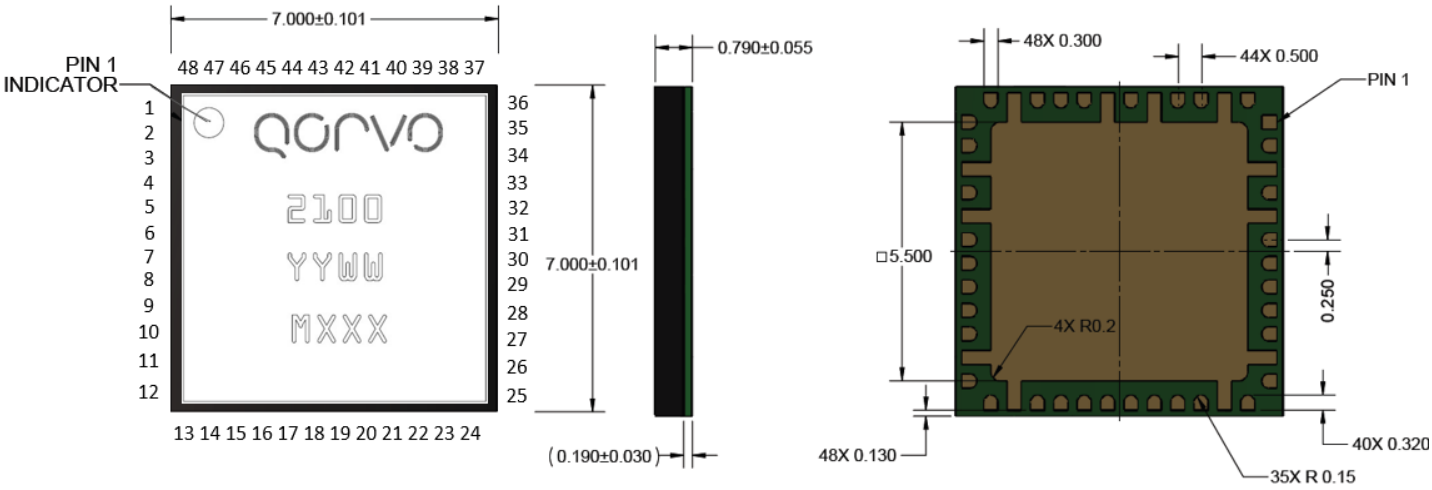
Mechanical Drawing & Pad Description



Dimensions in mm.
Part is mold encapsulated, package leads are gold plated with typical gold finish thickness of 0.1um.
Part Marking: QPM2100 = Part Number; YY = Part Assembly Year.
WW = Part Assembly Week; MXXX = Batch ID

Pin Number	Label	Description
3, 5, 11, 14, 23, 26, 32, 34, 38, 42, 44, 47 49 (package base ground)	GND	GROUND
4	RXIN	Receive Input, DC Blocked
6	VD1	Drain Supply
10	STBY	Standby Mode Switch
15	TRSW	T/R Switch Control
16, 17, 18	B2, B5, B1	DSA Digital Bit Control
19, 20, 21	B4, B3, B6	DSA Digital Bit Control
29	VDSA	DSA Signal Control Bias
31	VD3	Drain Supply
33	COMM, RXOUT / TXIN	Common Port, DC Blocked
43	TXOUT	Transmit Output, DC Blocked
1, 2, 7 - 9, 12, 13, 22, 24, 25, 27, 28, 30, 35 - 37 39 - 41, 45, 46, 48	N/C	No Internal Connections

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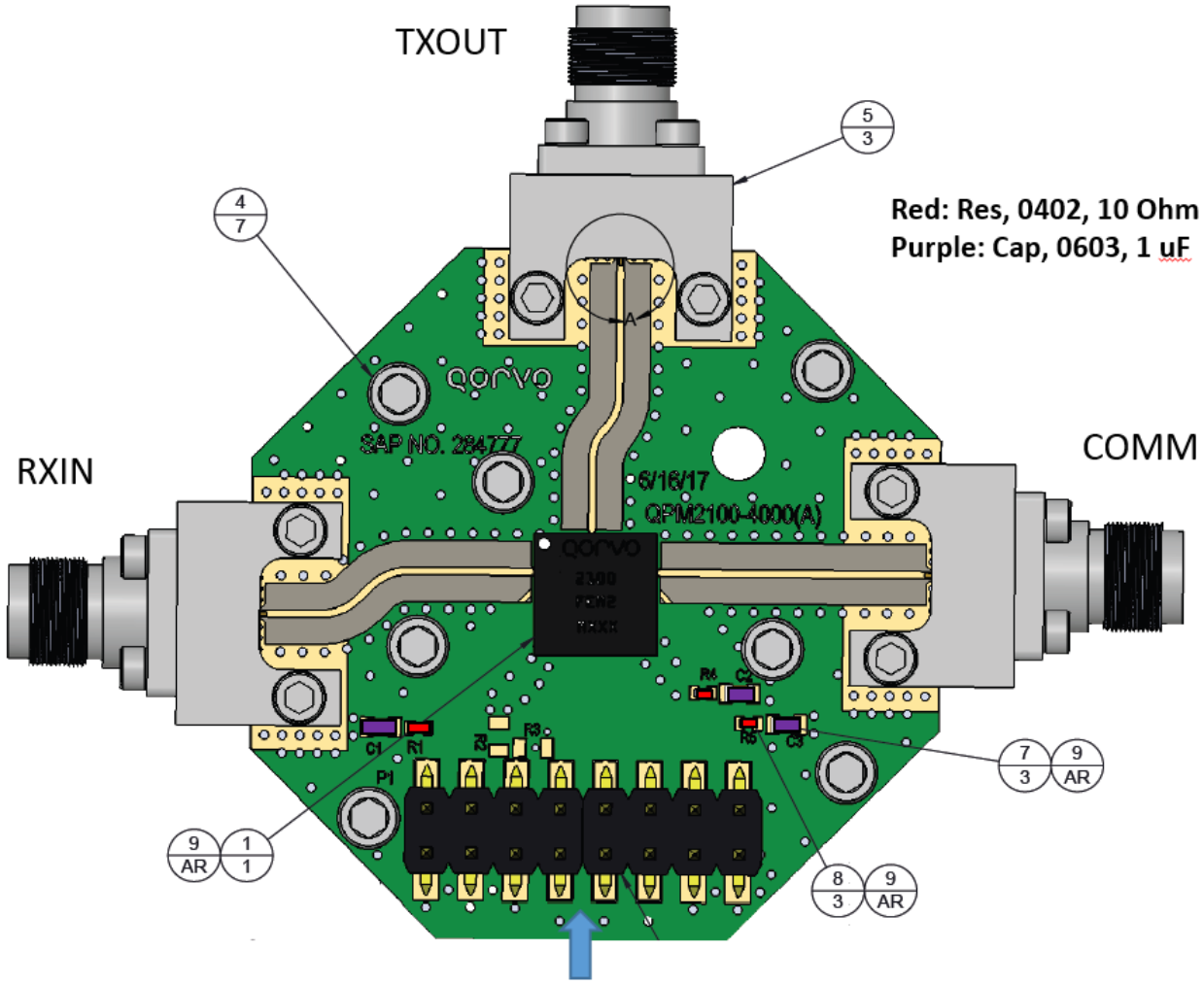
Evaluation Board and Assembly



Connector Pin Assignment

VD1	STBY	TRSW	B2	B1	B3	VDSA	VD3
GND	GND	GND	B5	B4	B6	GND	GND

RF Layer is 0.008” thick Rogers Corp. RO4003C (ε_r = 3.35). Metal layers are 0.5 oz. copper. The microstrip line at the connector interface is optimized for the Southwest Microwave end launch connector (1092-01A-12).

Bill of Materials

Ref. Des.	Component	Value	Manuf.	Part Number
C1, C2, C3	SMT Cap.	CAP, 0603 1.0uF +/-10% 50V X7R ROHS	Various	
R1, R4, R5	SMT Res.	RES, 0402 0 OHM, 5%, ROHS	Various	

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Absolute Maximum Ratings

Parameter	Min Value	Max Value	Units
Drain Voltage (VD1 and VD3)		5	V
Drain Current (ID1+ ID3)		250	mA
Enabling Control Voltage (STBY)	0	5	V
Enabling Control Current		5	mA
DSA Bias (VDSA)		5	V
DSA Bias Current		12	mA
Bit Control Voltage (B1 to B6)	0	5	V
Bit Control Current (total)		2	mA
Switch Control Voltage (TRSW)	0	5	V
Switch Control Current		5	mA
RF Input Power (Receive Mode)		18	dBm
RF Input Power (Transmit Mode, COMM and TXOUT Ports)		22	dBm
Channel Temperature, T_{CH}		150	°C
Mounting Temperature (30 seconds)		260	°C
Storage Temperature	−55	150	°C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied. Extended application of Absolute Maximum Rating conditions may reduce device reliability.

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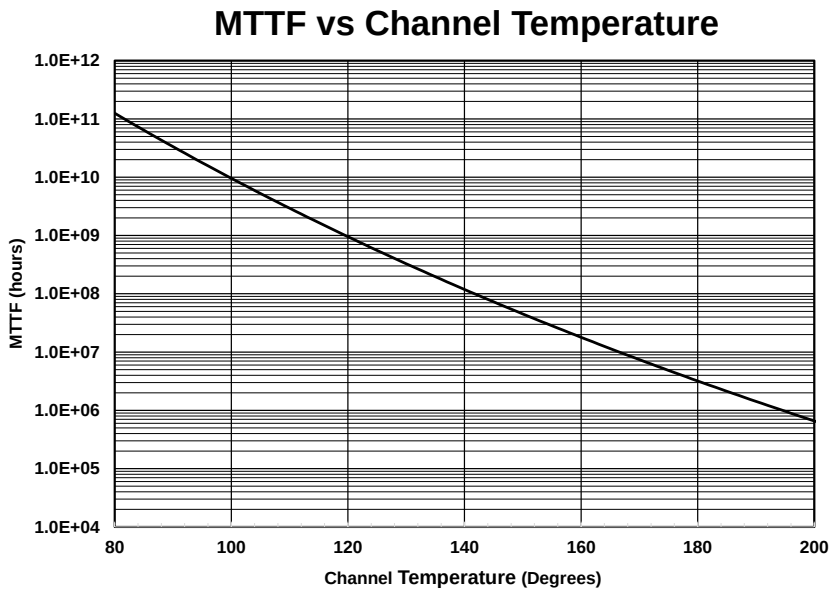
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85 °C VD1 = VD3 = Control Voltage = 3.3 V ID1 + ID3 + MISC Control =187 mA P_{DISS} = 0.62 W (All dies, LNA / RX ON, TX OFF)	33.37	°C/W
Channel Temperature (T_{CH})		105.69	°C
Median Lifetime (T_M)		4.85E09	Hrs

Notes:
1. Thermal resistance is measured to back of the package.

Median Lifetime

Test Conditions: VD = 4 V
Failure Criteria = 10% reduction in I_{D_MAX}



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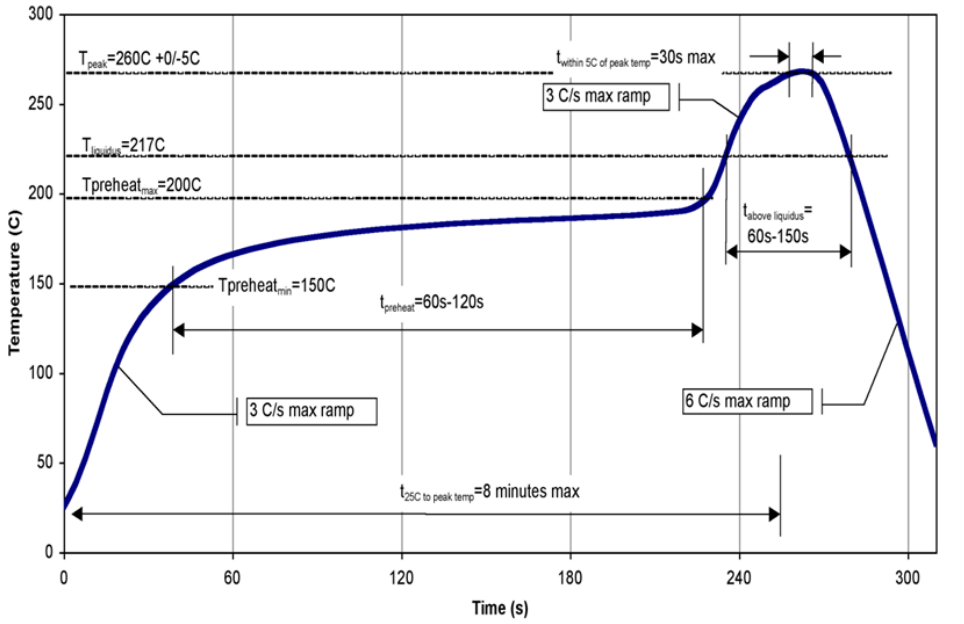
Solderability

1. Compatible with the latest version of J-STD-020, Lead-free solder, 260 °C.

Recommended Soldering Temperature Profile



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Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1A	ESDA / JEDEC JS-001-2017
ESD – Charged Device Model (CDM)	C2A	ESDA / JEDEC JS-002-2014
MSL – Convection Reflow 260 °C	3	JEDEC standard IPC/JEDEC J-STD-020

Caution! JS-002
ESD-Sensitive Device

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Halogen Free (Chlorine, romine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- SVHC Free
- PFOS Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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Web: www.qorvo.com

Email: customer.support@qorvo.com

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