CMD195

DC-20 GHz SPDT Non-reflective Switch

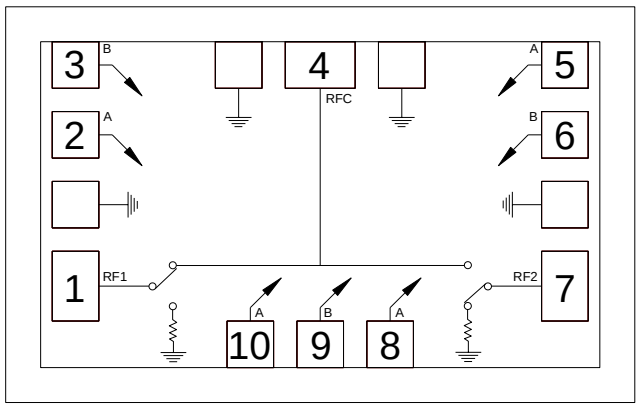
Features

- ► Positive gain slope
- ► High isolation
- ► Fast switching speed
- ► Non-reflective design
- ► Small die size

Description

The CMD195 is a broadband non-reflective GaAs MMIC SPDT switch in die form. The CMD195 covers DC to 20 GHz and offers a low insertion loss of 2 dB and high isolation of 37 dB as well as positive gain slope. The positive gain slope feature allows for several switches to be cascaded together without the need for gain equalization circuitry. The CMD195 die operates using complementary control voltage logic lines of 0/-5 V and requires no bias supply.

Functional Block Diagram



Electrical Performance - V_{ctl} = 0/-5 V, T_A = 25 °C, F = 20 GHz

Parameter	Min	Typ	Max	Units
Frequency Range		DC - 20		GHz
Insertion Loss		2		dB
Isolation		41		dB
Return Loss - On State		17		dB
Return Loss RF1, RF2 - Off State		20		dB
Input P1dB		25		dBm
Switching Characteristics tRISE, tFALL (10/90% RF) tON, tOFF (50% CTL to 10/90% RF)		 1.8 11/4		 ns ns

ver 1.6 0320

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Specifications

Absolute Maximum Ratings

Parameter	Rating
RF Input Power	+27 dBm
Control Voltage Range (A,B)	+0.5V to -7.5V
Channel Temperature, Tch	150 °C
Operating Temperature	-40 to 85 °C
Storage Temperature	-55 to 150 °C
Power Dissipation, Pdiss	
Thermal Resistance, Q_{JC}	

Exceeding any one or combination of the maximum ratings may cause permanent damage to the device.

Control Voltages

State	Bias Condition
Low	0 to -0.5V @ 1 uA Typ
High	-3V @ 1 uA Typ to -7V @ 6 uA Typ

Truth Table

Control Input		Signal Path State	
A	B	RFC to RF1	RFC to RF2
High	Low	On	Off
Low	High	Off	On

Electrical Specifications - V_{ctl} = 0/-5 V, T_A = 25 °C

Parameter	Min	Typ	Max	Min	Typ	Max	Units
Frequency Range		DC - 10			10 - 20		GHz
Insertion Loss		2.4	2.8		2.0	2.5	dB
Isolation	38	48		36	41		dB
Return Loss - On State		13			15		dB
Return Loss - RF1, 2 - Off State		17			20		dB
Input P1dB		25			25		dBm
Input IP3		38			40		dBm
Switching Characteristics tRISE, tFALL (10/90% RF) tON, tOFF (50% CTL to 10/90% RF)		 1.8 11/4			 1.8 11/4		 ns ns

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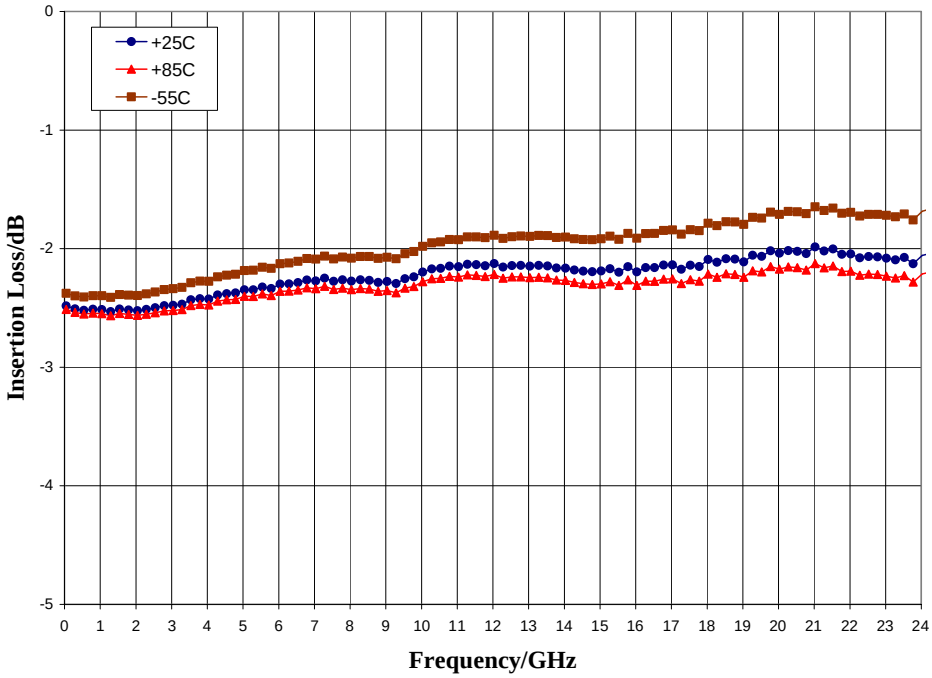
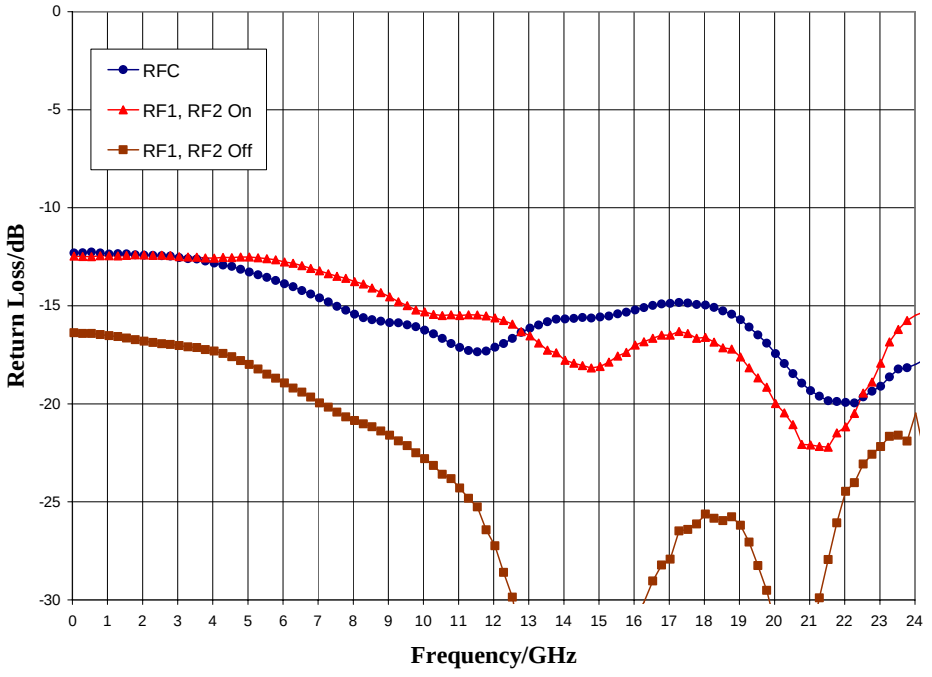
Typical Performance

Insertion Loss vs. Temperature



Return Loss



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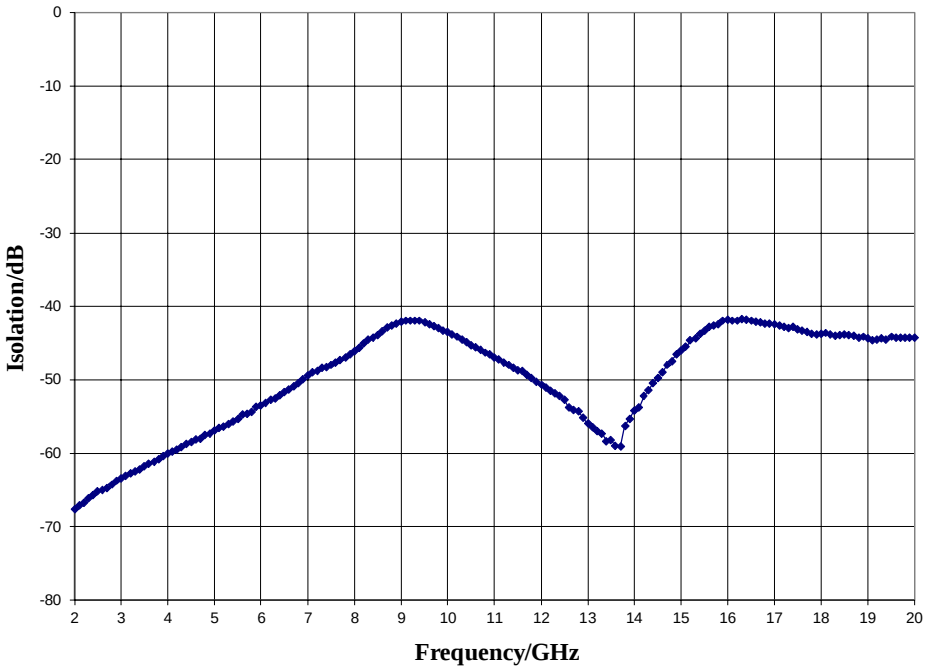
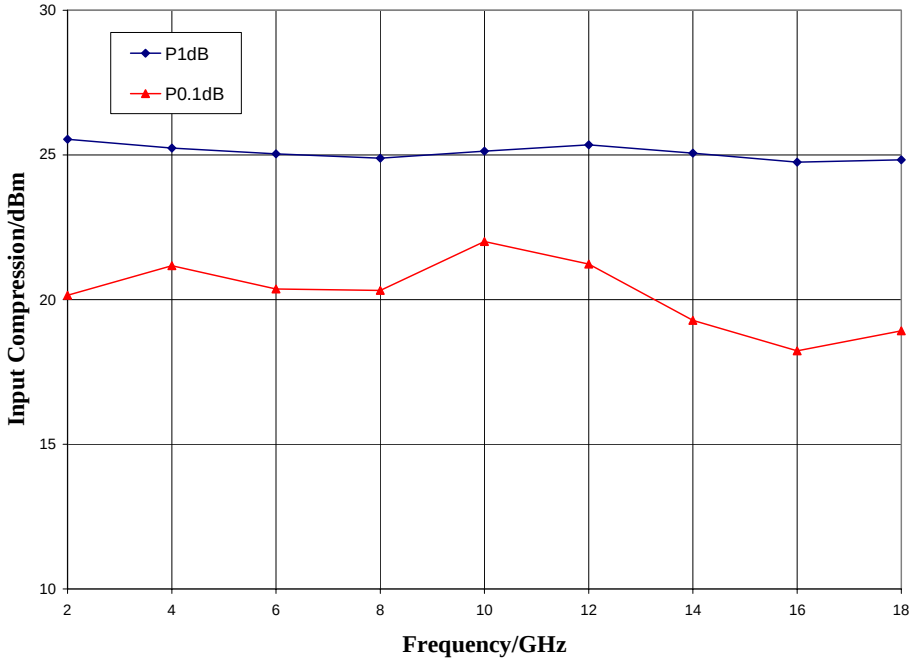
Typical Performance

Isolation Between Ports RFC and RF1/RF2



Input P1dB and P0.1dB Compression Point



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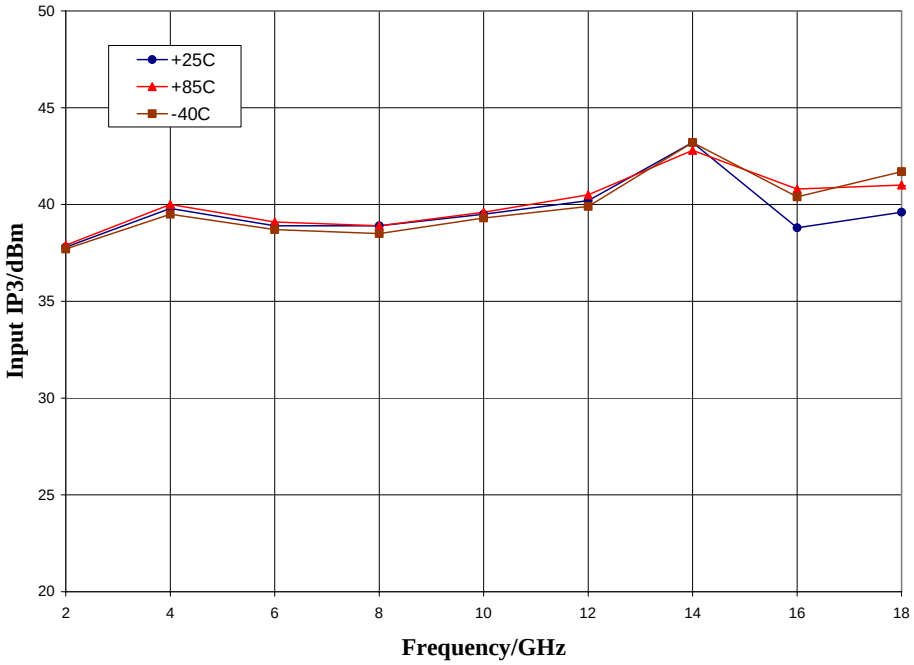
Typical Performance

Input Third Order Intercept Point



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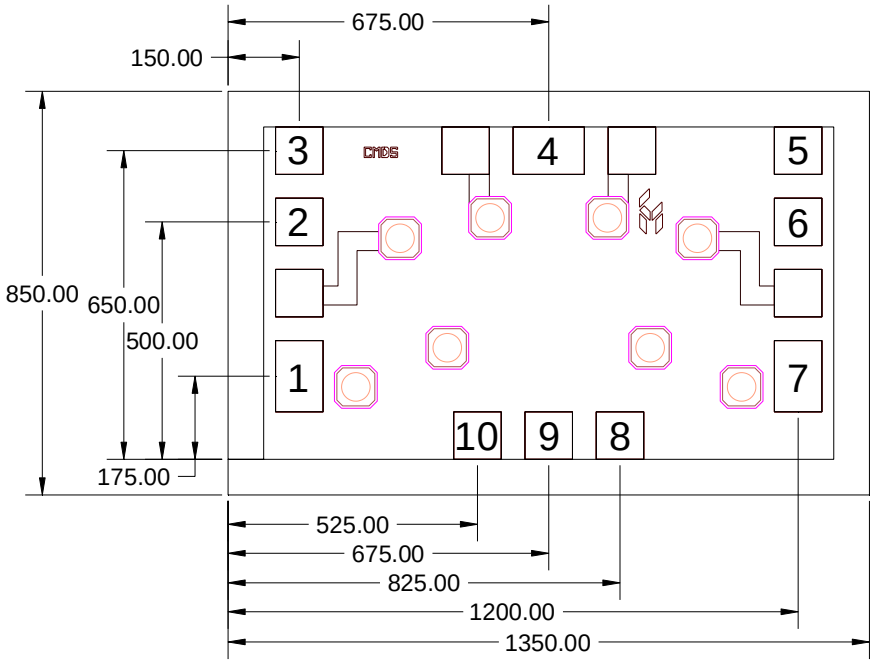
Mechanical Information

Die Outline (all dimensions in microns)



Notes:

1. No connection required for unlabeled pads
2. Backside is RF and DC ground
3. Backside and bond pad metal: Gold
4. Die is 85 microns thick
5. DC bond pads (2, 3, 5, 6, 8, 9, 10) are 100 x 100 microns
6. RF bond pads (1, 4, 7) are 100 x 150 microns

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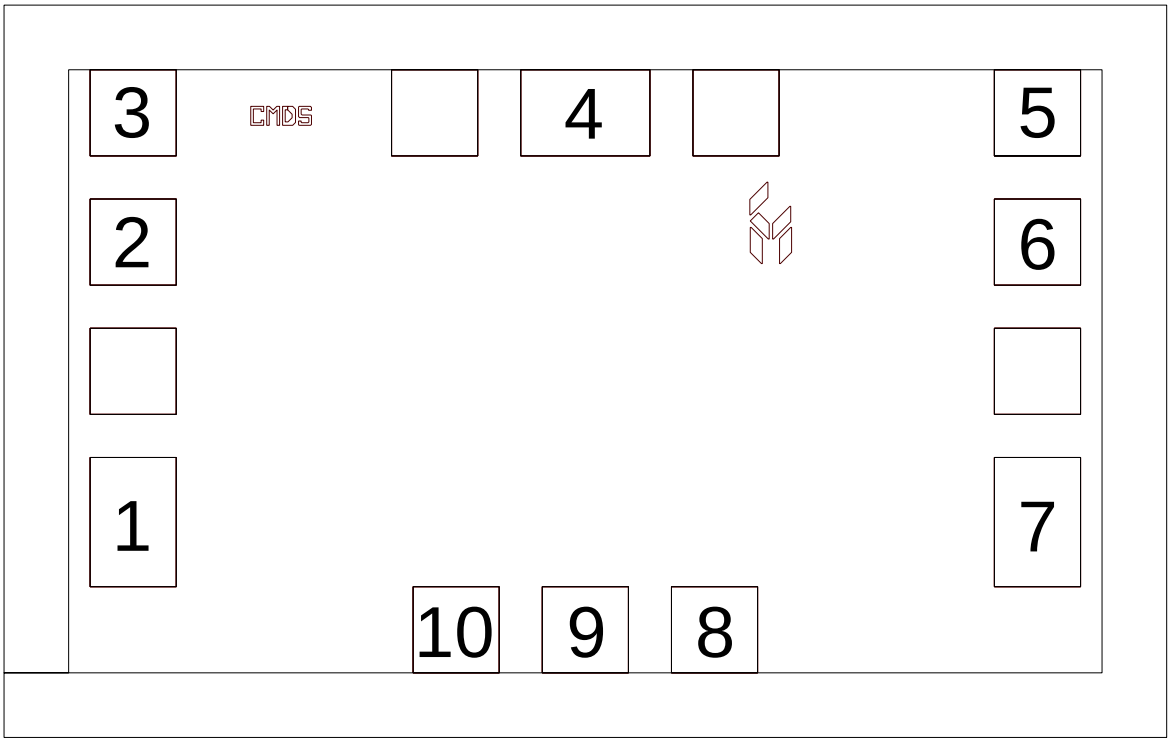
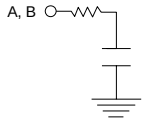
Pad Description

Pad Diagram



Functional Description

Pin	Function	Description	Schematic
1, 4, 7	RF1, RFC, RF2	These pins are DC coupled and matched to 50 Ohm. Blocking capacitors are required if RF line potential is not equal to 0V	
2, 5, 8, 10	CTRLA	See truth table and control voltage table	
3, 6, 9	CTRLB	See truth table and control voltage table	
Backside	Ground	Connect to RF / DC ground	

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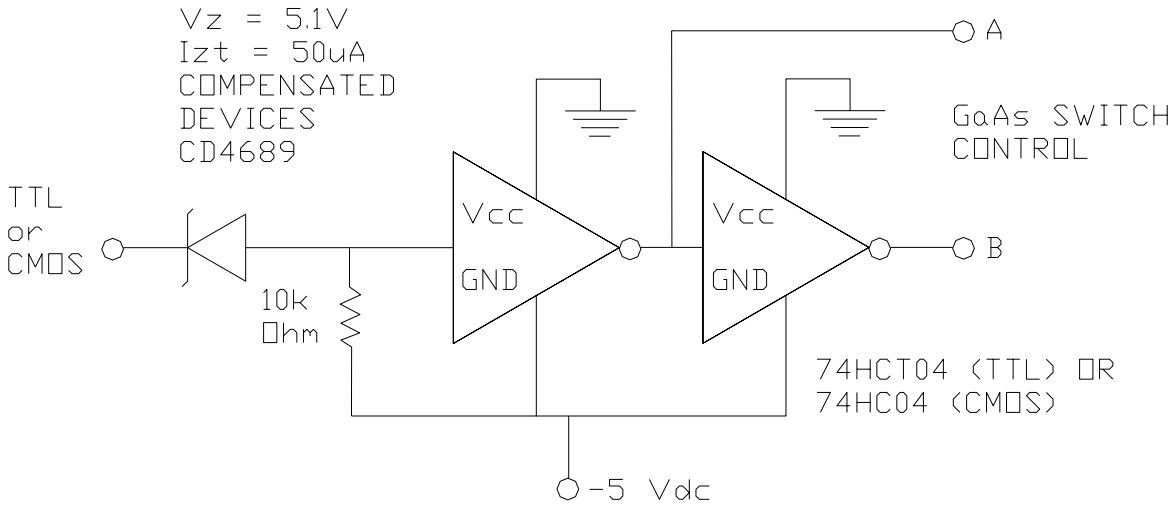
Applications Information

Suggested Driver Circuit



GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

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Applications Information

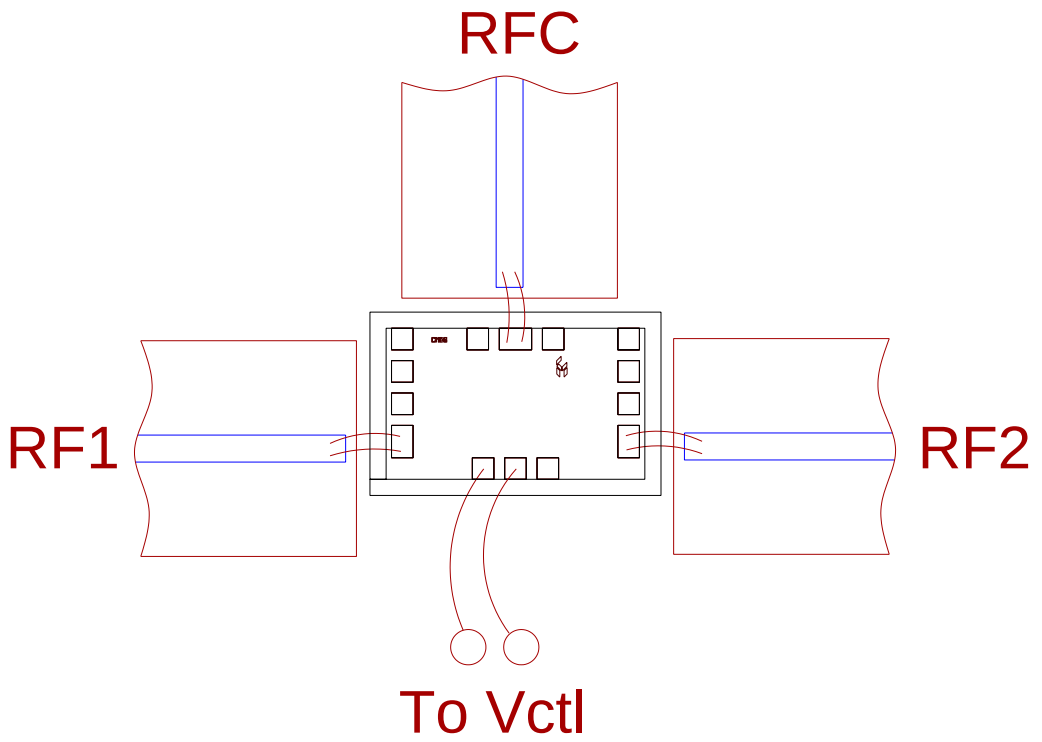
Assembly Guidelines

The backside of the CMD195 is RF ground. Die attach should be accomplished with electrically and thermally conductive epoxy only. Eutectic attach is not recommended. Standard assembly procedures should be followed for high frequency devices. The top surface of the semiconductor should be made planar to the adjacent RF transmission lines, and the RF decoupling capacitors placed in close proximity to the DC connections on chip.

RF connections should be made as short as possible to reduce the inductive effect of the bond wire. Use of a 0.8 mil thermosonic wedge bonding is highly recommended as the loop height will be minimized. The RF inputs and outputs require a double bond wire as shown.

The semiconductor is 85 um thick and should be handled by the sides of the die or with a custom collet. Do not make contact directly with the die surface as this will damage the monolithic circuitry. Handle with care.

Assembly Diagram



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