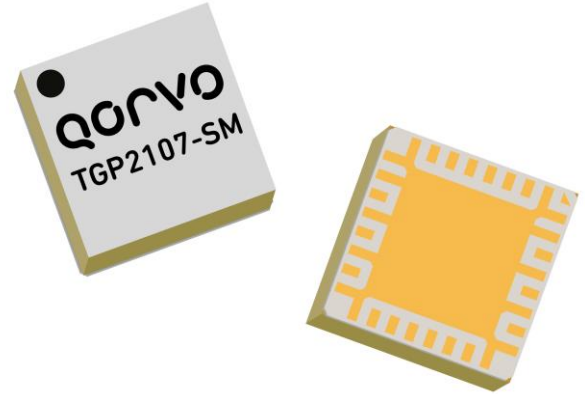


Product Description

The Qorvo TGP2107-SM is a packaged 6-bit digital phase shifter, fabricated on Qorvo's high performance 0.15 μm GaAs pHEMT process. It operates over 6 to 18 GHz and provides 360° of phase coverage with a LSB of 5.625°. It also achieves a low RMS phase error of 5° with 8 dB of insertion loss over all states.

The TGP2107-SM uses negative switch logic, eliminating the need for a reference voltage. That, along with low insertion and a high degree of resolution makes the TGP2107-SM ideally suited for a variety of wideband phased array applications, including commercial and military radars, satellite-based communication systems and electronic warfare.



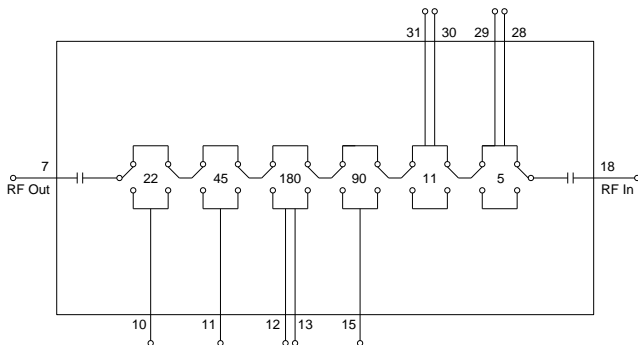
Air Cavity Ceramic QFN 5x5 mm 32L

Product Features

- Frequency Range: 6 to 18 GHz
- 6-Bit Digital Phase Shifter
- 360° Coverage, LSB = 5.625°
- RMS Phase Error: 5°
- RMS Amplitude Error: 0.55 dB
- Insertion Loss: <10 dB
- Return Loss: >12 dB
- Input P1dB: >25 dBm
- Input IP3: >41 dBm
- Switching Speed: < 40ns
- Control Voltage: -5/0 V
- Package Dimensions: 5.0 x 5.0 x 1.45 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Block Diagram



Applications

- Phased Array Antenna Systems
- Satellite Communication Systems
- Electronic Warfare

Ordering Information

Part No.	Description
TGP2107-SM	6-18 GHz 6-Bit Digital Phase Shifter (-Vc)
TGP2107-SMEVB	TGP2107-SM EVAL BOARD

Absolute Maximum Ratings

Parameter	Value
Control and Reference Voltage	6 V
Control Current	-15 to +5 mA
Power Dissipation	0.9 W
Input Power, CW, 50 Ω, 85°C	30 dBm
Channel Temperature	200 °C
Mounting Temperature (30 Seconds)	260 °C
Storage Temperature	-55 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied. Extended application of Absolute Maximum Rating conditions may reduce device reliability.

Recommended Operating Conditions

Parameter	Value
Control Voltage (5N, 5P, 11N, 11P, 22, 45, 90, 180N, 180P)	-5/0 V
Temperature Range	-40 to +85 °C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed overall operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: 25°C. Control Voltage (5N, 5P, 11N, 11P, 22, 45, 90, 180N, 180P) = -5/0 V; See Bias Truth Table.

Parameter	Conditions	Min	Typical	Max	Units
Operational Frequency Range		6		18	GHz
Insertion Loss			6 to 10		dB
Input Return Loss			>12		dB
Output Return Loss			>12		dB
RMS Phase Error			5		deg
RMS Amplitude Error			0.55		dB
Input P1dB			>25		dBm
Input IP3	Spacing = 10 MHz, Pin/Tone = 8 dBm		45		dBm
Insertion Loss Temperature Coefficient			0.008		dB/°C

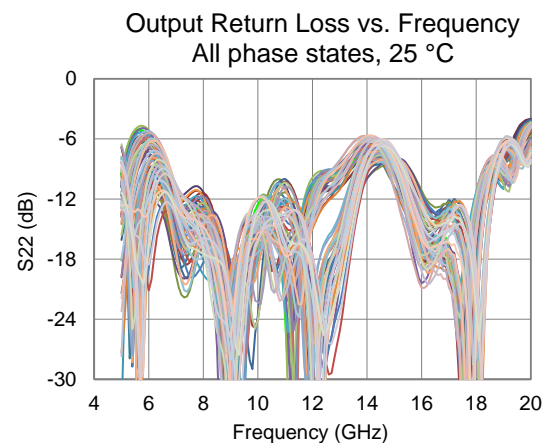
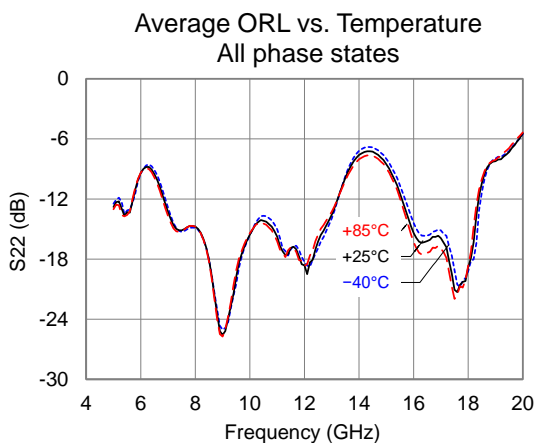
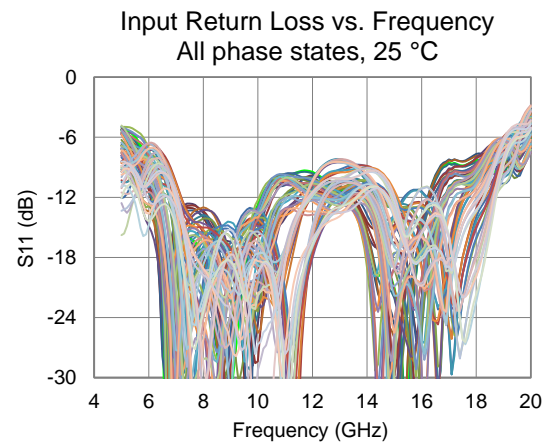
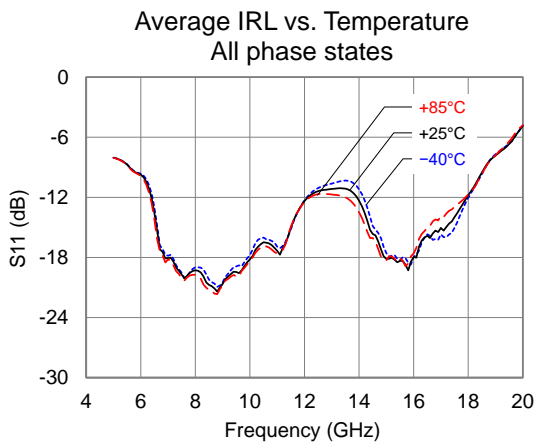
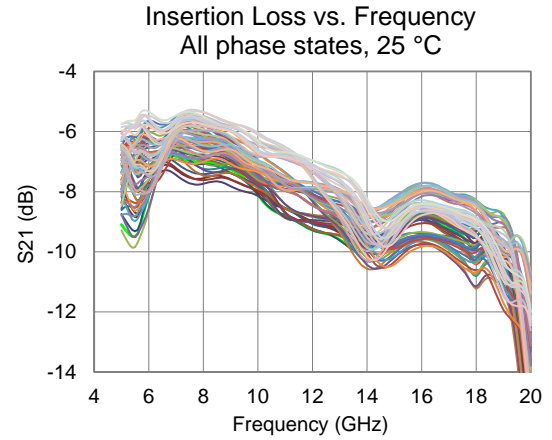
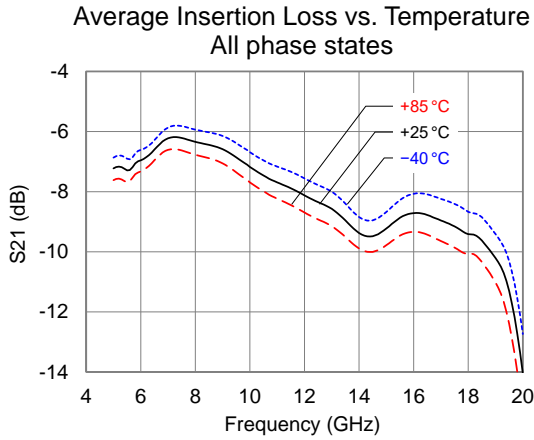
Bias Truth Table

Logic "0" = -5 V, Logic "1" = 0 V

Phase Shifter	5P	5N	11P	11N	22	45	90	180P	180N
0° (Reference)	0	1	0	1	0	0	0	0	1
5°	1	0	0	1	0	0	0	0	1
11°	0	1	1	0	0	0	0	0	1
22°	0	1	0	1	1	0	0	0	1
45°	0	1	0	1	0	1	0	0	1
90°	0	1	0	1	0	0	1	0	1
180°	0	1	0	1	0	0	0	1	0
355°	1	0	1	0	1	1	1	1	0

Performance Plots – Small Signal

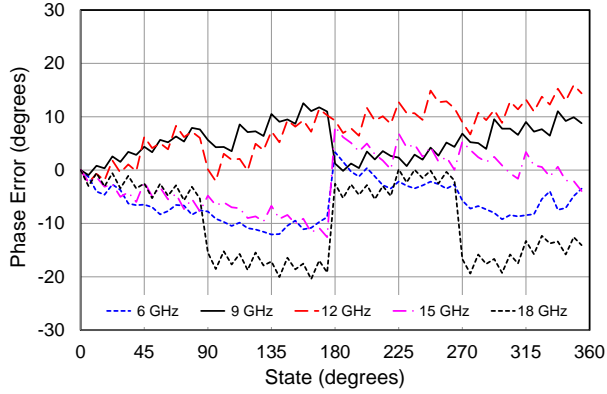
Test conditions unless otherwise noted: -5V, 25 °C



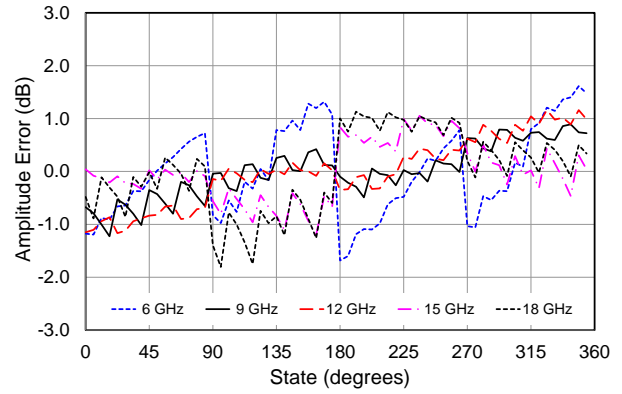
Performance Plots – Small Signal (Cont.)

Test conditions unless otherwise noted: -5V, 25 °C

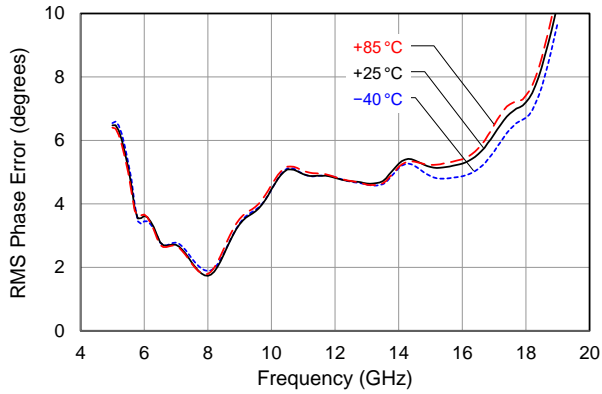
Phase Error vs. State
25 °C



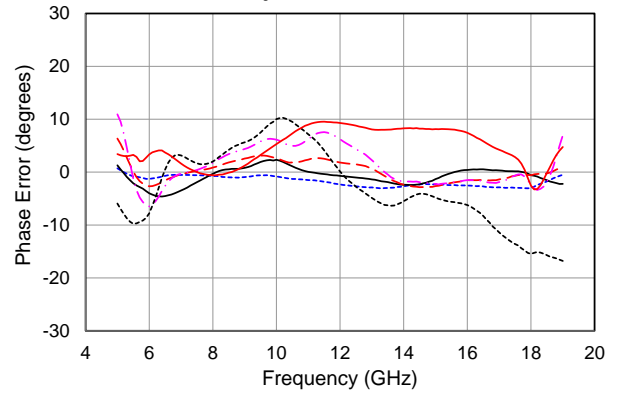
Amplitude Error (relative to mean) vs. State
25 °C



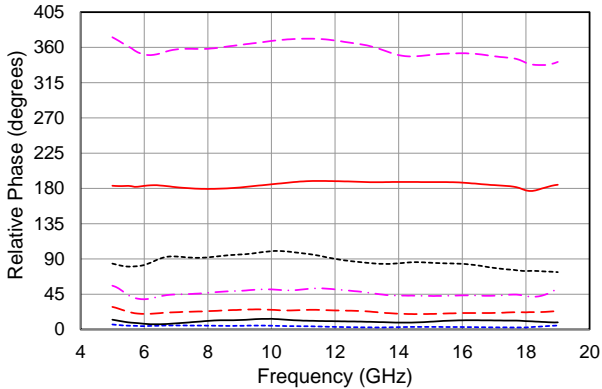
RMS Phase Error vs. Frequency
All Phase States, 25 °C



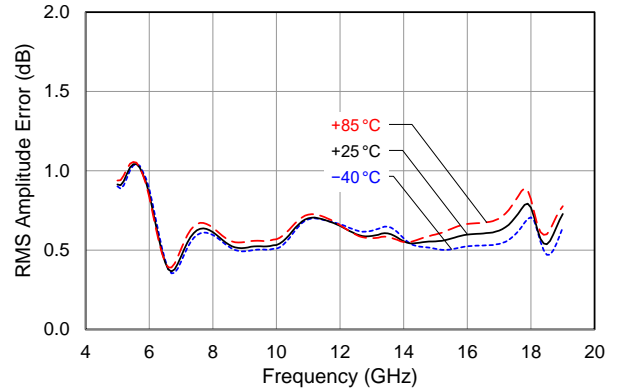
Phase Error vs. Frequency
Major States, 25 °C



Relative Phase Shift vs. Frequency
Major States, 25 °C

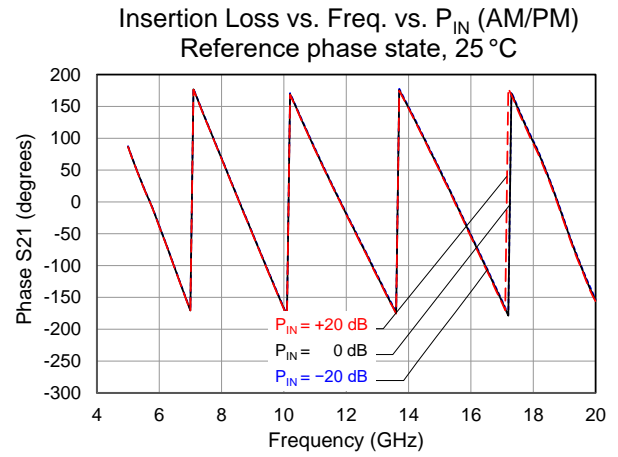
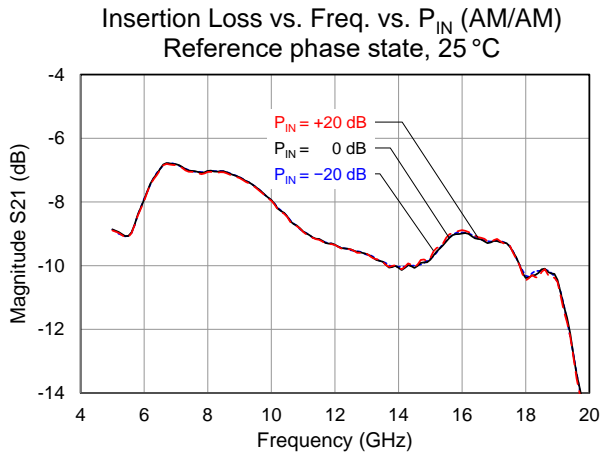


RMS Amplitude Error vs. Frequency
All Phase States, 25 °C



Performance Plots – Small Signal (Cont.)

Test conditions unless otherwise noted: -5V, 25 °C



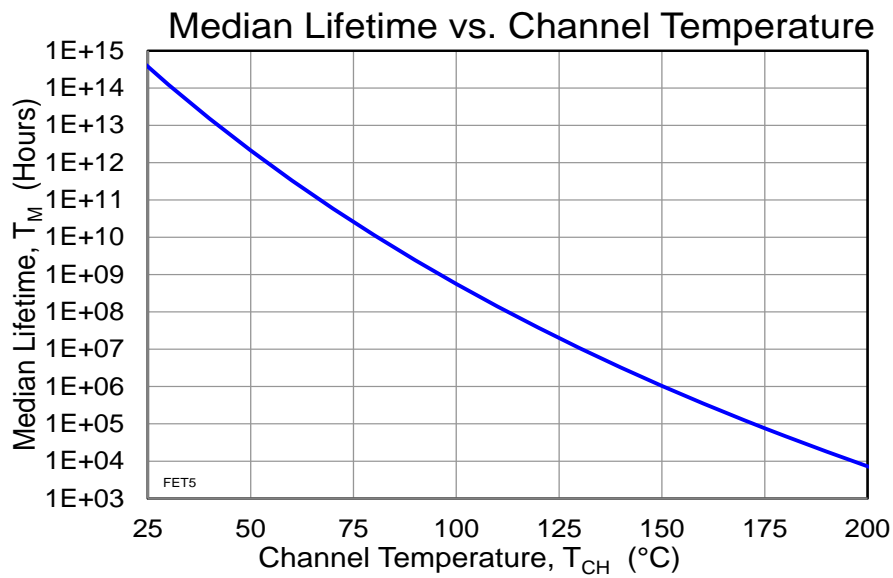
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) ⁽¹⁾	$P_{DISS} = 0.09 \text{ W}$, $T_{BASE} = 85^\circ\text{C}$	22	$^\circ\text{C/W}$
Channel Temperature (T_{CH})		87	$^\circ\text{C}$
Median Lifetime (T_M)		3.8E+9	Hrs

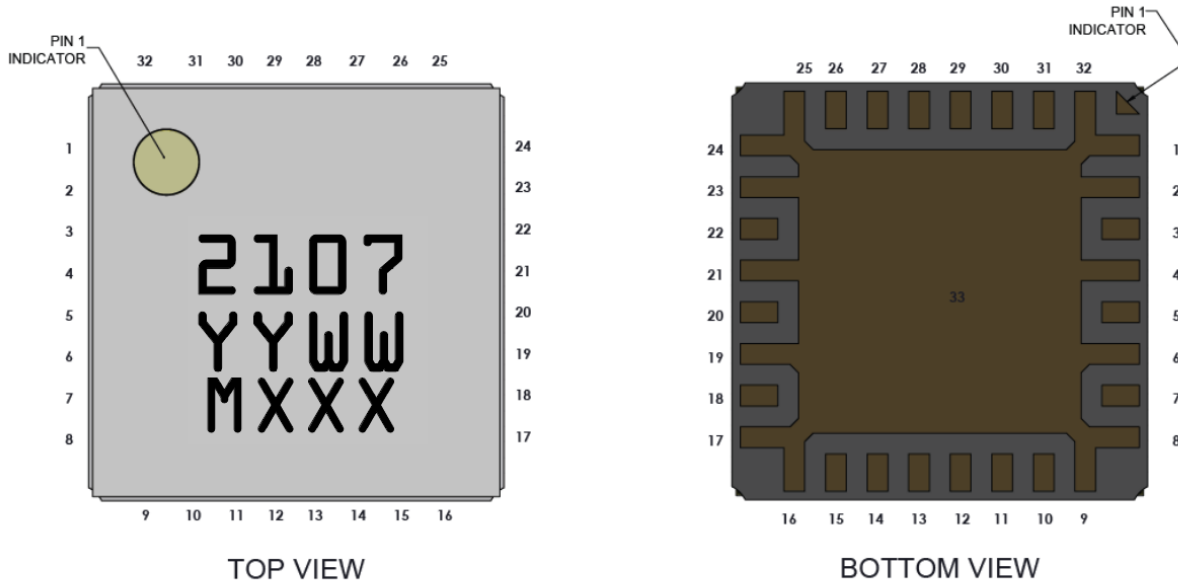
Notes:

1. Thermal resistance measured to back of package.

Median Lifetime

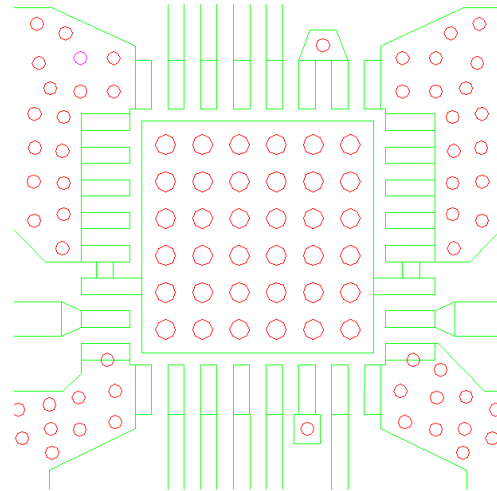
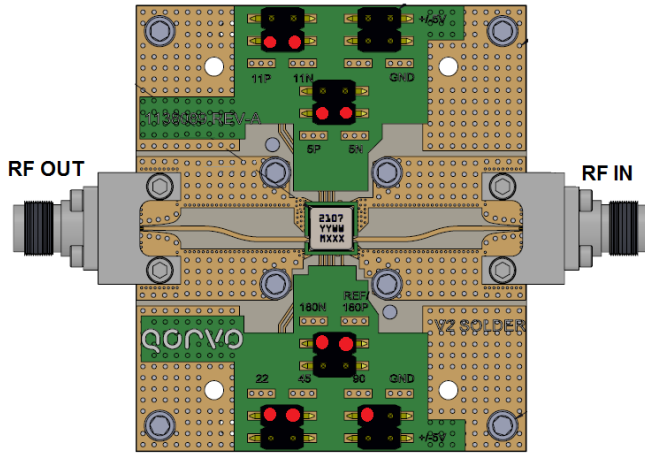


Pin Description



Pin No.	Symbol	Description
1 - 6, 8 - 9, 14, 16 - 17, 19 – 27, 32	GND	Internal grounding; must be grounded on PCB
7	RF OUT	Output; matched to 50 Ω; DC blocked
10	22°	22° Bit; De-Qing network is not required
11	45°	45° Bit; De-Qing network is not required
12	180N°	180N° Bit; De-Qing network is not required
13	180P°	180P° Bit; De-Qing network is not required
15	90°	90° Bit; De-Qing network is not required
18	RF IN	Input; matched to 50 Ω; DC blocked
28	5N°	5N° Bit; De-Qing network is not required
29	5P°	5P° Bit; De-Qing network is not required
30	11N°	11N° Bit; De-Qing network is not required
31	11P°	11P° Bit; De-Qing network is not required
33	GND	Backside Paddle; multiple vias should be employed to minimize inductance and thermal resistance

Evaluation Board (EVB) Layout Assembly



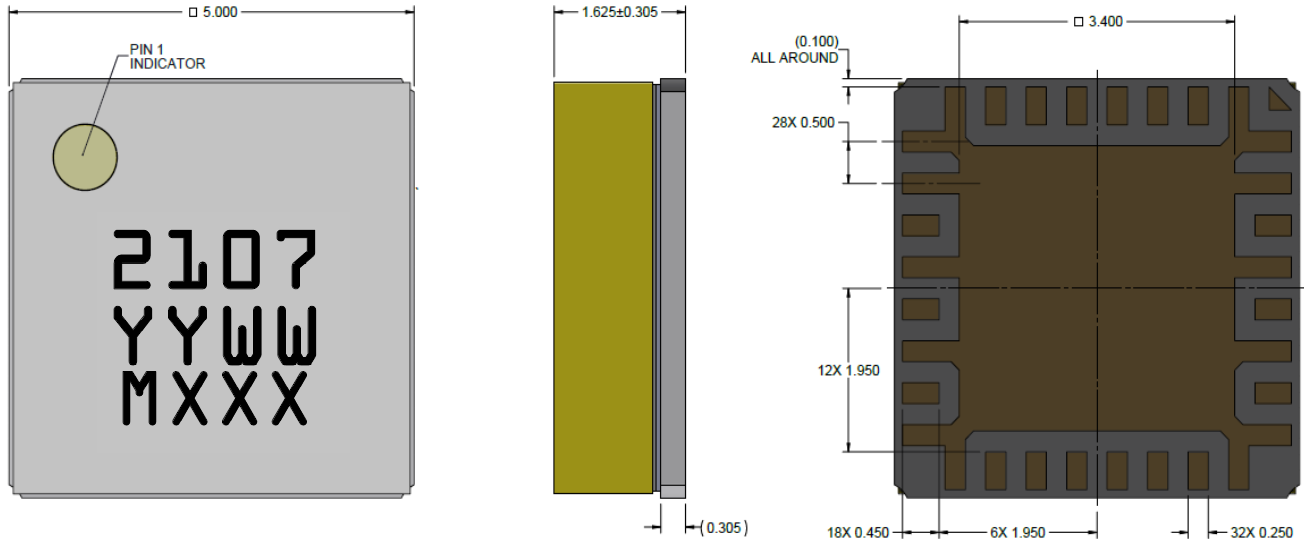
Via pattern

RF layer is 0.010" thick Rogers RO4350. Metal layers are 1-oz copper. The microstrip line taper at the connector interface is optimized for the Southwest Microwave end-launch connector 1092-01A-5.

Ground / thermal vias under the DUT are critical for the proper performance of this device. The PCB shown herein utilizes copper filled vias under the DUT.

The pad pattern shown has been developed and tested for optimized assembly at Qorvo. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company careful process development is recommended.

Mechanical Information



Package lead finish:

Ni / Au plating with minimum gold thickness of 0.5 μm

Materials:

Base: Ceramic, Lid: Laminate, Part is epoxy sealed

Part Marking:

2107 = Part Number, YY = Part Assembly Year, WW = Part Assembly Week, MXXX = Batch ID

Unless otherwise specified dimensions are in mm.

Tolerances: XXX = ± 0.127

Assembly Notes

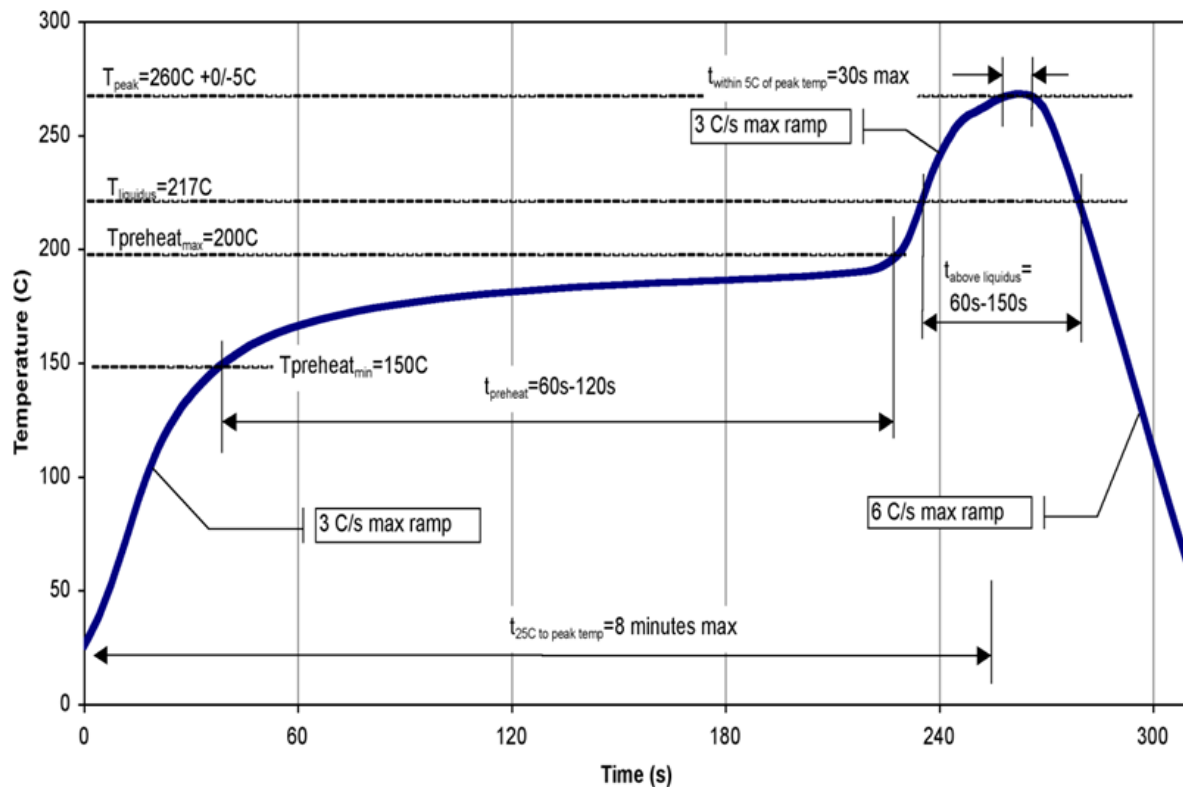
Compatible with both lead-free (260°C peak reflow temp.) and tin/lead (245°C peak reflow temp.) soldering processes.

This package is air-cavity and non-hermetic, and therefore cannot be subjected to aqueous washing. The use of no-clean solder to avoid washing after soldering is highly recommended.

Solder rework not recommended.

Contact plating: Ni-Au.

Recommended Soldering Temperature Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 0B	ESDA / JEDEC JS-001-2012
ESD – Charge Device Model (CDM)	Class C1	JS-002-2014
MSL – Moisture Sensitivity Level	Level 5a	IPC/JEDEC J-STD-020



Caution!
ESD-Sensitive Device

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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Web: www.qorvo.com

Email: customer.support@qorvo.com

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