QPA3055P

100 W S-Band GaN Power Amplifier

Product Overview

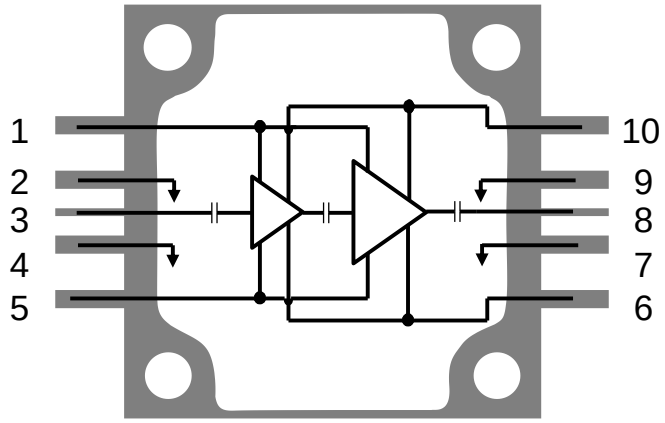
Qorvo's QPA3055P is a packaged, high-power S-band amplifier fabricated on Qorvo's production 0.25 um GaN on SiC process (QGaN25). Covering 2.9 – 3.5 GHz, the QPA3055P provides 100 W of saturated output power and 25 dB of large-signal gain while achieving 53% power-added efficiency.

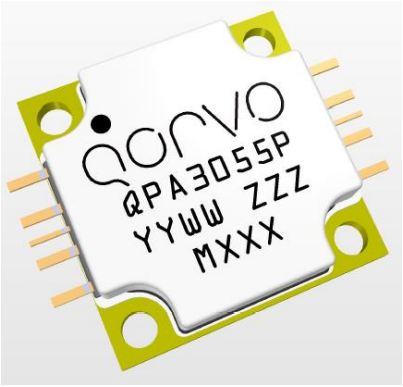
The QPA3055P is packaged in a 10-lead 15.2 x 15.2 mm bolt-down package with a Cu base for superior thermal management. It can support a variety of operating conditions to best support system requirements. With good thermal properties, it can support a range of bias voltages and will perform well under both short and long pulse operations.

The QPA3055P MMIC has DC blocking capacitors on both RF ports, which are matched to 50 ohms. The QPA3055P is ideal for both commercial and military radar systems.

RoHS compliant.

Functional Block Diagram





Key Features

- Frequency Range: 2.9 – 3.5 GHz
- P_{SAT} (P_{IN}=25 dBm): 50 dBm
- PAE (P_{IN}=25 dBm): > 53 %
- Power Gain (P_{IN}=25 dBm): 25 dB
- Bias: V_D = 30 V, I_{DQ} = 300 mA, P_{IN} = 25 dBm
- Alt. Bias: V_D = 30 V, I_{DQ} = 1500 mA, P_{IN} = 22 dBm
- Characterized at PW = 15 ms, DC = 30%, and PW = 100 us, DC = 10%
- Package Dimensions: 15.2 x 15.2 x 3.5 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Applications

- Radar

Ordering Information

Part No.	Description
QPA3055P	100 W S-Band GaN Power Amplifier (10 Pcs.)
QPA3055PS2	Samples (2 pcs.)
QPA3055PEVB1	Evaluation Board for QPA3055P

Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage (V_D)	40 V
Gate Voltage Range (V_G)	−8 to +1 V
Peak Drain Current (I_D)	11.7 A
Average Drain Current (I_D)	5.7 A
Duty Cycle	50%
Gate Current (I_G)	300 mA
Power Dissipation (P_{DISS}), 85 °C	150 W
Input Power (P_{IN}), Pulsed (15 ms, 30%), 50 Ω, V_D=28 V, I_{DQ}=300 mA, 85 °C	31 dBm
Input Power (P_{IN}), Pulsed (15 ms, 30%), 3:1 VSWR, V_D=28 V, I_{DQ}=300 mA, 85 °C	31 dBm
Channel Temperature (T_{CH})	275 °C
Mounting Temperature	Refer to Assembly Notes, page 25
Storage Temperature	−65 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value / Range
Drain Voltage (V_D)	30 V
Drain Current (I_{DQ})	300 mA
Gate Voltage (V_G), Typical	−2.5 V
Operating Temperature	−40 to +85 °C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

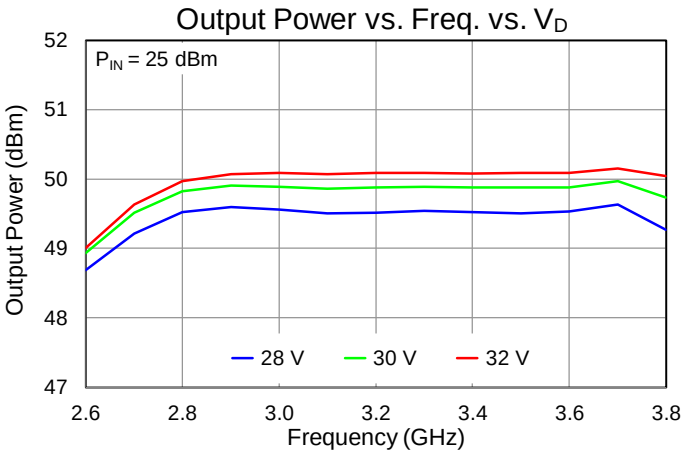
Electrical Specifications

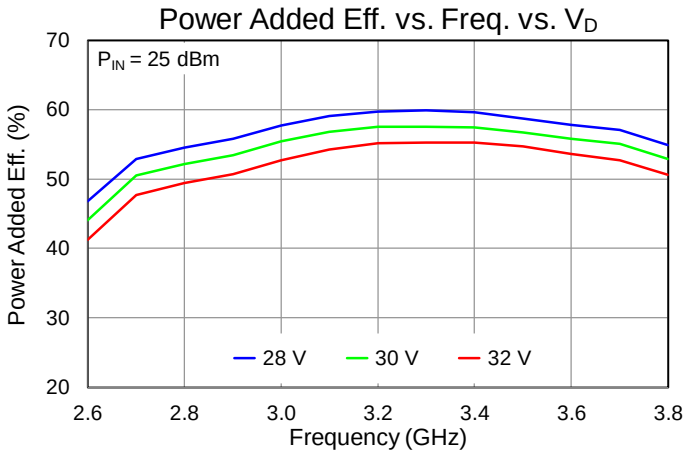
Parameter		Min	Typ	Max	Units
Operational Frequency Range		2.9		3.6	GHz
Output Power (P_{IN} = 25 dBm)	2.9 GHz 3.2 GHz 3.5 GHz		50 50 50		dBm dBm dBm
Power Added Efficiency (P_{IN} = 25 dBm)	2.9 GHz 3.2 GHz 3.5 GHz		53.5 57.5 56.5		% % %
Small Signal Gain (CW)	2.9 GHz 3.2 GHz 3.5 GHz		30.0 32.0 29.5		dB dB dB
Input Return Loss (CW)	2.9 GHz 3.2 GHz 3.5 GHz		19 17 22		dB dB dB
Output Return Loss (CW)	2.9 GHz 3.2 GHz 3.5 GHz		7 6 14		dB dB dB
P_{OUT} Temp. Coeff. (85 – 25 °C, P_{IN} = 25 dBm))			0.001		dB/°C
Sm. Sig. Gain Temp. Coefficient (85 to −40 °C, CW)			-0.059		dB/°C

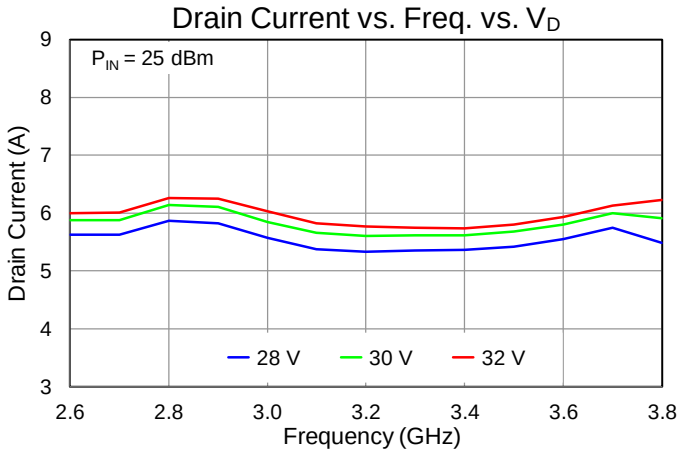
Test conditions, unless otherwise noted: T = 25 °C, V_D = 28 V, I_{DQ} = 300 mA, V_G = −2.5 V Typical, PW = 15 ms, Duty Cycle = 30%

Performance Plots – Large Signal (I_{DQ}=300 mA, PW=15 ms, DC=30%)

Test conditions unless otherwise noted: V_D = 28 V, I_{DQ} = 300 mA, T= +25 °C







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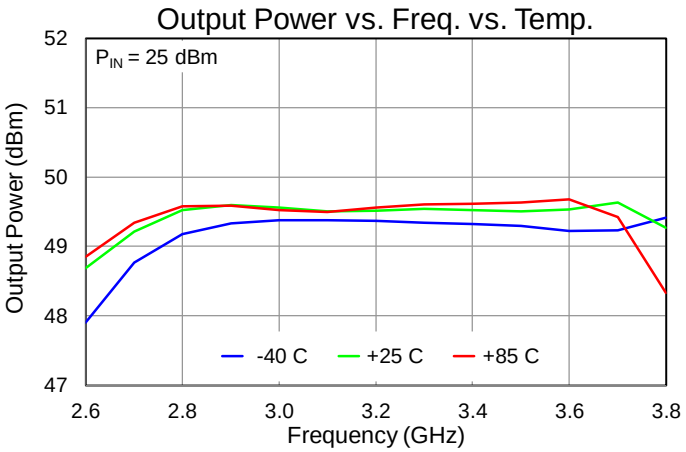

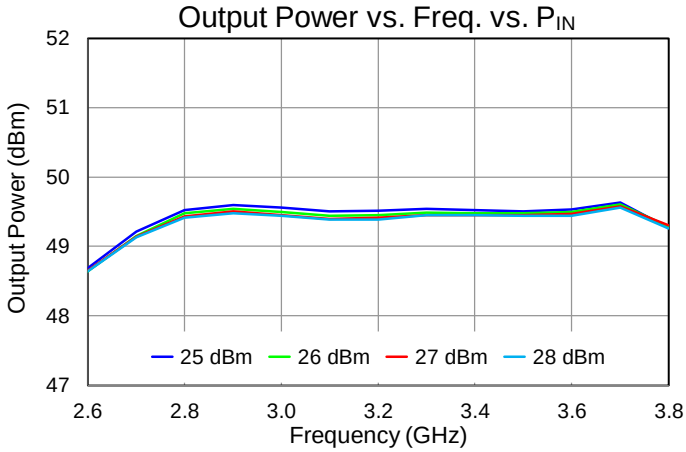

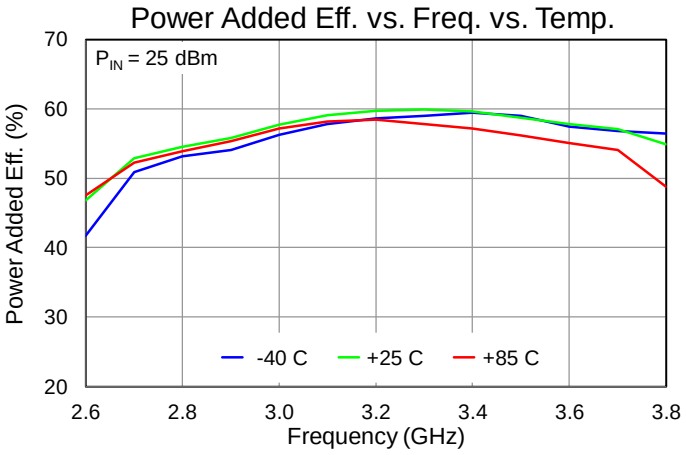

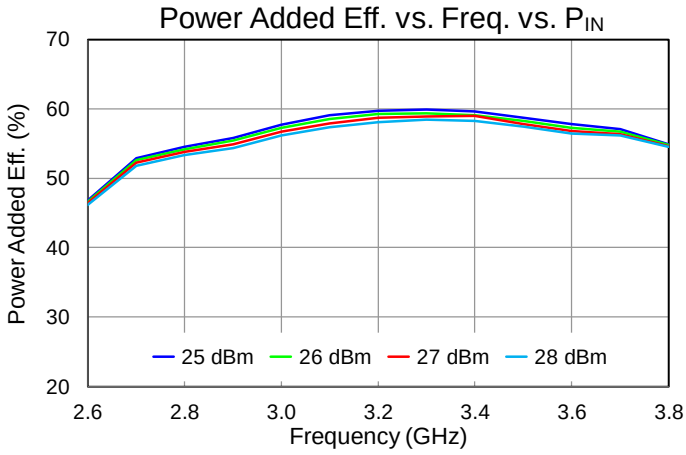

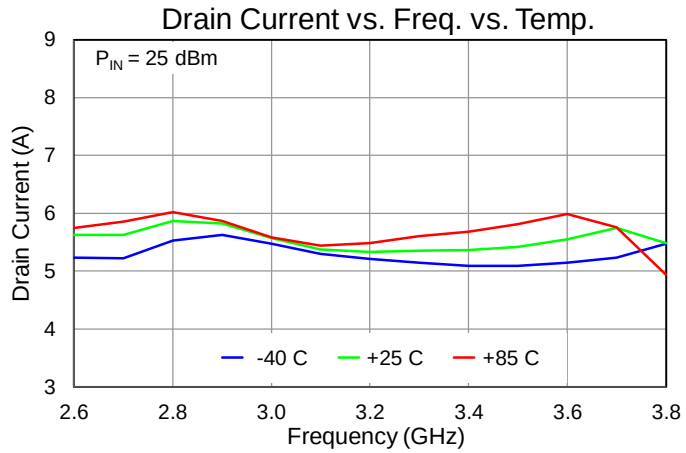

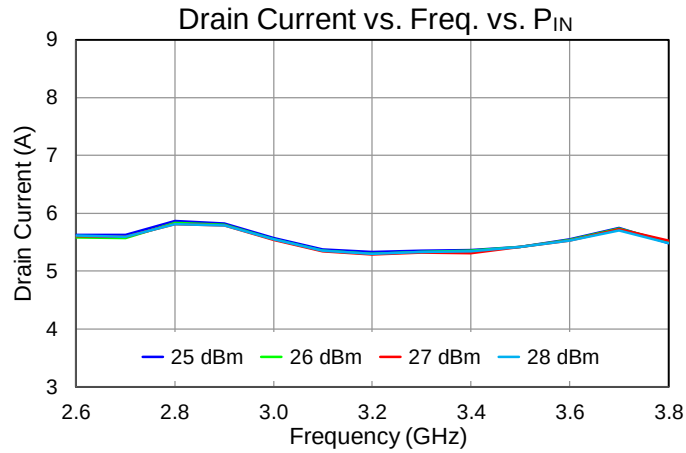

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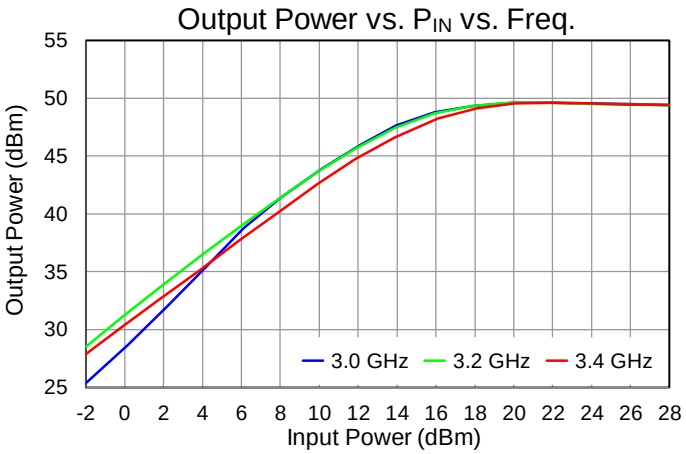

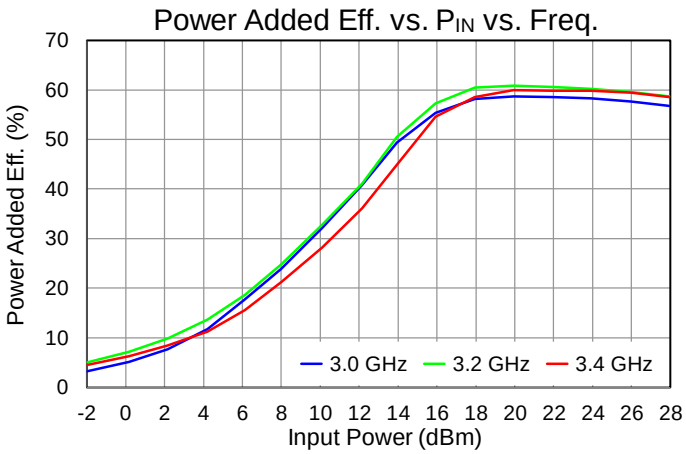

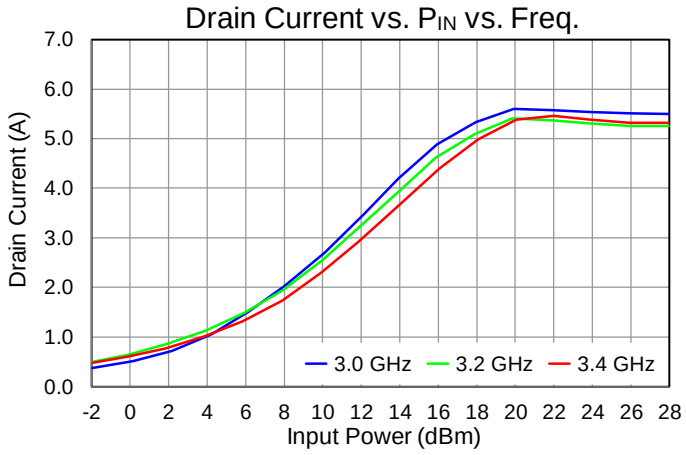

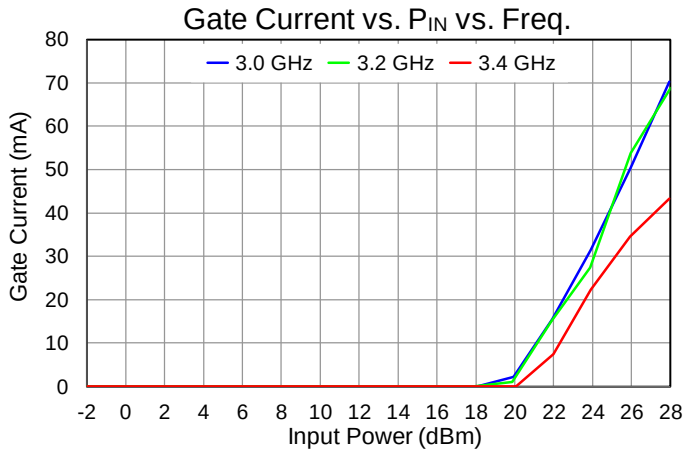

Performance Plots – Large Signal, Harmonics (I_{DQ}=300 mA, PW=15 ms, DC=30%)

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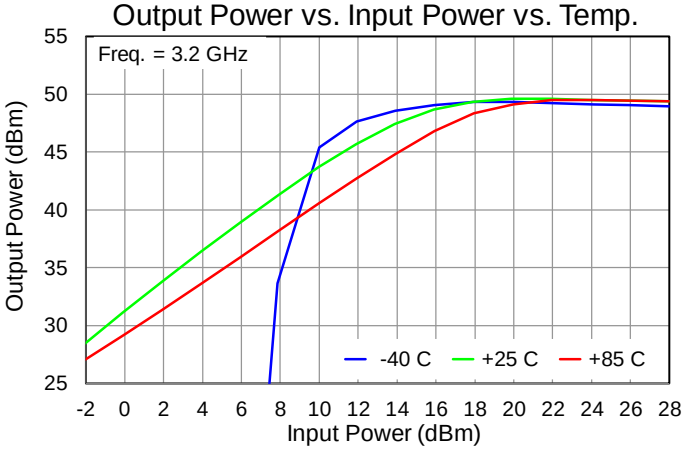
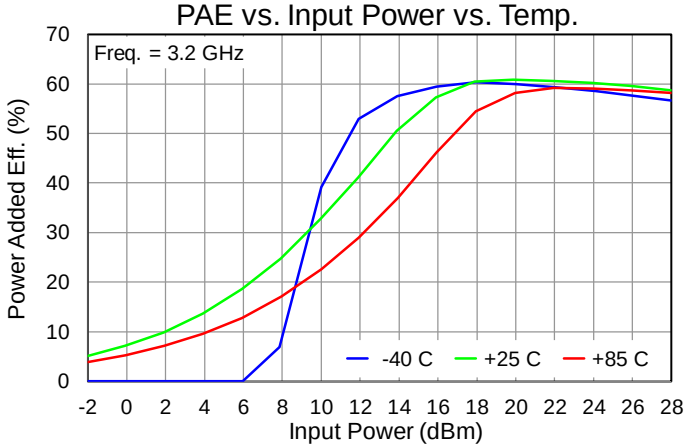
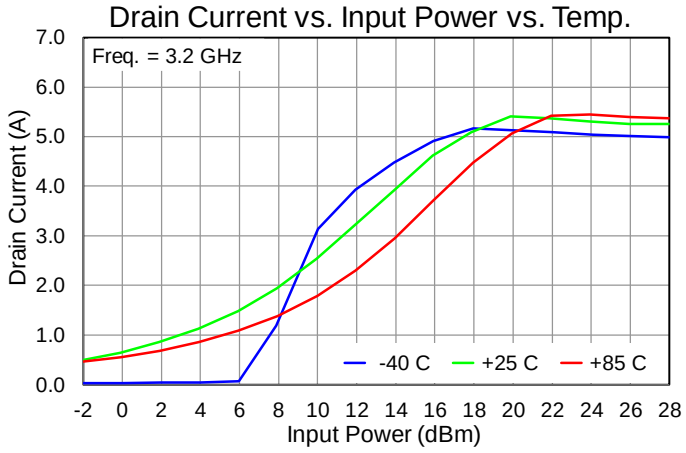
Output Power vs. Input Power vs. Temp.



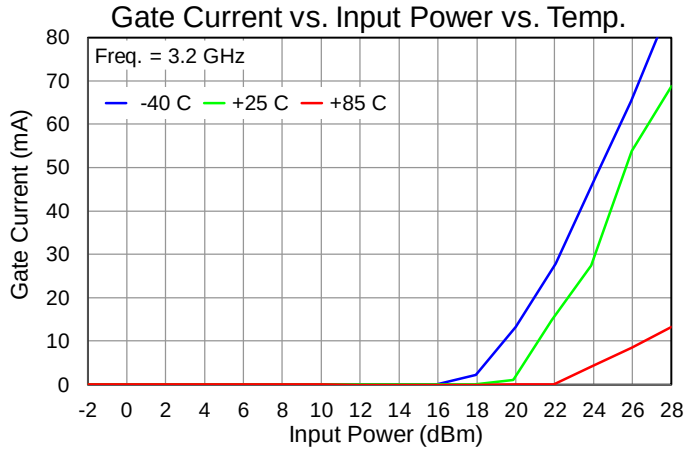
PAE vs. Input Power vs. Temp.



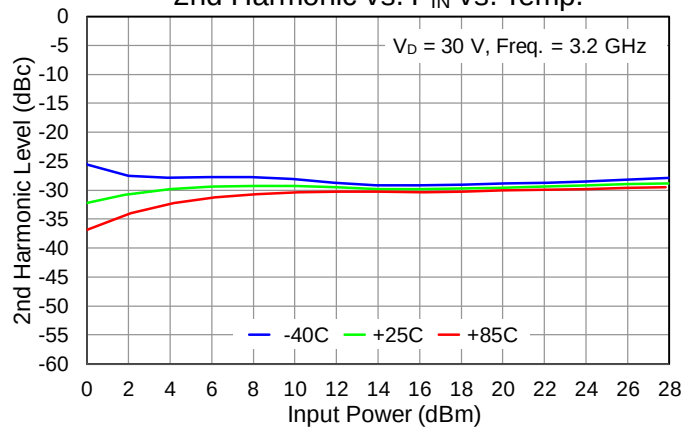
Drain Current vs. Input Power vs. Temp.



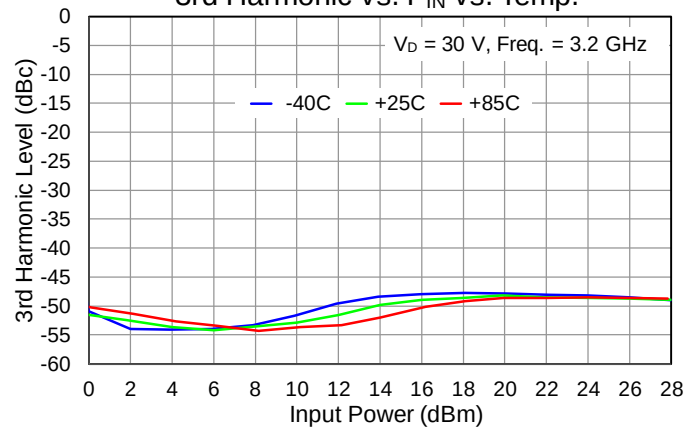
Gate Current vs. Input Power vs. Temp.



2nd Harmonic vs. P_{IN} vs. Temp.

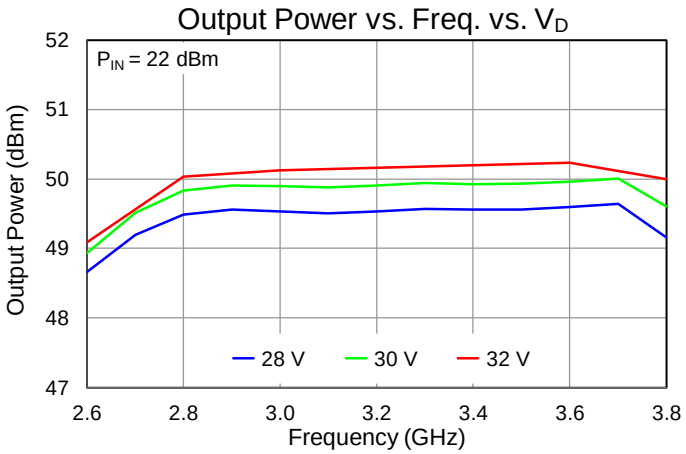


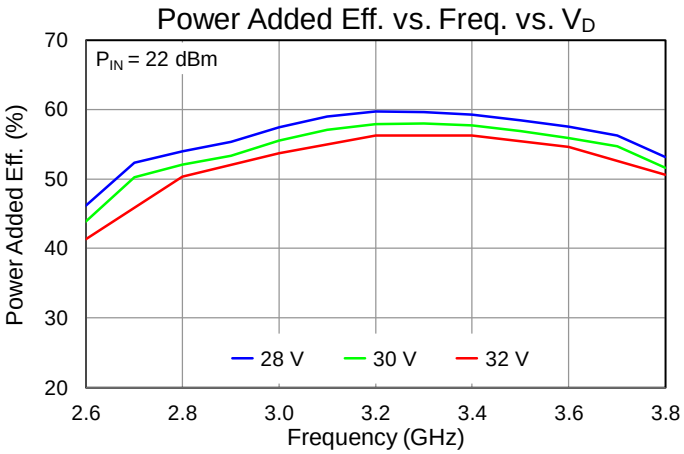
3rd Harmonic vs. P_{IN} vs. Temp.

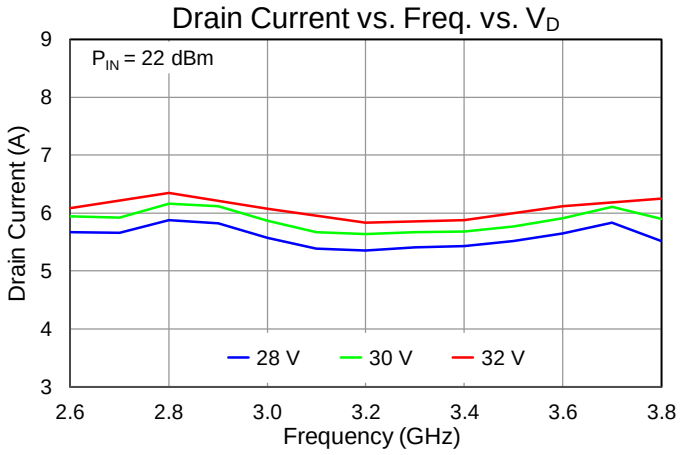


Performance Plots – Large Signal (I_{DQ}=1.5 A, PW=15 ms, DC=30%)

Test conditions unless otherwise noted: V_D = 28 V, I_{DQ} = 1.5 A, T= +25 °C







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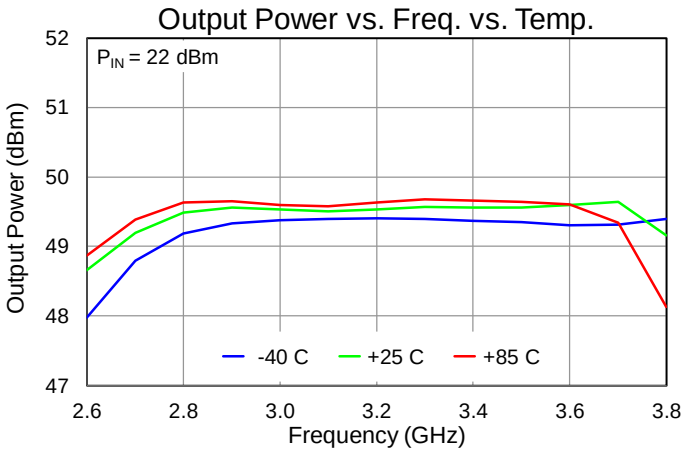

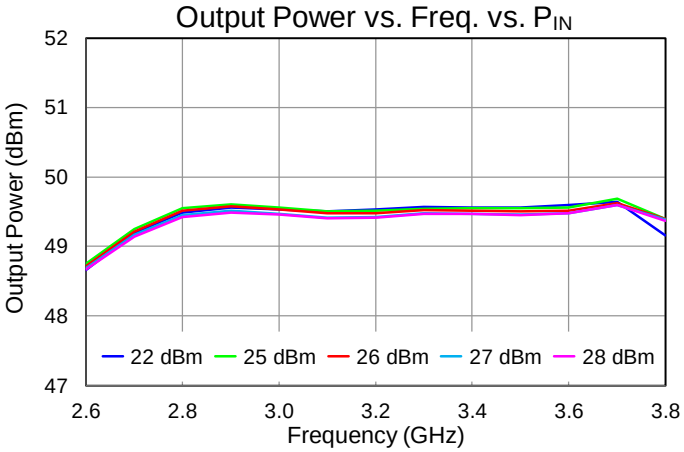

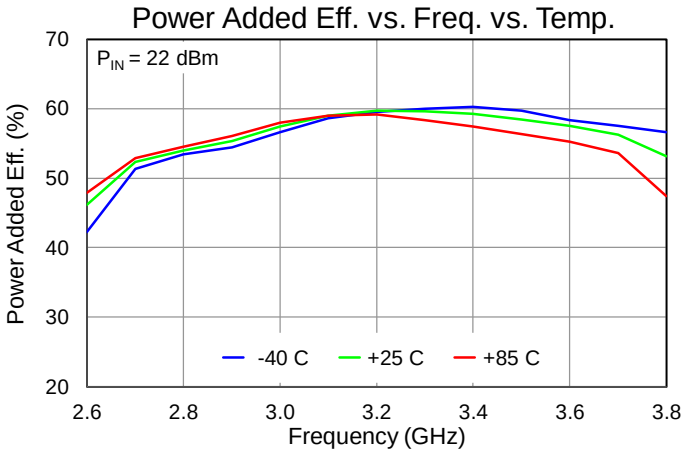

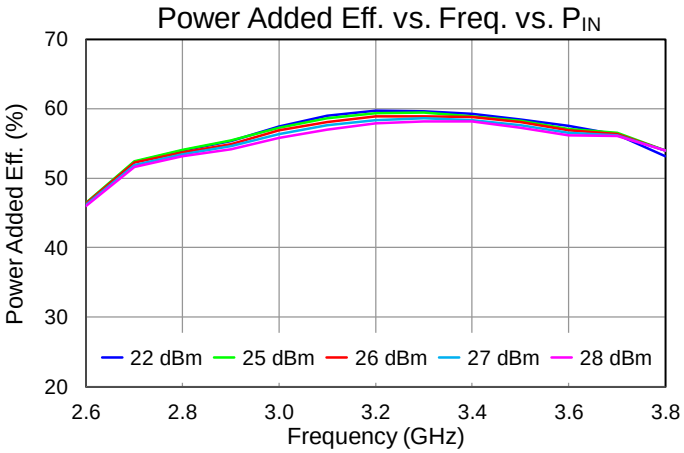

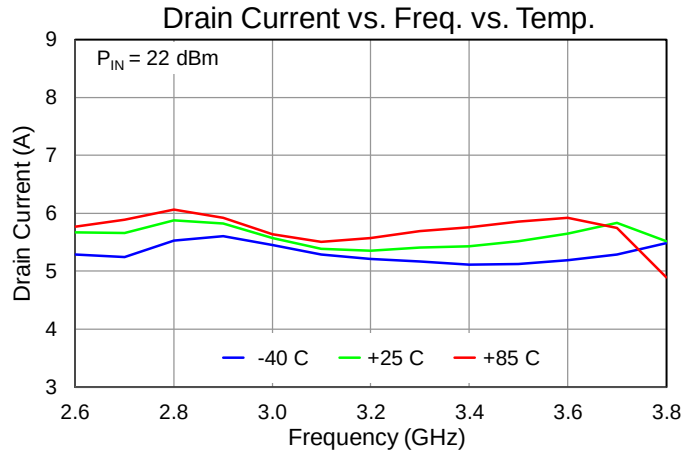

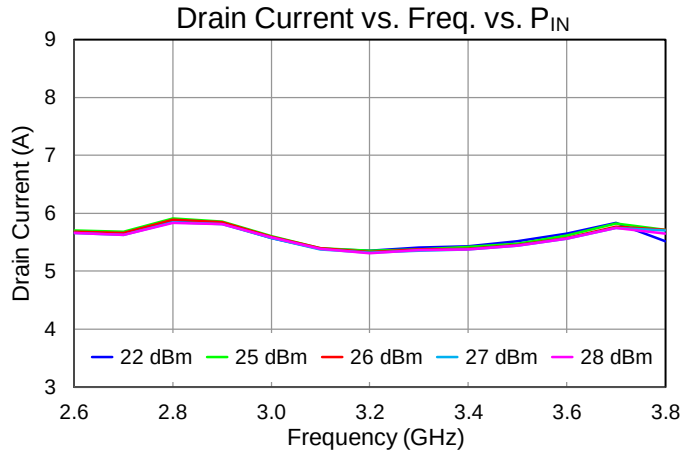

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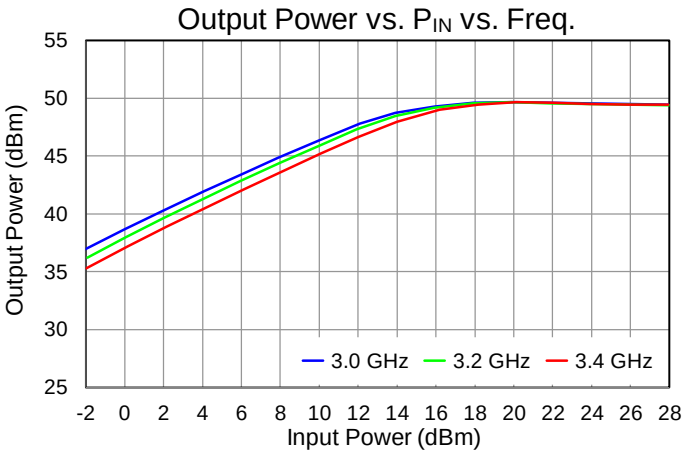

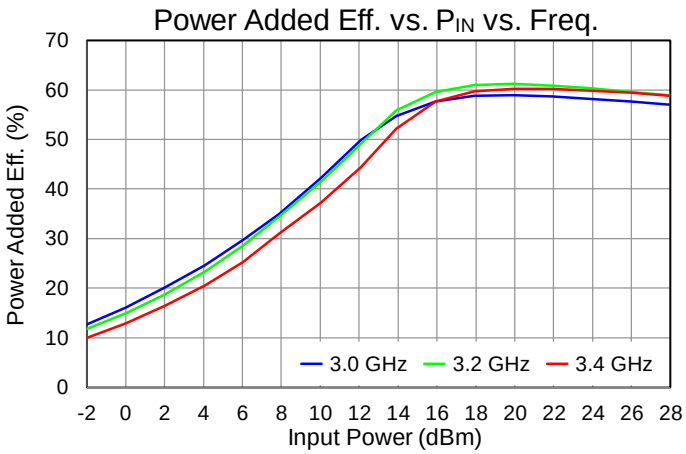

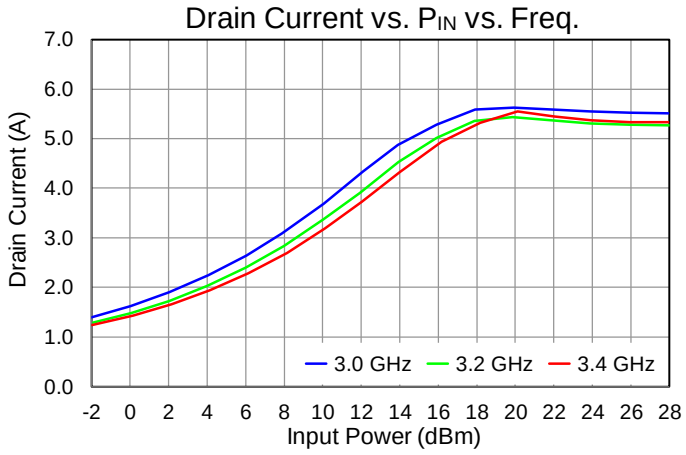

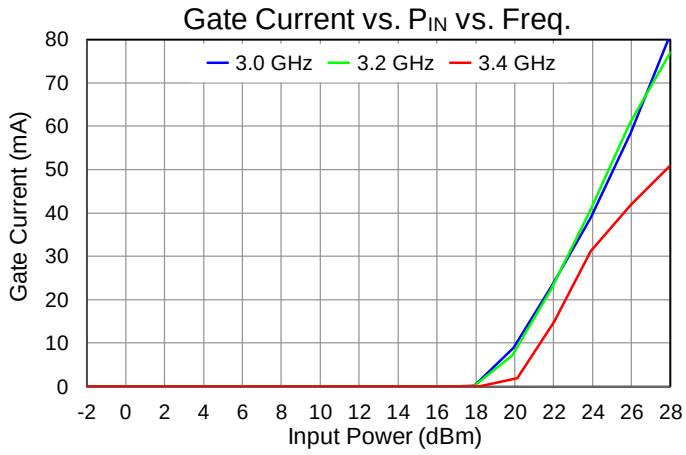

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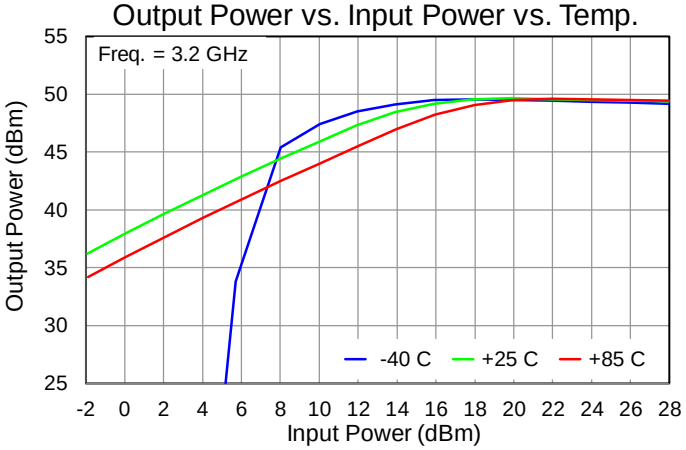
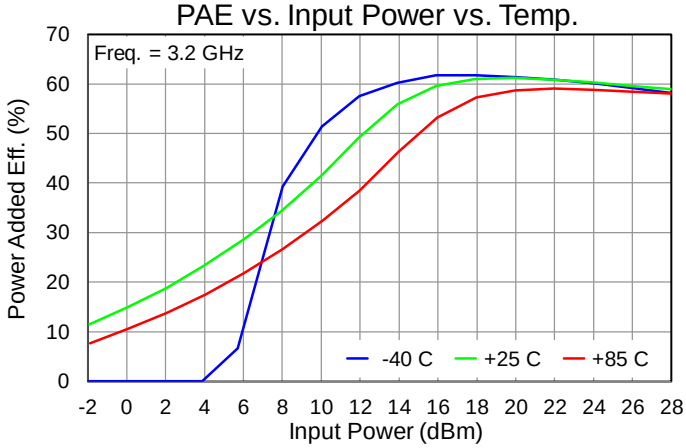
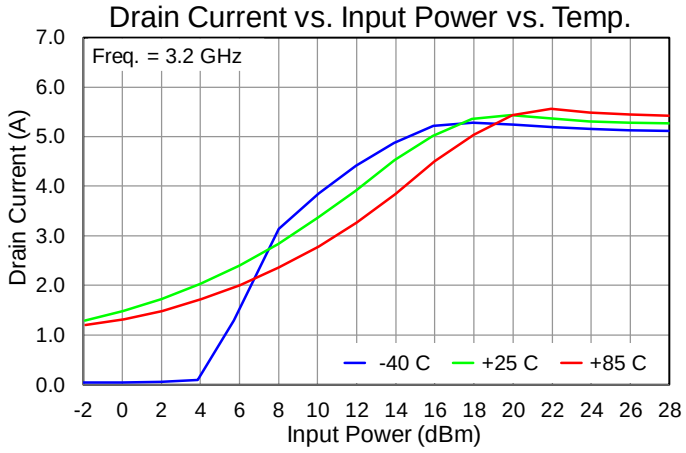
Output Power vs. Input Power vs. Temp.



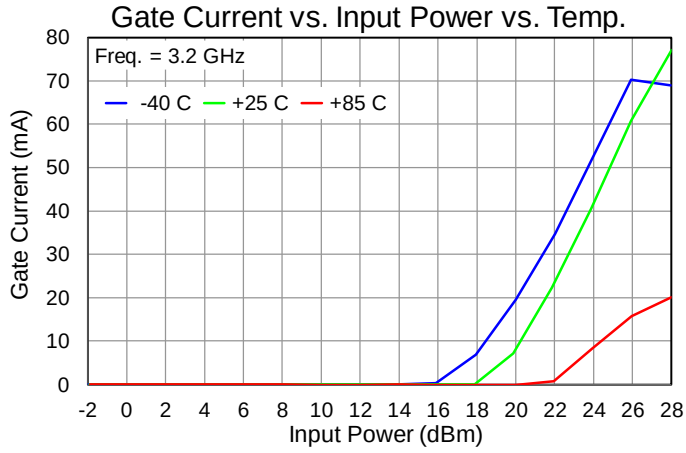
PAE vs. Input Power vs. Temp.



Drain Current vs. Input Power vs. Temp.



Gate Current vs. Input Power vs. Temp.



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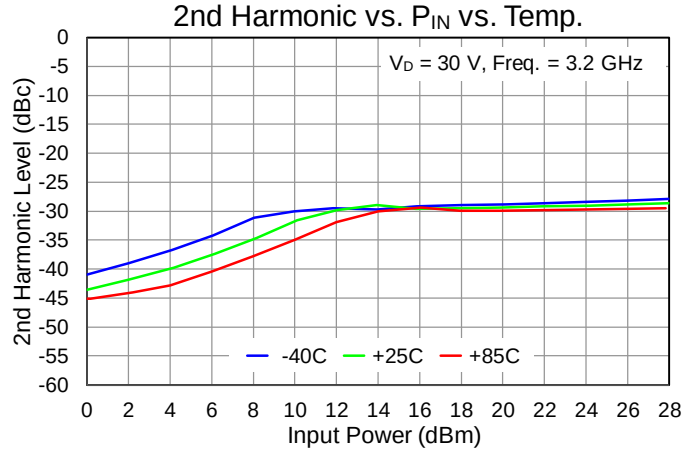

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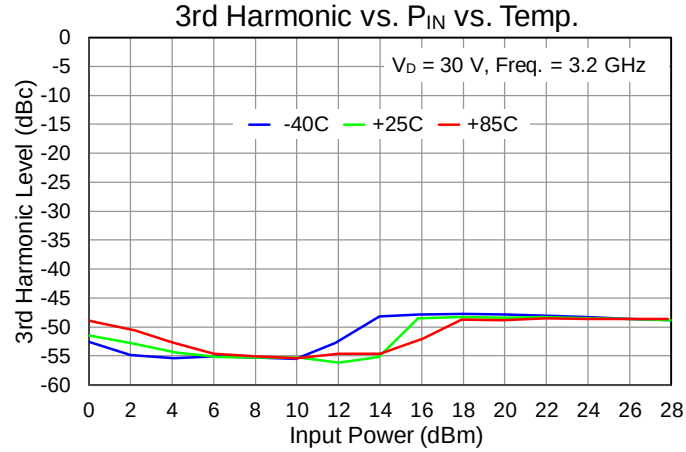

Performance Plots – Large Signal (I_{DQ}=300 mA, PW=100 us, DC=10%)

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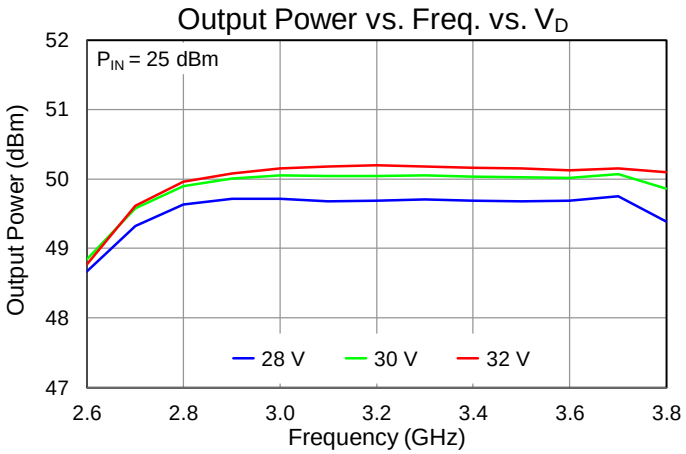

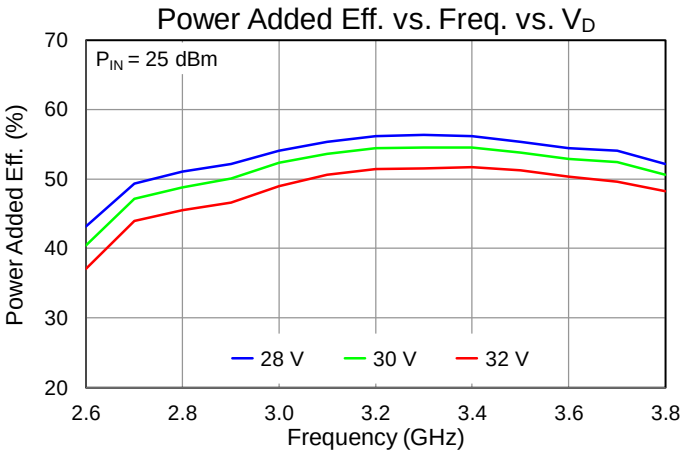

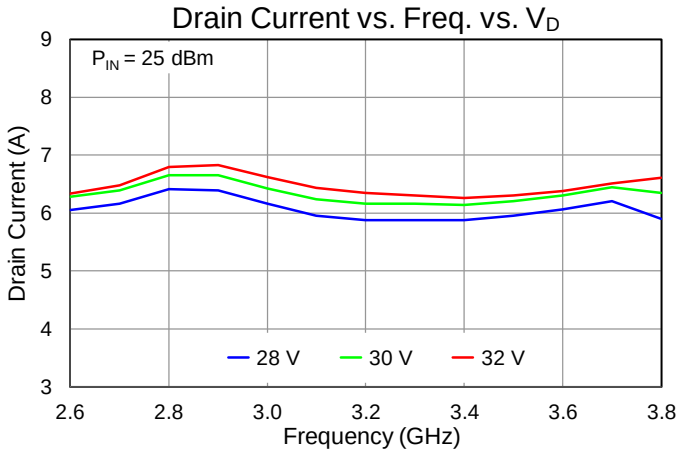

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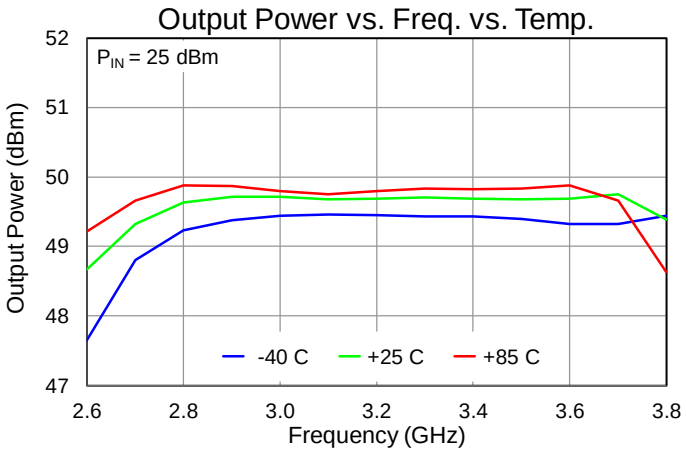
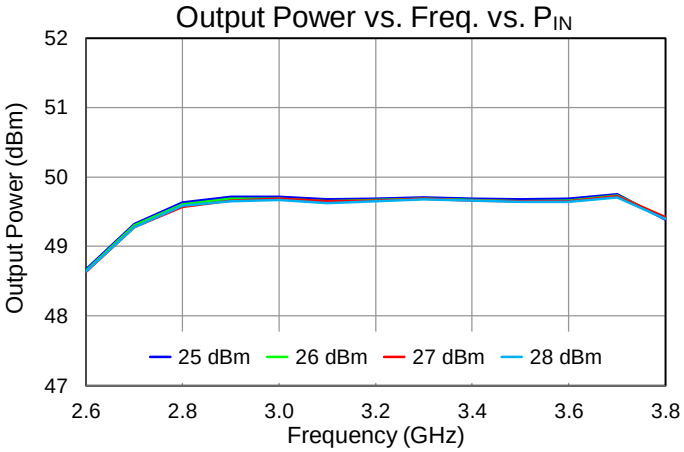
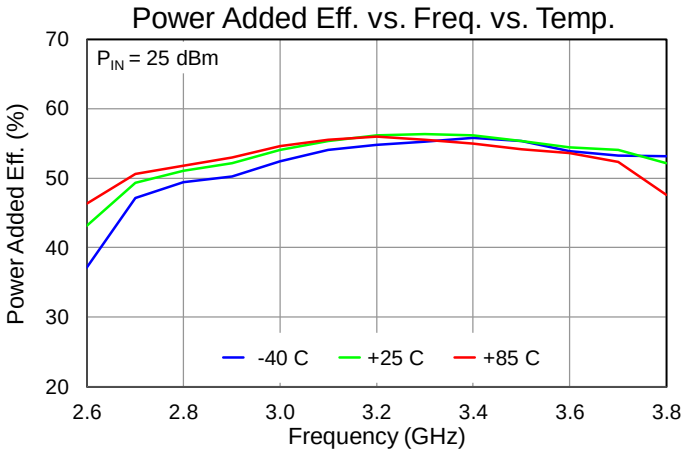
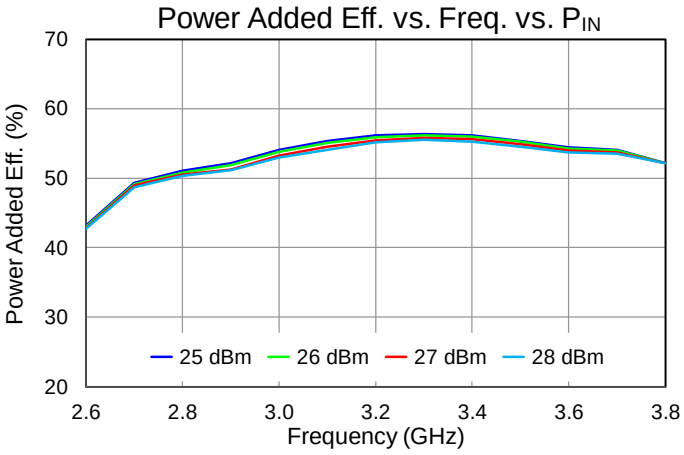
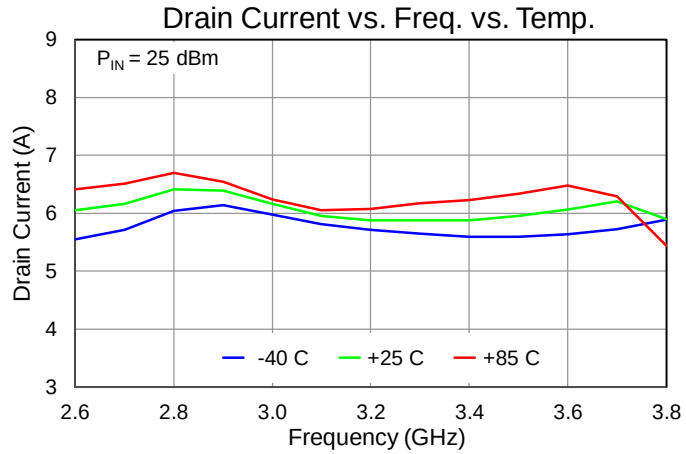
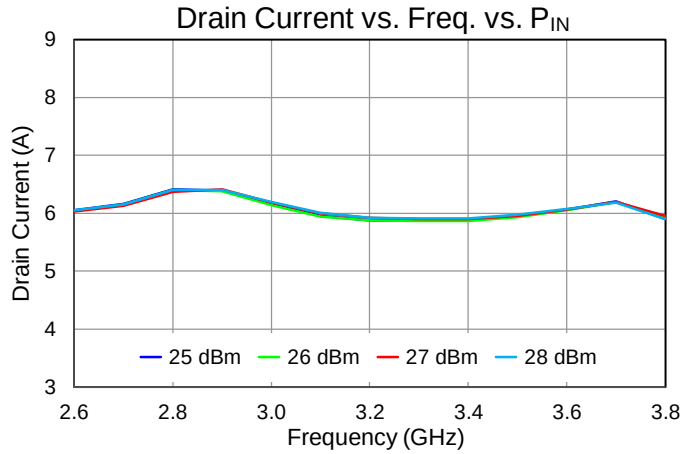






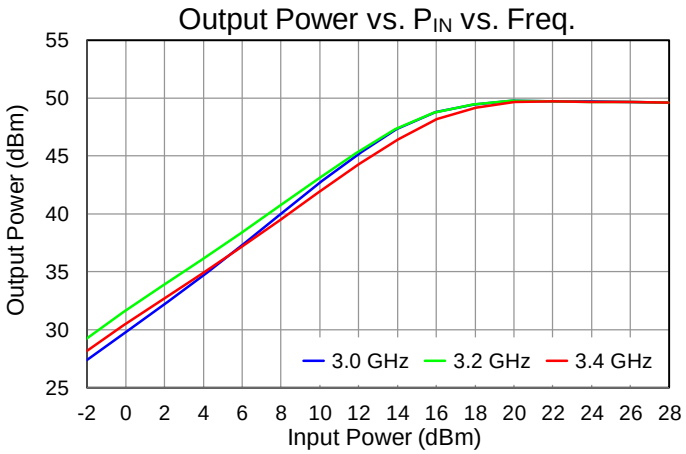


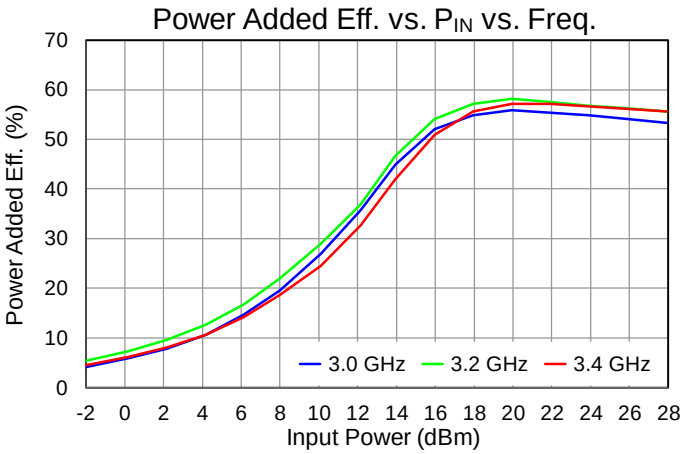


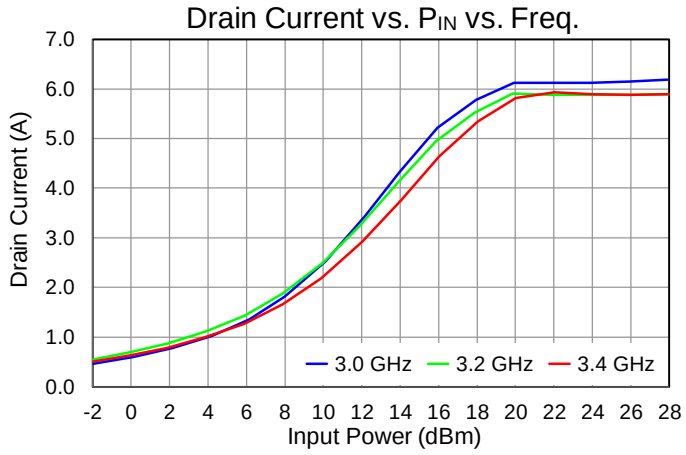


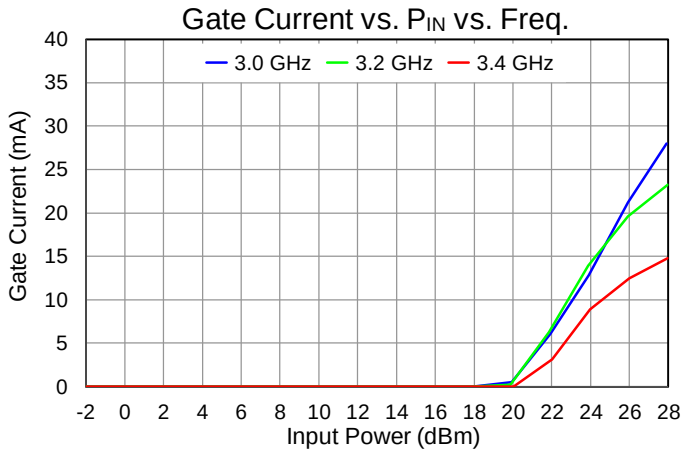
Performance Plots – Large Signal (I_{DQ}=300 mA, PW=100 us, DC=10%)

Test conditions unless otherwise noted: V_D = 28 V, I_{DQ} = 300 mA, T= +25 °C



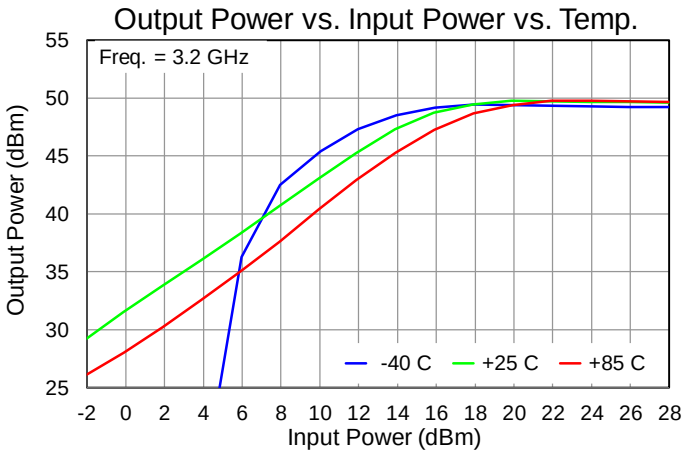


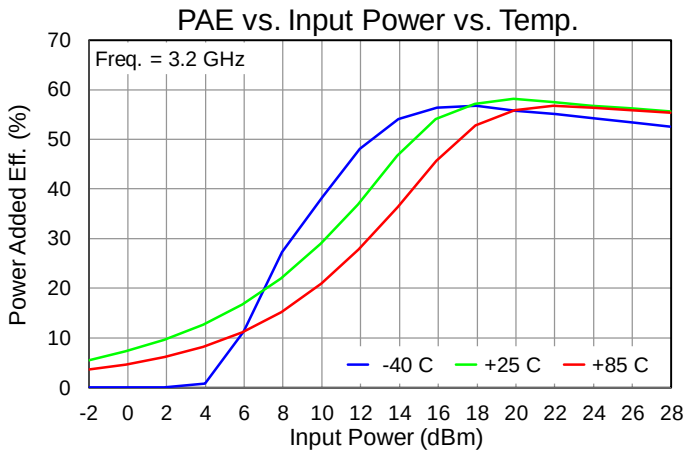


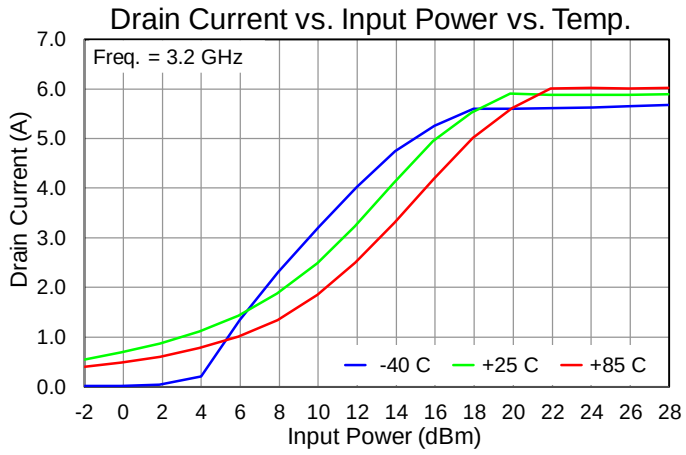


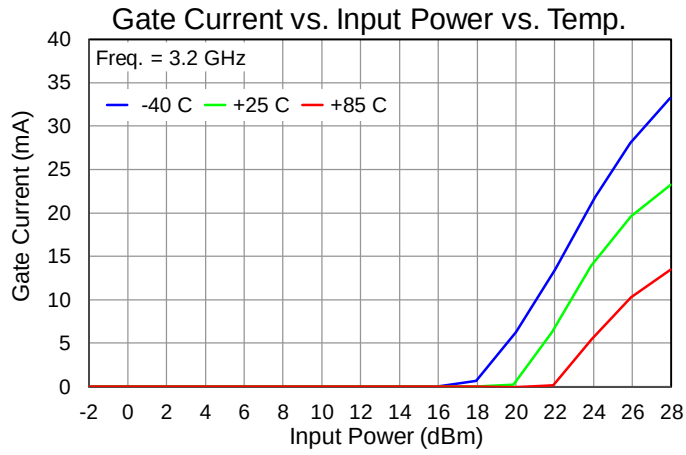
Performance Plots – Large Signal (I_{DQ}=300 mA, PW=100 us, DC=10%)

Test conditions unless otherwise noted: V_D = 28 V, I_{DQ} = 300 mA, T= +25 °C



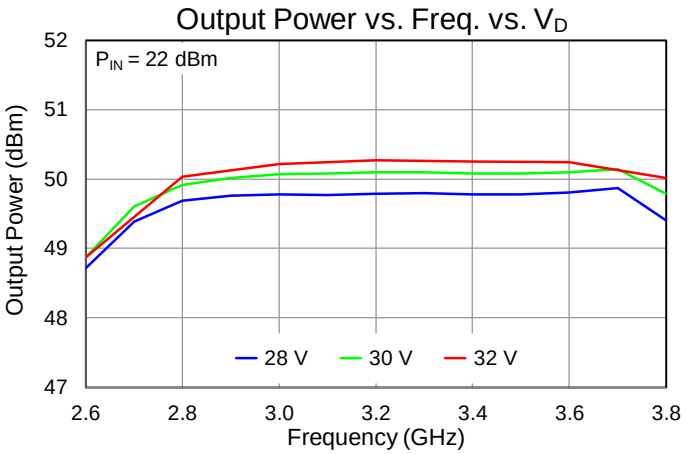


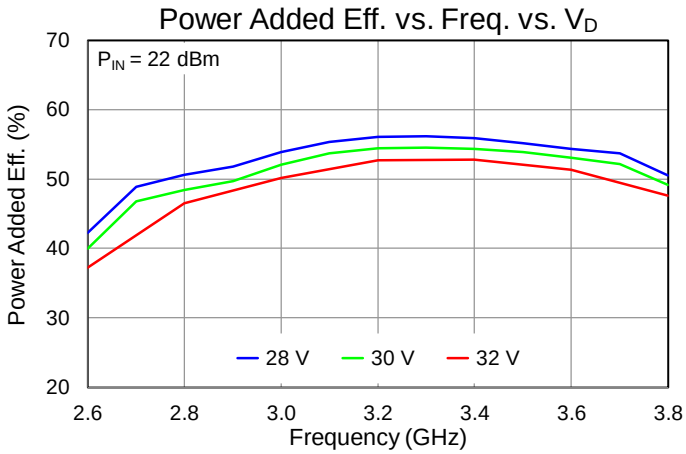


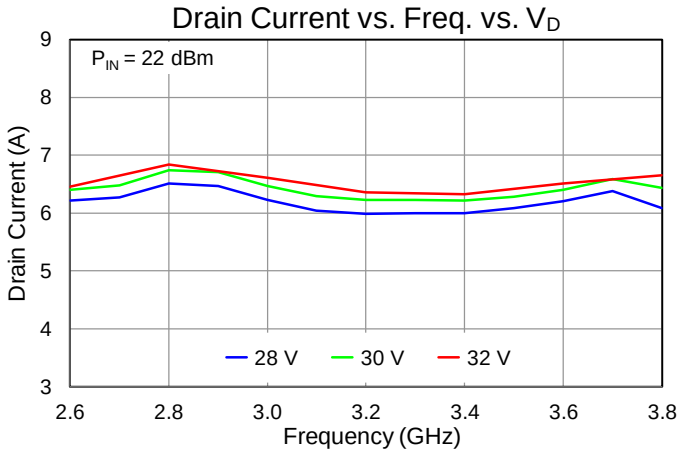


Performance Plots – Large Signal (I_{DQ}=1.5 A, PW=100 us, DC=10%)

Test conditions unless otherwise noted: V_D = 28 V, I_{DQ} = 1.5 A, T= +25 °C

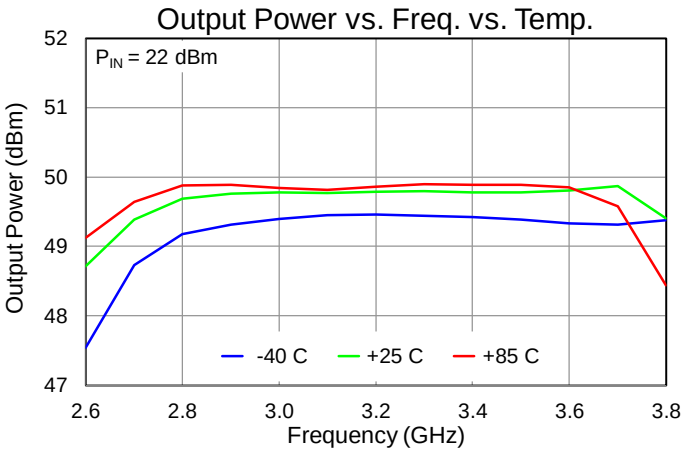


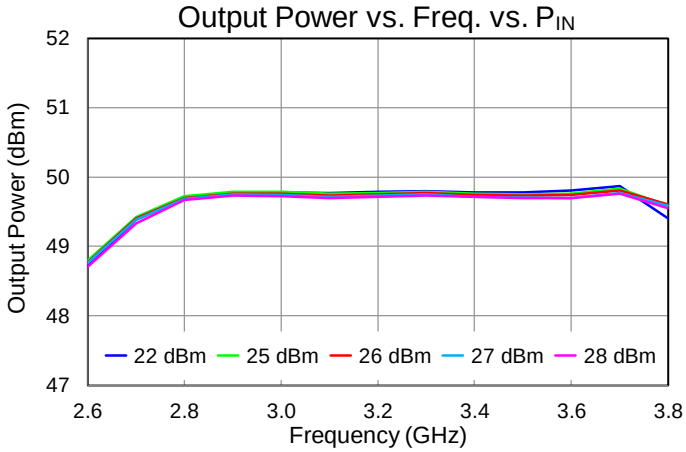


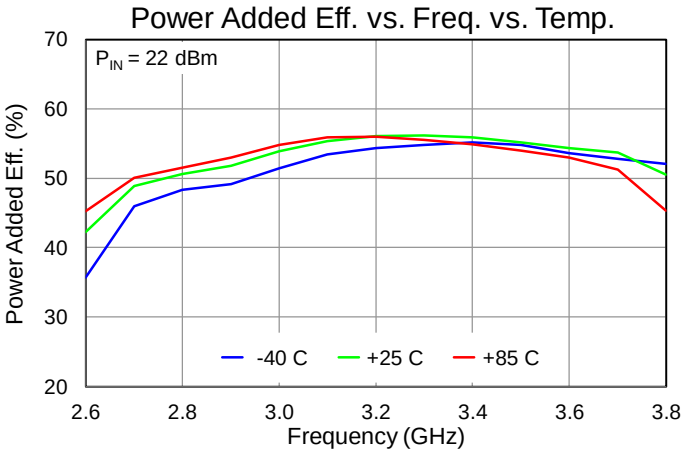


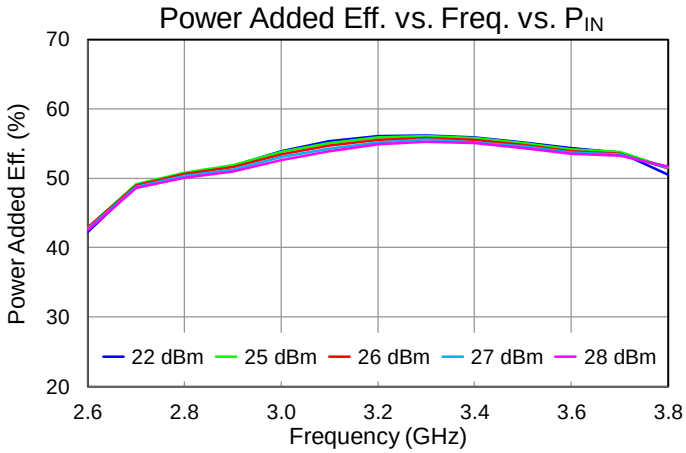
Performance Plots – Large Signal (I_{DQ}=1.5 A, PW=100 us, DC=10%)

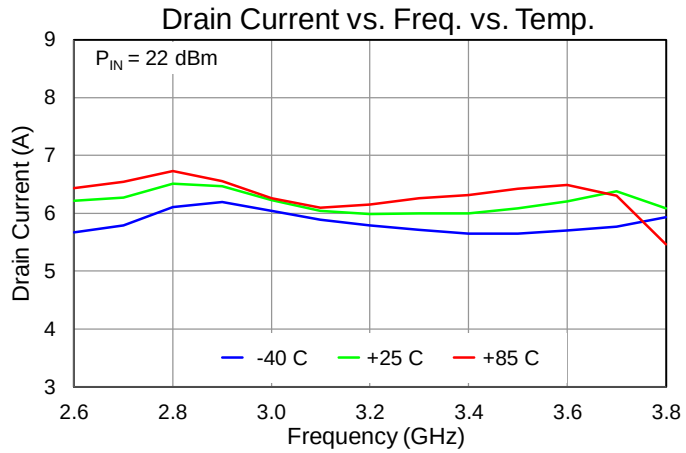
Test conditions unless otherwise noted: V_D = 28 V, I_{DQ} = 1.5 A, T= +25 °C

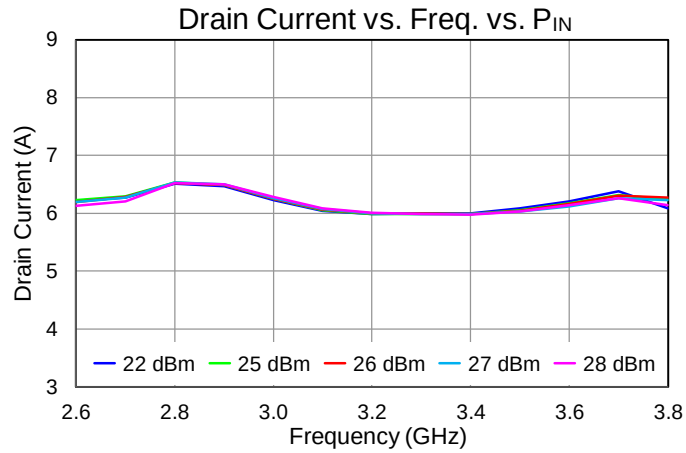






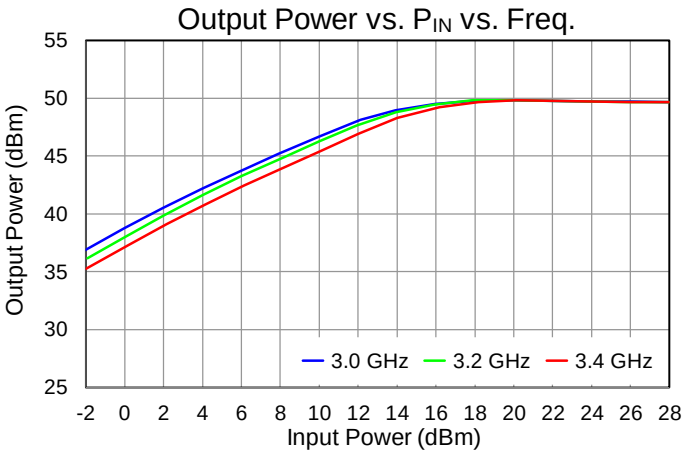


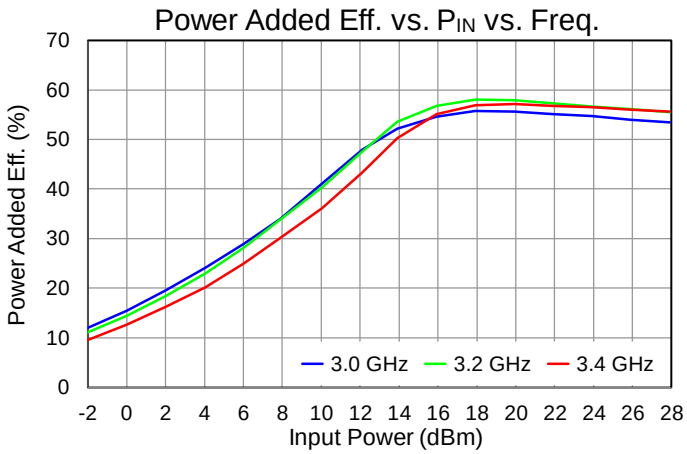


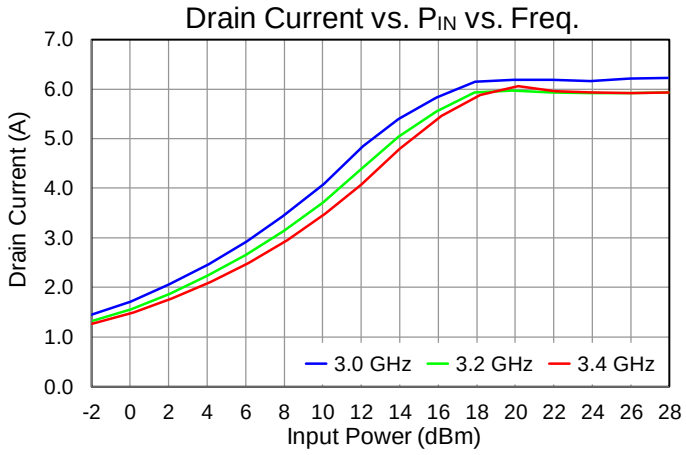


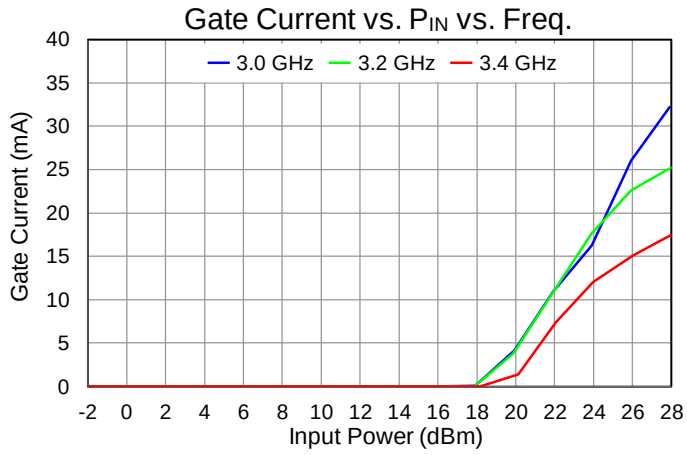
Performance Plots – Large Signal (I_{DQ}=1.5 A, PW=100 us, DC=10%)

Test conditions unless otherwise noted: V_D = 28 V, I_{DQ} = 1.5 A, T= +25 °C



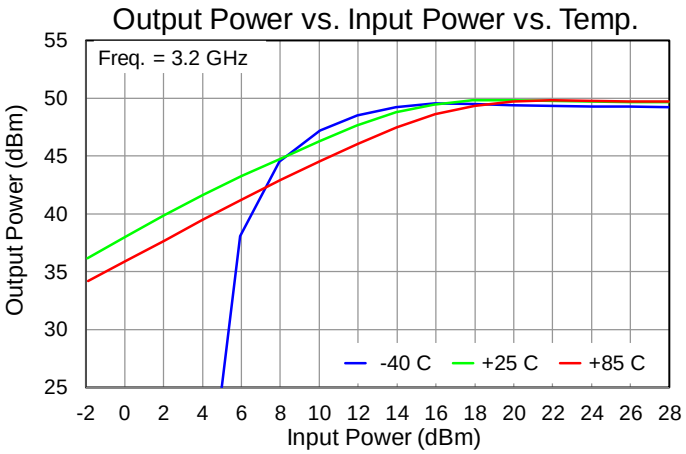


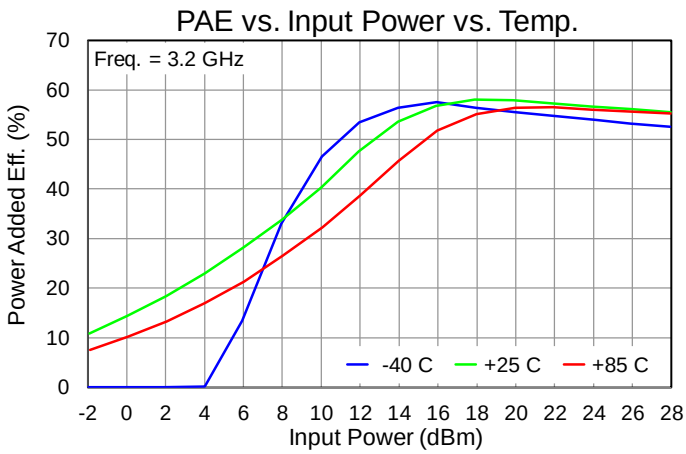


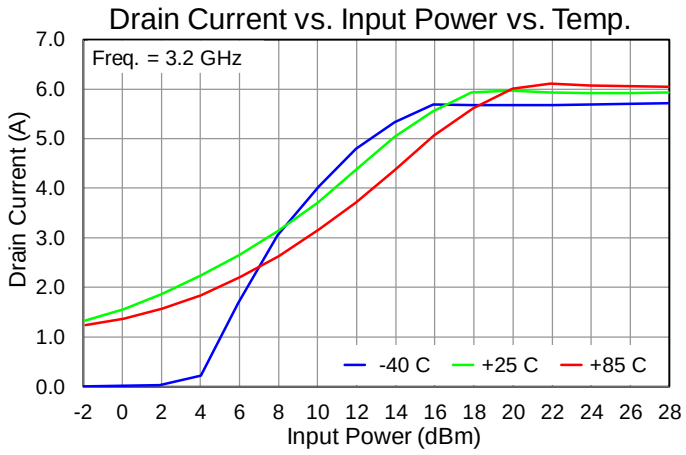


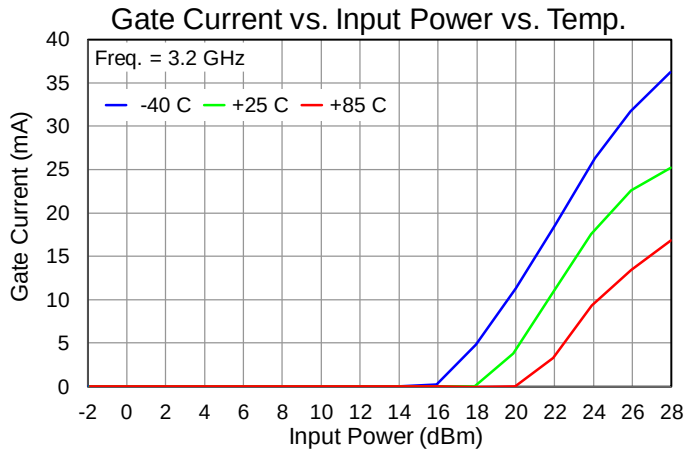
Performance Plots – Large Signal (I_{DQ}=1.5 A, PW=100 us, DC=10%)

Test conditions unless otherwise noted: V_D = 28 V, I_{DQ} = 1.5 A, T= +25 °C





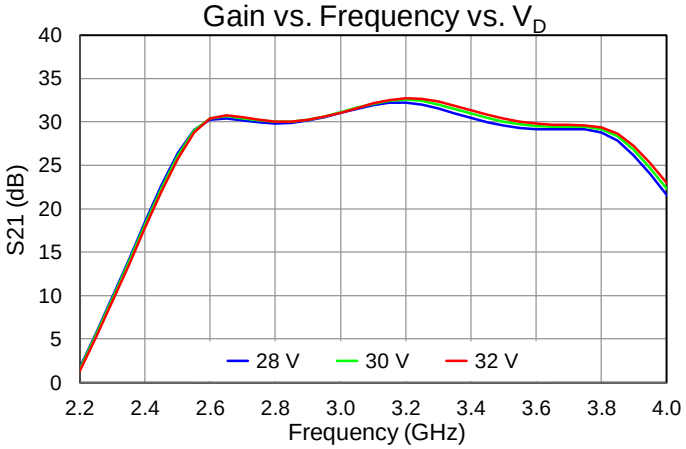




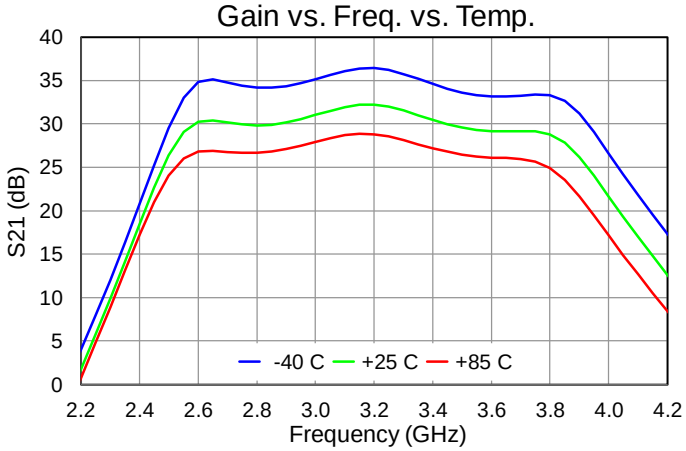
Performance Plots – Small Signal (CW)

Test conditions unless otherwise noted: V_D = 28 V, I_{DQ} = 300 mA, CW input power, T=+25 °C

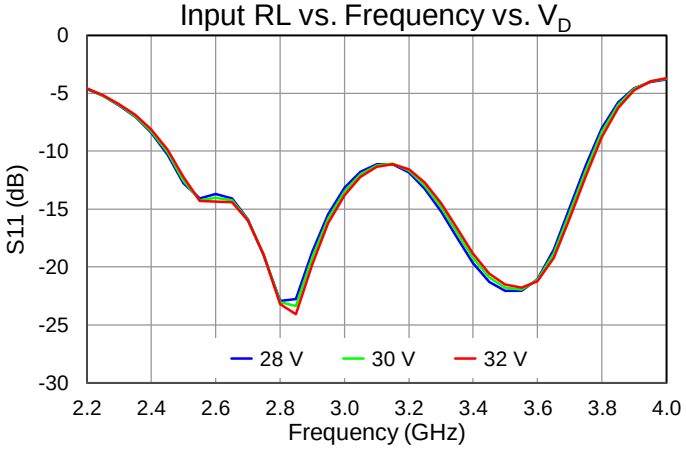
Gain vs. Frequency vs. V_D



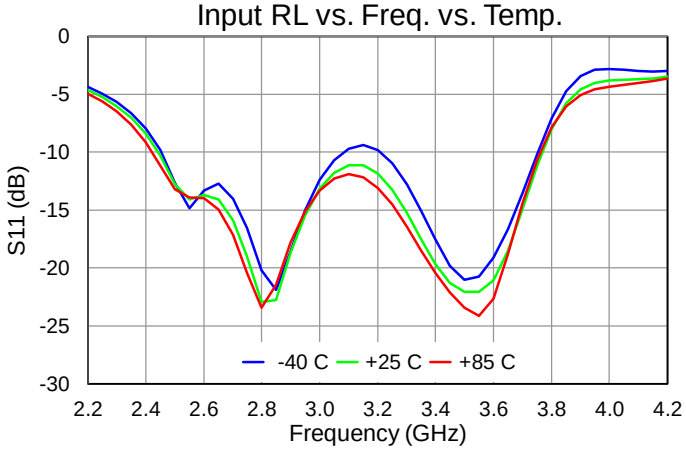
Gain vs. Freq. vs. Temp.



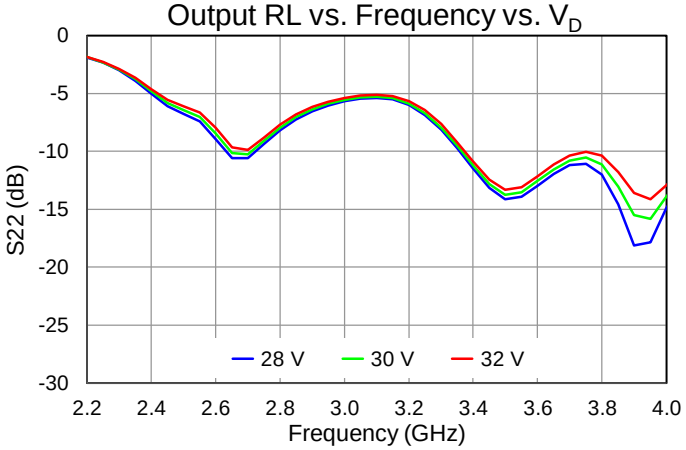
Input RL vs. Frequency vs. V_D



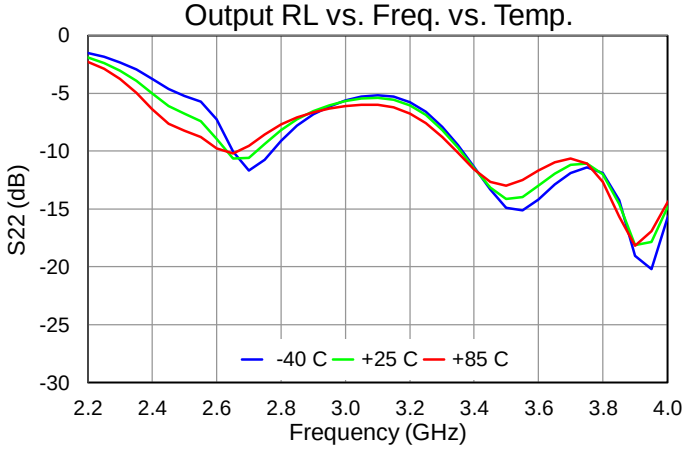
Input RL vs. Freq. vs. Temp.



Output RL vs. Frequency vs. V_D

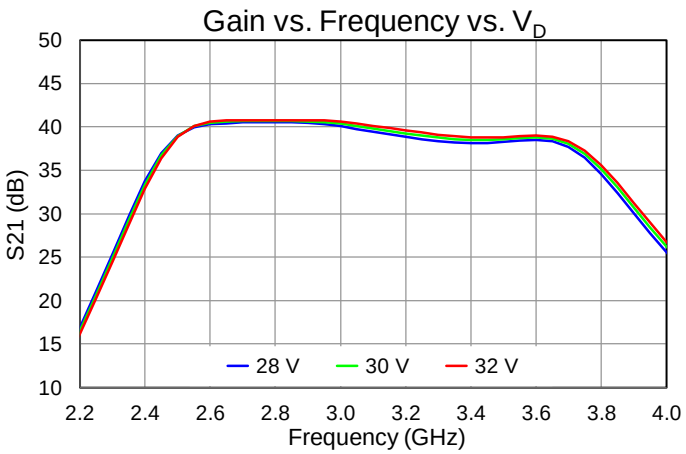


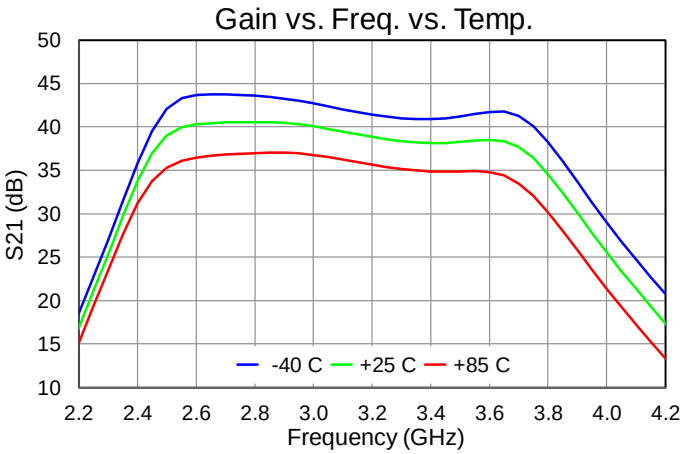
Output RL vs. Freq. vs. Temp.

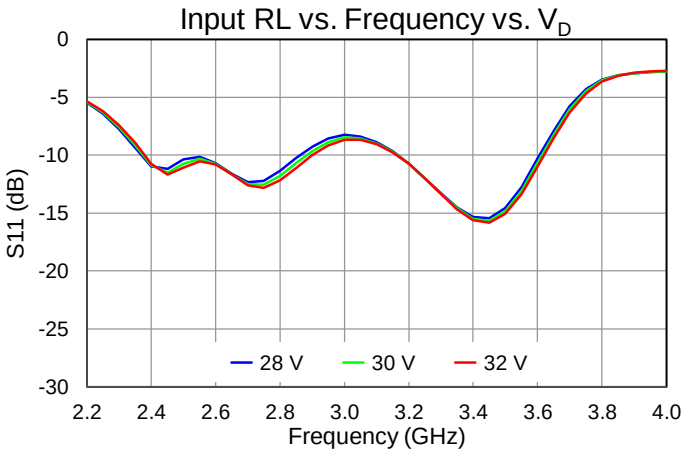


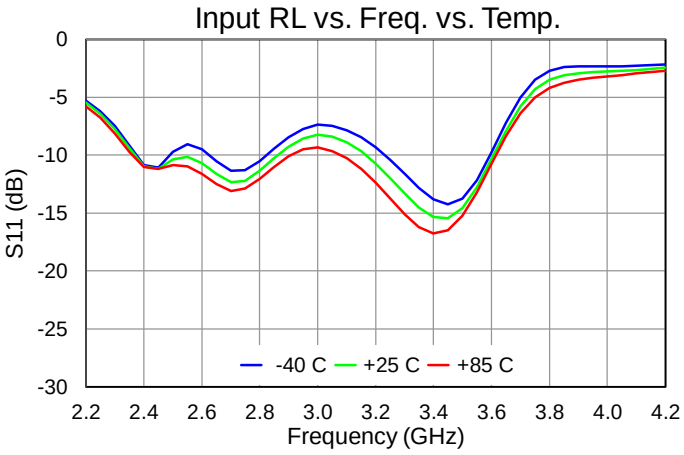
Performance Plots – Small Signal (CW)

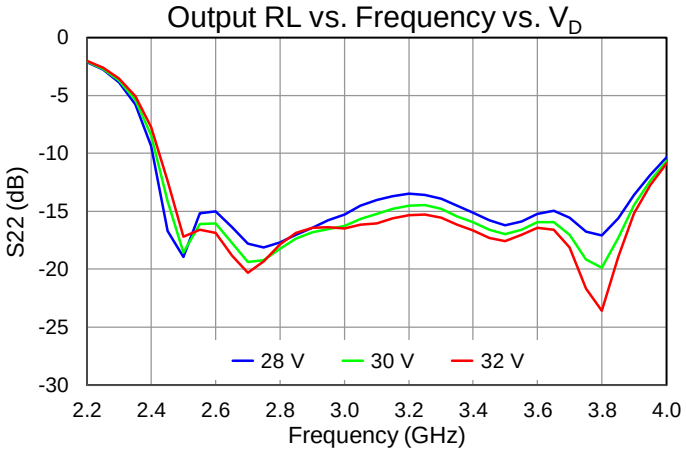
Test conditions unless otherwise noted: V_D = 28 V, I_{DQ} = 1.5 A, CW input power, T=+25 °C

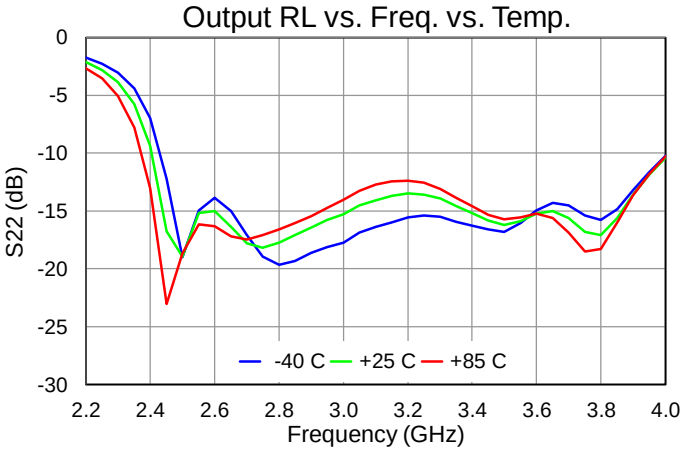










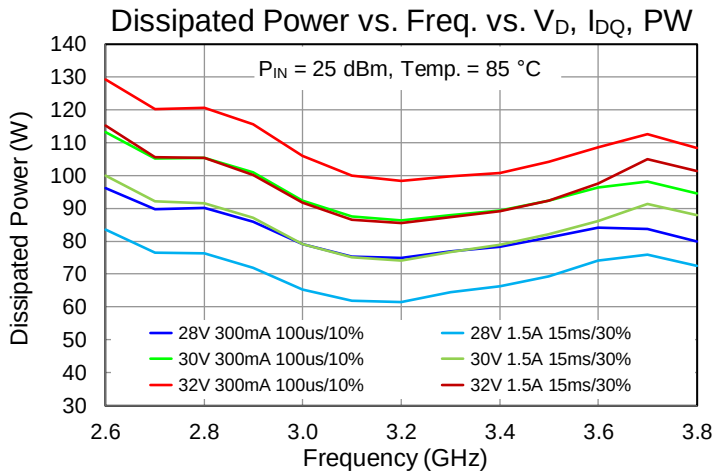


Thermal and Reliability Information

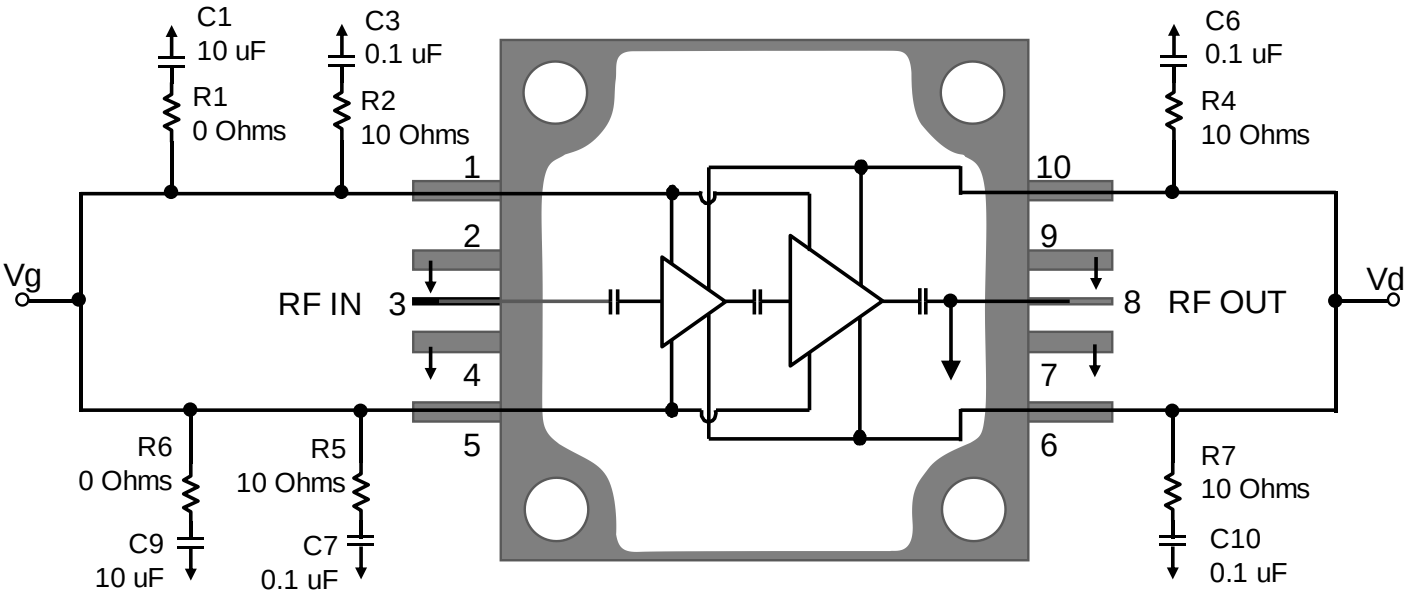
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85 °C, V_D = 30 V, I_{DQ} = 300 mA, Freq = 2.9 GHz, I_{D_Drive} = 6.9 A, P_{IN} = 25 dBm, P_{OUT} = 50.2 dBm, P_{DISS} = 101.0 W, PW = 100 us, DC = 10%	0.36	ºC/W
Channel Temperature, T_{CH} (Under RF) (2)		122	°C
Median Lifetime (T_M)		6.39E+09	Hrs
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85 °C, V_D = 30 V, I_{DQ} =1.5 A, Freq = 2.9 GHz, I_{D_Drive} = 6.3 A, P_{IN} = 25 dBm, P_{OUT} = 50.0 dBm, P_{DISS} = 90.1 W, PW = 15ms, DC = 30%	0.74	ºC/W
Channel Temperature, T_{CH} (Under RF) (2)		151	°C
Median Lifetime (T_M)		2.66E+09	Hrs
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85 °C, V_D = 32 V, I_{DQ} = 300 mA, Freq = 2.9 GHz, I_{D_Drive} = 7.2 A, P_{IN} = 25 dBm, P_{OUT} = 50.6 dBm, P_{DISS} = 115.6 W, PW = 100 us, DC = 10%	0.36	ºC/W
Channel Temperature, T_{CH} (Under RF) (2)		127	°C
Median Lifetime (T_M)		4.72E+07	Hrs
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85 °C, V_D = 32 V, I_{DQ} = 1.5 A, Freq = 2.9 GHz, I_{D_Drive} = 6.5 A, P_{IN} = 25 dBm, P_{OUT} = 50.4 dBm, P_{DISS} = 100.1 W, PW = 15 ms, DC = 30%	0.83	ºC/W
Channel Temperature, T_{CH} (Under RF) (2)		168	°C
Median Lifetime (T_M)		4.55E+06	Hrs

Notes:
1. Thermal resistance determined to the back of package (85 °C)
2. Channel temperature indicated is an IR scan equivalent temperature. Thermal resistance is calculated using this value. Additional information can be found in the Qorvo Applications Note “GaN Device TCHMAX Theta-JC and Reliability Estimates,” located here https://www.qorvo.com/products/d/da006480

Dissipated Power



Applications Information



Notes:
1. V_G & V_D need to be biased from both sides.

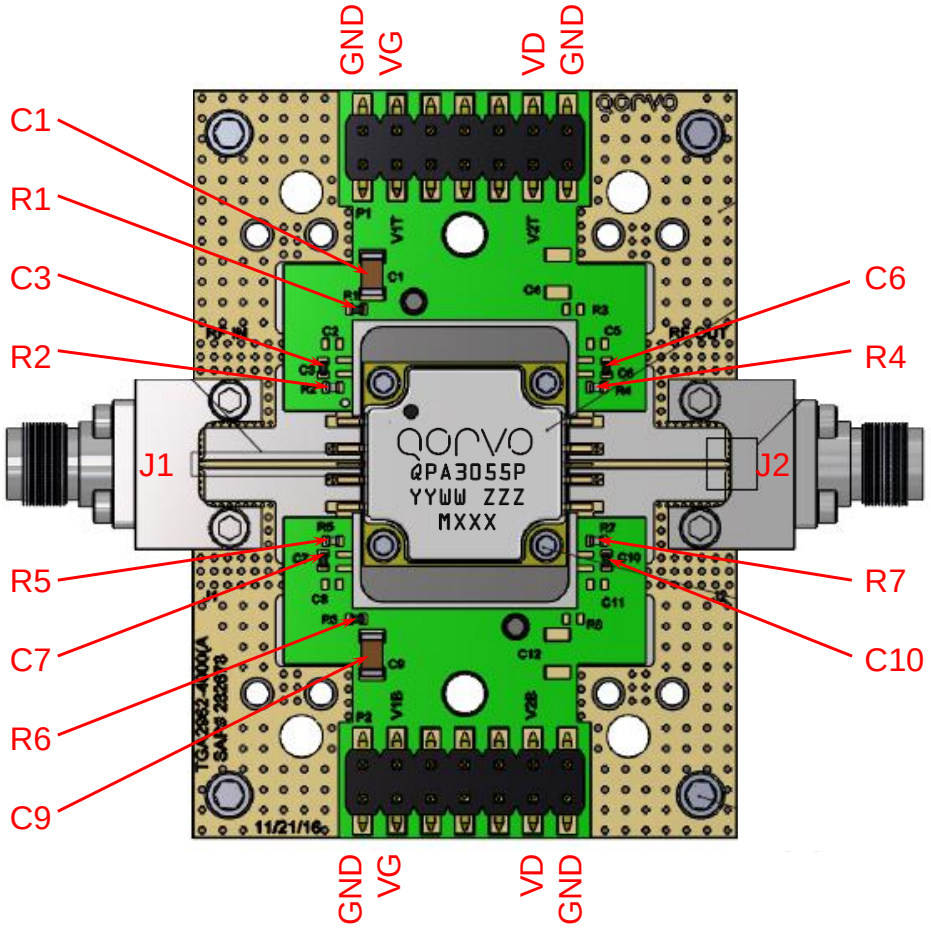
Bias-Up Procedure

1. Set I_D limit (CW) to 7000 mA, I_G limit to 60 mA
2. Set V_G to −5.0 V
3. Set V_D +30 V
4. Adjust V_G more positive until I_{DQ} ≈ 300 mA, peak (V_G ~ −2.5 V, typical)
5. Apply RF signal

Bias-Down Procedure

1. Turn off RF signal
2. Reduce V_G to −5.0 V. Ensure I_{DQ} ~ 0mA
4. Set V_D to 0 V
5. Turn off V_D supply
6. Turn off V_G supply

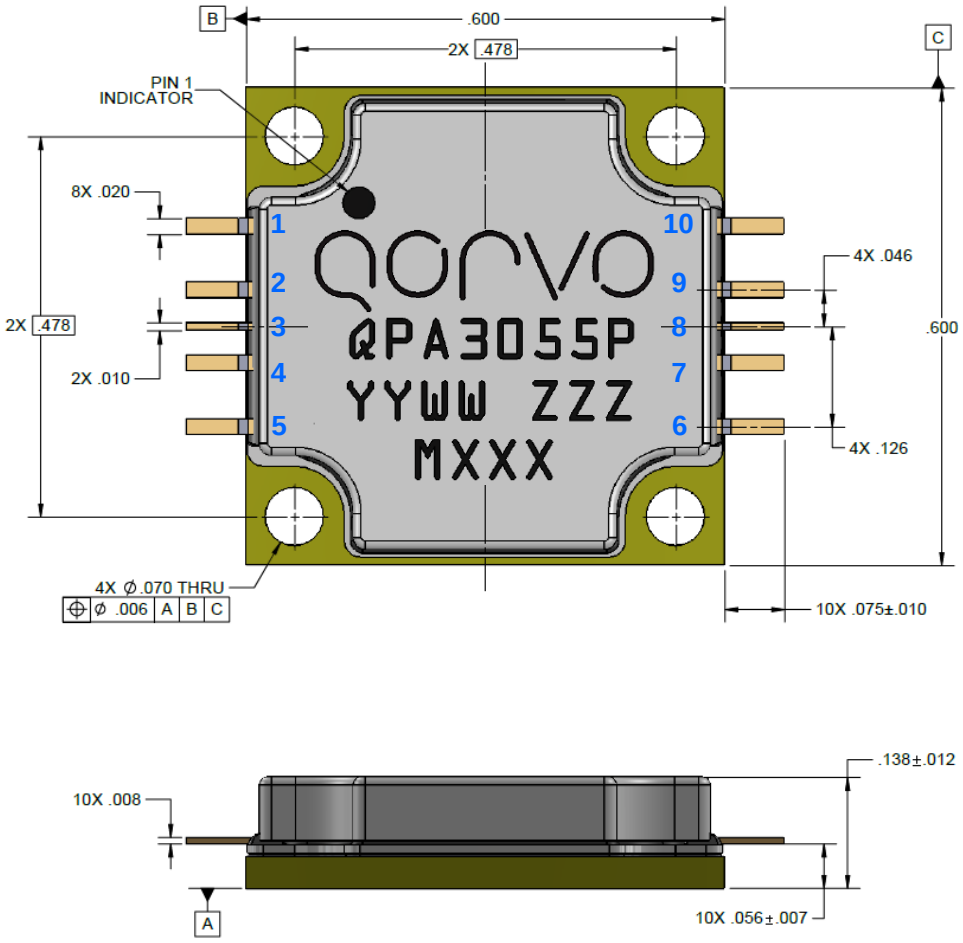
Evaluation Board (EVB) Layout Assembly



Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C1, C9	10 uF	CAP, CER, 10 uF, 50 V, 20%, X5R, 1206	Various	
C3, C6, C7, C10	0.1 uF	CAP, 0.1 uF, 10%, 50 V, X7R, 0402	Various	
R2, R4, R5, R7	10 Ohm	RESISTOR, 10 OHM, 5%, 0.1 W, 0402	Various	
R1, R6	0 Ohm	RES, 0 OHM, JMPR, 0402	Various	
J1, J2	2.92 mm	Female End Launch Connector	Southwest Microwave	1092-02A-5
PCB	-----	Rogers 6035HTC, 10 mil dielectric, 0.5 oz. copper (gold plated)	Rogers Corp.	

Mechanical Information and Bond Pad Description



NOTES:

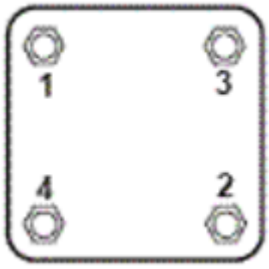
1. **MATERIALS**
   - **PACKAGE BASE: COPPER**
   - **LEADS: ALLOY 194**
   - **LID: PLASTIC**
   - **FINISH: GOLD**
2. **PART IS EPOXY SEALED**
3. **UNITS: INCHES**
4. **TOLERANCES (UNLESS NOTED):**
   - **.XX = ± .01**
   - **.XXX = ± .005**
5. **MARKINGS**
   - **PART NUMBER: QPA3055P**
   - **WORK YEAR: YY**
   - **WORK WEEK: WW**
   - **SERIAL NUMBER: ZZZ**
   - **BATCH ID: MXXX**

Bond Pad Description

Pad No.	Symbol	Description
1, 5	V_G	Gate voltage. Bias network is required; see Application Circuit on page 21 as an example. Gate must be biased from both sides.
2, 4, 7, 9	Ground	Must be grounded to PCB
3	RF Input	RF Input; matched to 50 Ω, DC blocked
6, 10	V_D	Drain voltage. Bias network is required; see Application Circuit on page 21 as an example.
8	RF Output	RF Output; matched to 50 Ω, DC blocked, DC grounded

Assembly Notes

1. Carefully clean the PC board and package leads with alcohol. Allow it to dry fully.
2. To improve the thermal and RF performance, Qorvo recommends attaching a heat sink to the bottom of the PCB and apply thermal compound (Arctic Silver 5 recommended) or 4 mil indium shim between the heat sink and the package.
3. (The following is for *information only*. There are many variables in a second level assembly that Qorvo does not control, so Qorvo does not recommend an absolute torque value.) Use screws to attach the component to the heat sink. A suggested torque value is 16 in-oz. for a 0-80 screw. Start with screws finger tight, then torque to 8 in-oz., then torque to final value. Use the following tightening pattern:



4. The component leads should be manually soldered. Apply a low residue solder alloy meeting J-STD-001 (ROL0, ROL1 or equivalent) with a liquidus temperature below 220 °C to each pin of the QPA3055P. The use of low residue/no-clean flux (ROL0, ROL1) is recommended. Adding flux during hand soldering of the component leads with localized spot cleaning is acceptable. Soldering irons meeting the requirements of J-STD-001, Appendix A are acceptable. The packaged part should not be subjected to conventional SMT automated solder reflow processes.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B	ANSI/ESDA/JEDEC JS-001
MSL Rating	NA	

Caution!
ESD-Sensitive Device

Solderability

The component leads should be manually soldered, and the package cannot be subjected to conventional reflow processes. The use of no-clean solder to avoid washing after soldering is recommended.

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_40_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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