Preliminary

QPA2226D

34 – 36 GHz 20 Watt GaN Power Amplifier

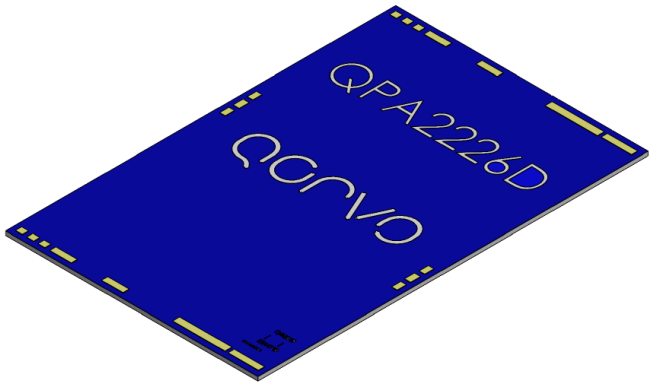
Product Overview

Qorvo's QPA2226D is a high power MMIC amplifier fabricated on Qorvo's production 0.15 um GaN on SiC process (QGaN15). Operating between 34 – 36 GHz, it provides 20 W of saturated output power with 15 dB of large signal gain.

To simplify system integration, the QPA2226D is fully matched to 50 ohms with integrated DC blocking caps on both I/O ports. Its RF ports are DC coupled to ground for optimum ESD performance.

The QPA2226D is 100% DC and RF tested on-wafer to ensure compliance to electrical specifications.

Lead-free and RoHS compliant

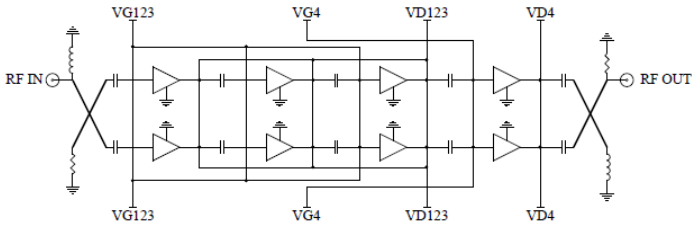


Key Features

- Frequency Range: 34 – 36 GHz
- P_{SAT} (P_{IN} = 28 dBm): 43 dBm
- PAE (P_{IN} = 28 dBm): 12 %
- Power Gain (P_{IN} = 28 dBm): 15 dB
- Small Signal Gain: > 7 dB
- Bias: pulsed, V_D = +28 V, I_{DQ} = 100 mA, V_G = -2.5 V typ.
- Die Dimensions: 3.29 x 5.09 x 0.05 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Applications

- Radar
- Satellite Communications

Ordering Information

Part No.	Description
QPA2226D	34 – 36 GHz 20 Watt GaN Amplifier
QPA2226DEVB	Evaluation Board for QPA2226D

Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage (V_D)	29.5 V
Gate Voltage Range (V_G)	-6 V to 0 V
Drain Current (I_{D123}), top + bottom	4.02 A
Drain Current (I_{D4})	2.88 A
Gate Current (I_G)	See plot page 17
Power Dissipation (P_{DISS}), 85 °C	Pulsed, 130 W CW, 95 W
Input Power (P_{IN}), Pulsed RF, 50 Ω, V_D = 28 V, I_{DQ} = 50 mA, DC = 50%, PW = 50 us, T_{BASE} = 125 °C	35 dBm*
Input Power (P_{IN}), Pulsed RF, 3:1 VSWR, V_D = 28 V, I_{DQ} = 50 mA, DC = 50%, PW = 50 us, T_{BASE} = 125 °C	30 dBm*
Mounting Temperature (30 seconds)	320 ºC
Storage Temperature	-55 to +150 ºC

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

* Robustness guaranteed over 34 - 36 GHz. Out of band operation not recommended

Recommended Operating Conditions

Parameter	Min	Typ.	Max	Units
Pulsed RF (or V_D)	DC = 50%, PW = 50 us			
Drain Voltage (V_D)		+28		V
Drain Current, Quiescent (I_{DQ})		100	300	mA
Drain Current, RF (I_{D_Drive})	See plot page 14			mA
Gate Voltage Typ. Range (V_G)	−2 to -2.9			V
Gate Current, RF (I_{G_Drive})	See plot page 14			mA
Input Power @ Saturation, (P_{IN})	-40 °C: 21			dBm
	+25 °C: 23			
	+85 °C: 28			
Operating Temp. Range (T_{BASE})	−40		+85	ºC

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

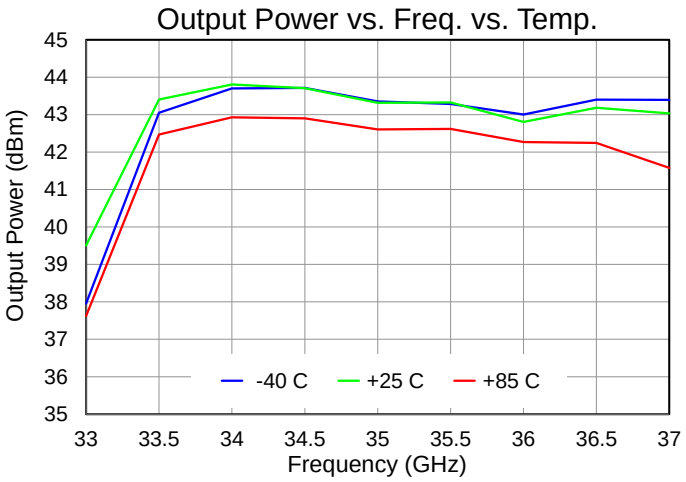
Parameter	Conditions (1) (2)	Min	Typ.	Max	Units
Operational Frequency Range		34		36	GHz
Output Power at Saturation, P_{SAT}	P_{IN} = +28 dBm, Pulsed		43		dBm
Power Added Efficiency, PAE	P_{IN} = +28 dBm, Pulsed		> 15		%
Large Signal Gain	P_{IN} = +28 dBm, Pulsed		12		dB
Small Signal Gain, S21	CW		> 7		dB
Input Return Loss, IRL	CW		10		dB
Output Return Loss, ORL	CW		10		dB
P_{SAT} Temperature Coefficient	T_{DIFF} = −40 ºC to +85 ºC; P_{IN} = +28 dBm, Pulsed		-0.01		dBm/ºC
S21 Temperature Coefficient	T_{DIFF} = −40 ºC to +85 ºC, CW		-0.17		dB/ºC

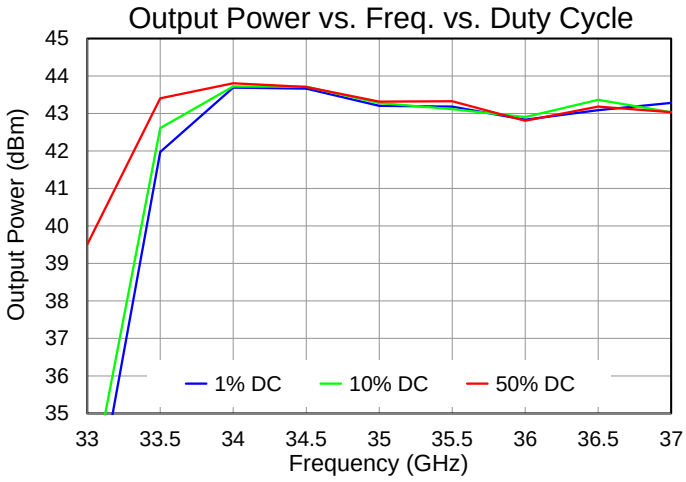
Notes:

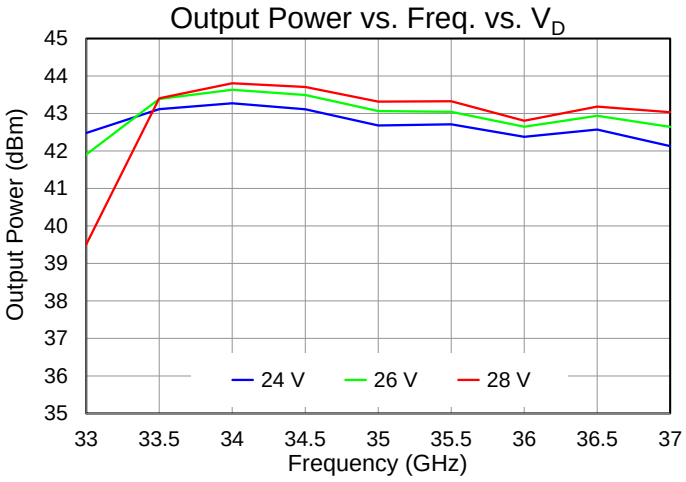
1. Test conditions unless otherwise noted: Pulsed RF, V_D = +28 V, I_{DQ} = 100 mA, V_G = -2.5V +/- typical, DC = 50%, PW = 50 us, T_{BASE} = +25 ºC, Z_0 = 50 Ω
2. T_{BASE} is back side of 20 mil CuMo carrier plate with AuSn solder

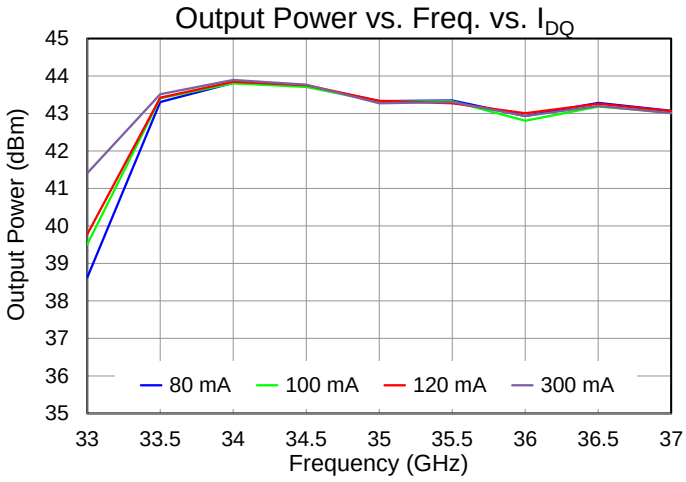
Performance Plots – Large Signal

Test conditions, unless otherwise noted: **Pulsed RF**, V_D = 28 V, I_{DQ} = 100 mA, Duty Cycle = 50%, PW = 50 us, P_{IN} = 28 dBm, T_{BASE} = +25 ºC









Performance Plots – Large Signal

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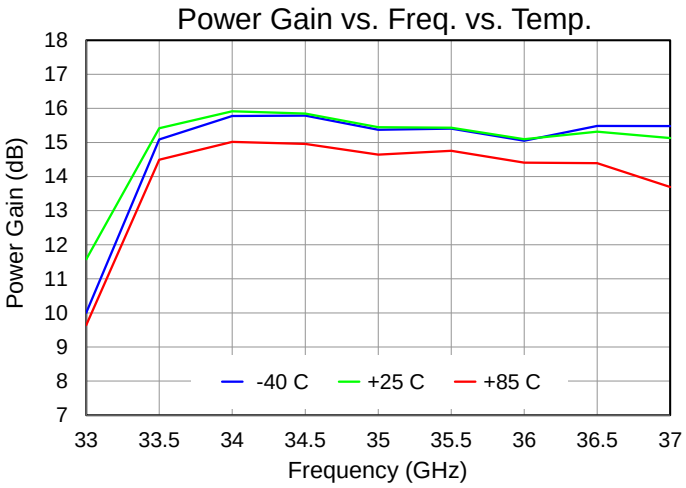
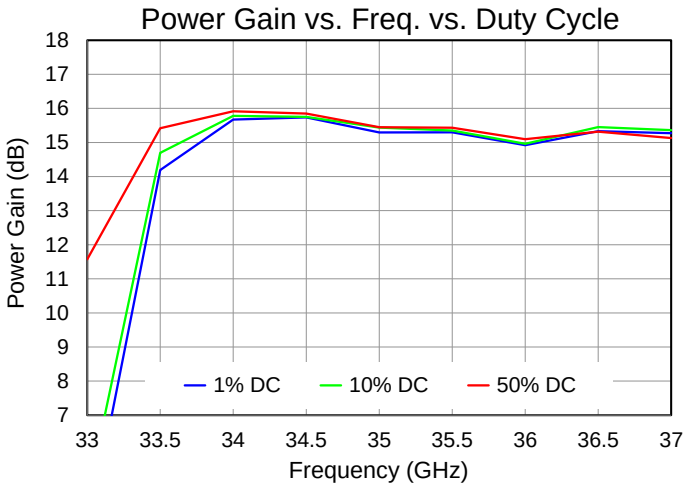
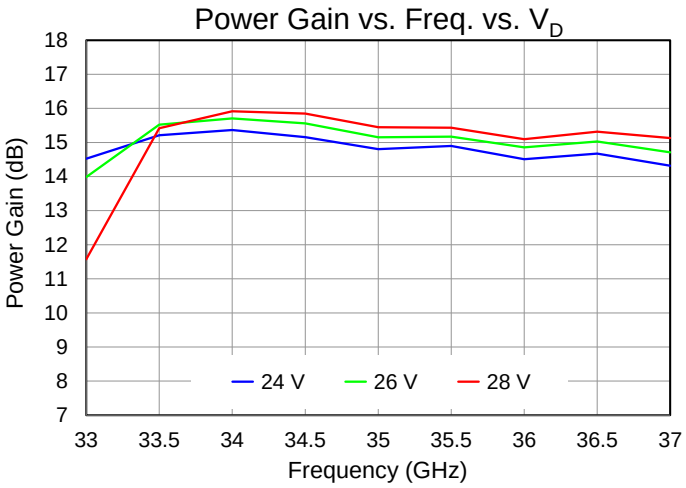
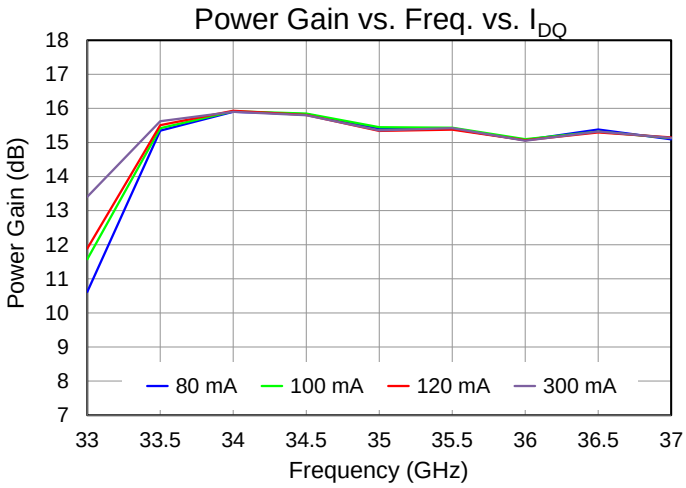


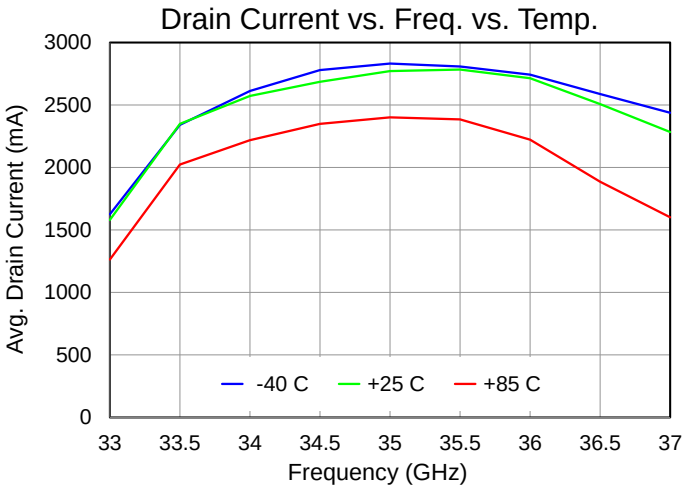


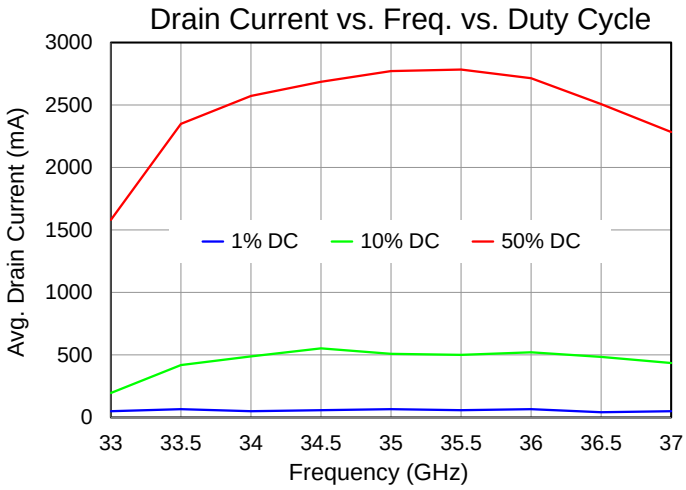


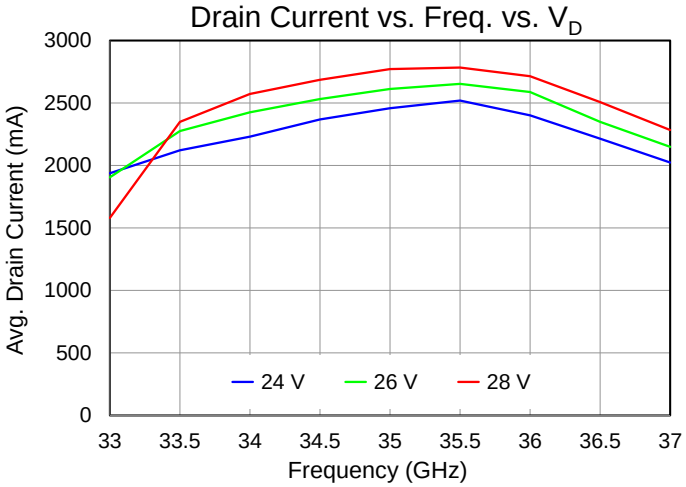


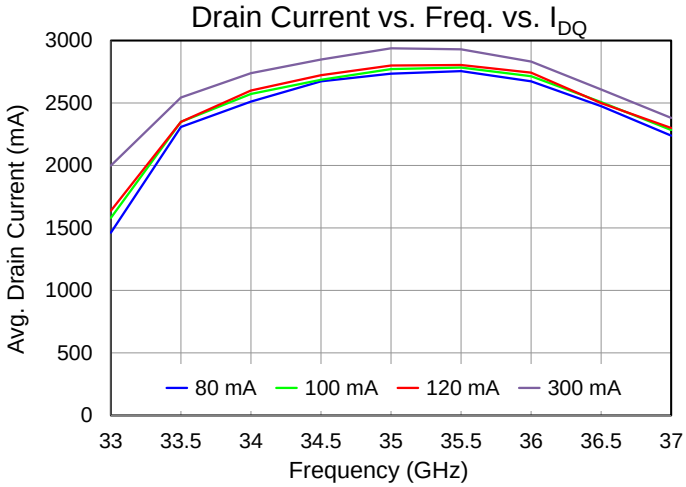
Performance Plots – Large Signal

Test conditions, unless otherwise noted: **Pulsed RF**, V_D = 28 V, I_{DQ} = 100 mA, Duty Cycle = 50%, PW = 50 us, P_{IN} = 28 dBm, T_{BASE} = +25 ºC









Performance Plots – Large Signal

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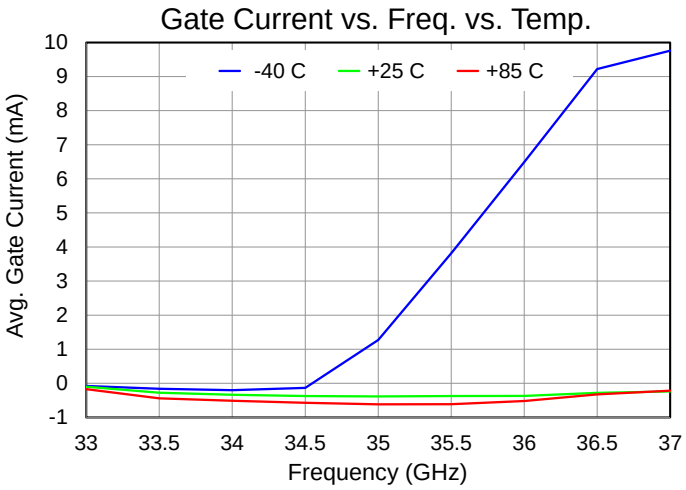

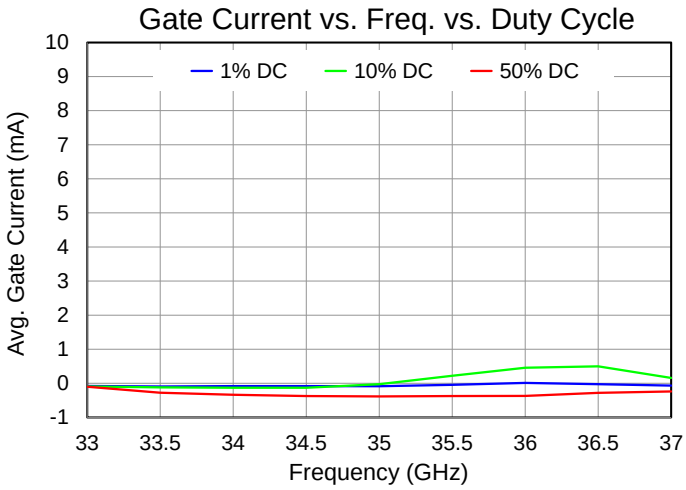

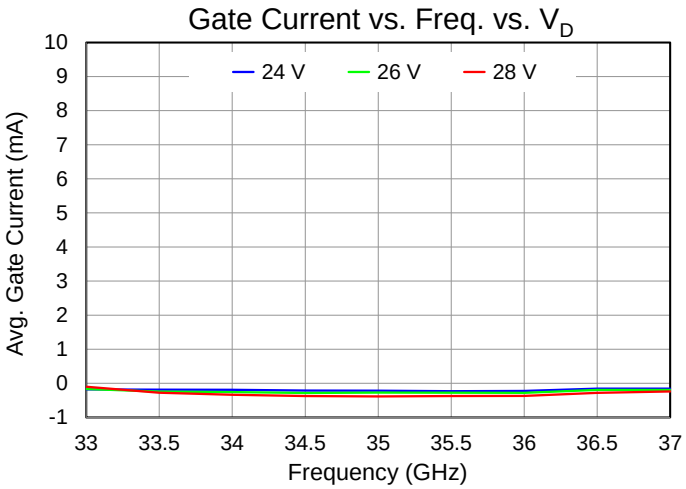

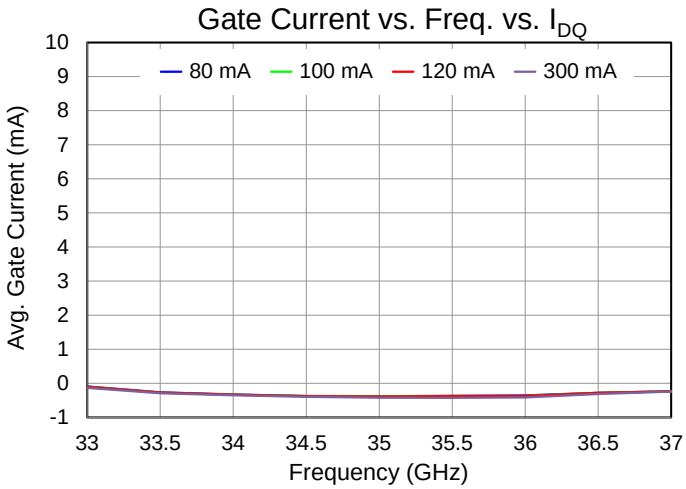

Performance Plots – Large Signal

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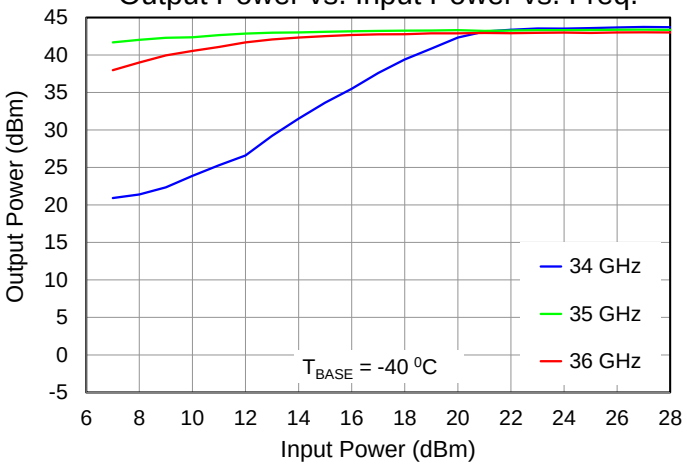
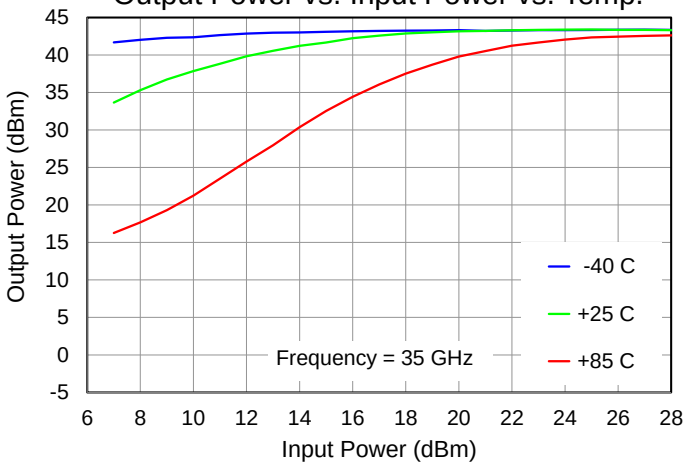
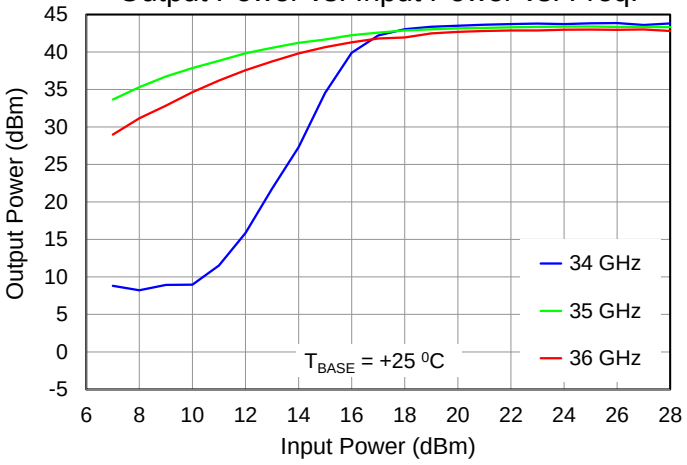
Output Power vs. Input Power vs. Freq.



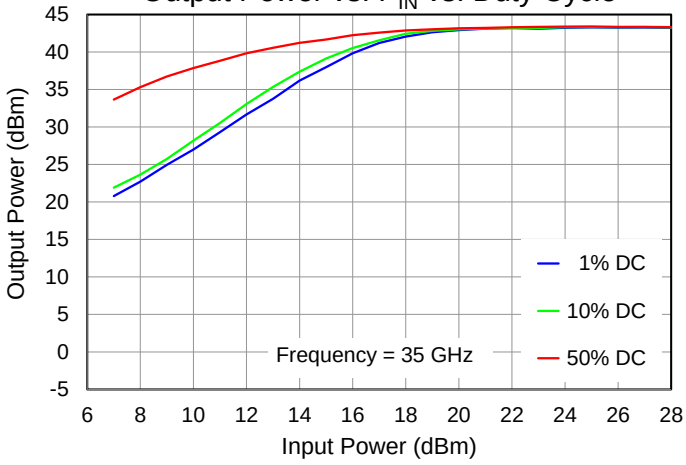
Output Power vs. Input Power vs. Temp.



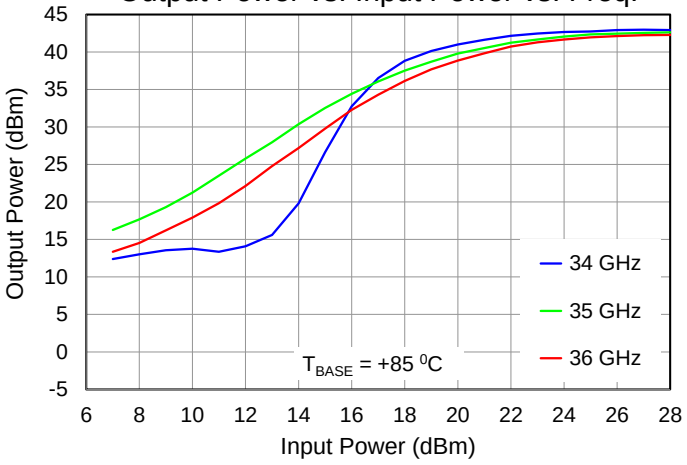
Output Power vs. Input Power vs. Freq.



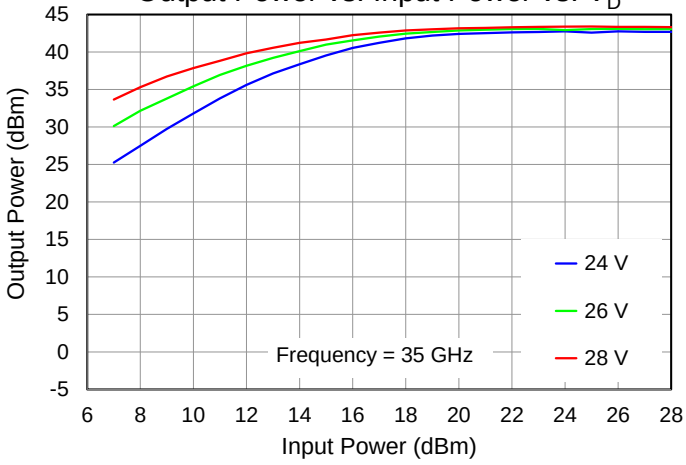
Output Power vs. P_{IN} vs. Duty Cycle



Output Power vs. Input Power vs. Freq.



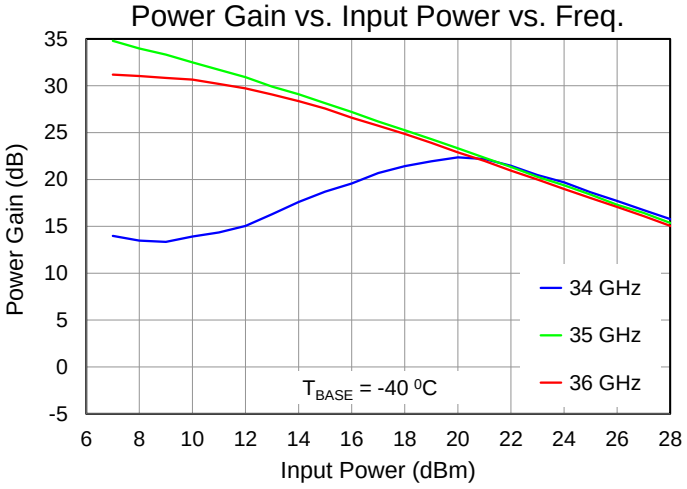
Output Power vs. Input Power vs. V_D



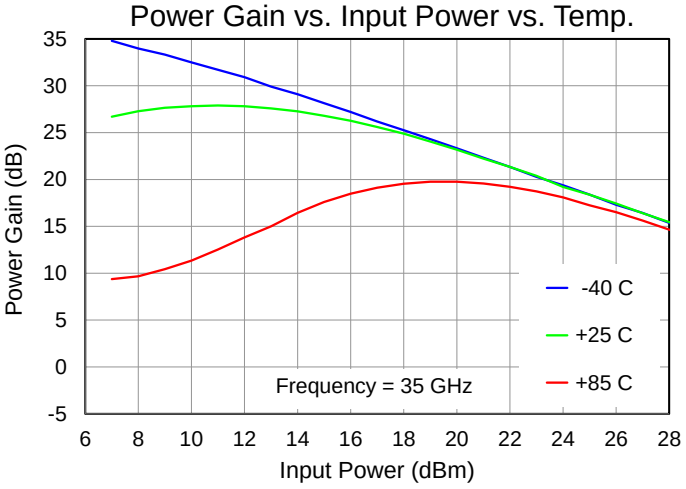
Performance Plots – Large Signal

Test conditions, unless otherwise noted: **Pulsed RF**, V_D = 28 V, I_{DQ} = 100 mA, Duty Cycle = 50%, PW = 50 us, P_{IN} = 28 dBm, T_{BASE} = +25 ºC

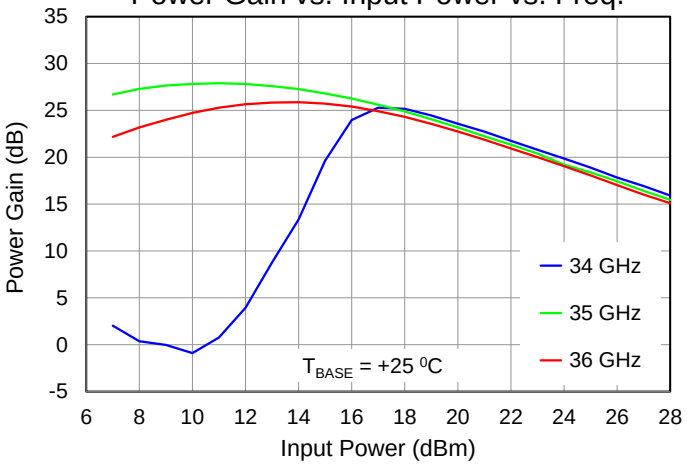
Power Gain vs. Input Power vs. Freq.



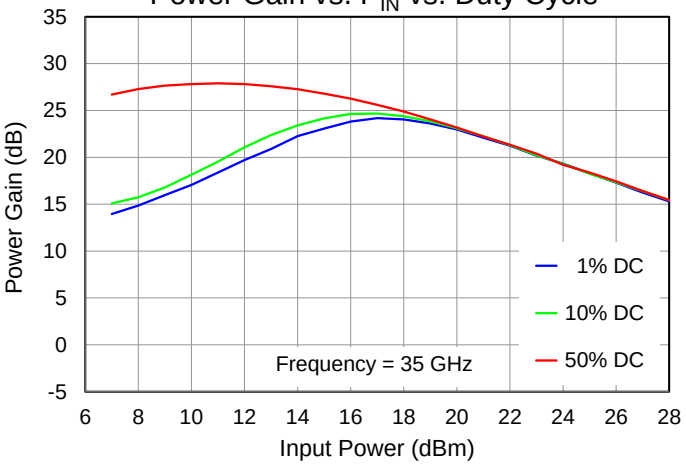
Power Gain vs. Input Power vs. Temp.



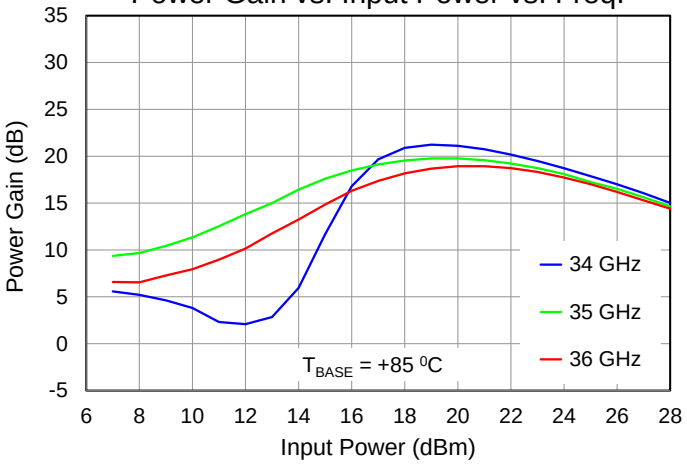
Power Gain vs. Input Power vs. Freq.



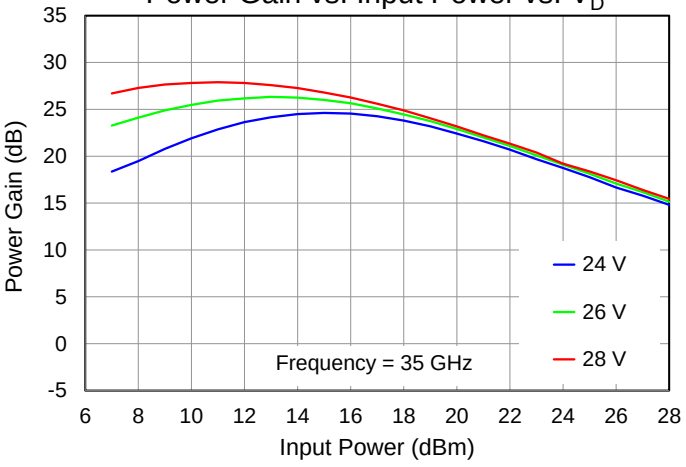
Power Gain vs. P_{IN} vs. Duty Cycle



Power Gain vs. Input Power vs. Freq.



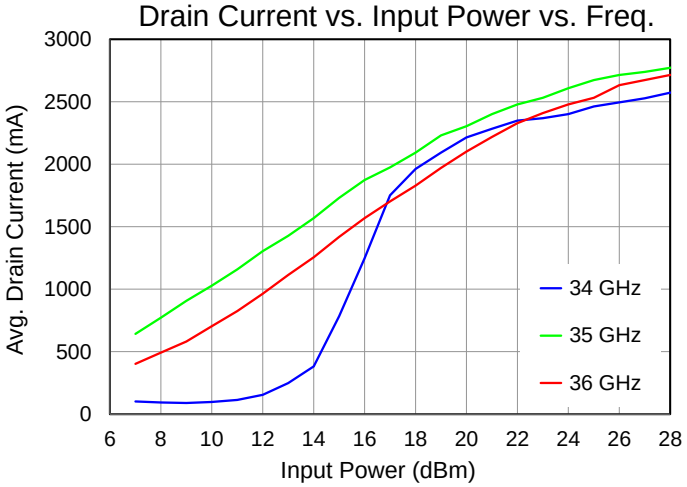
Power Gain vs. Input Power vs. V_D



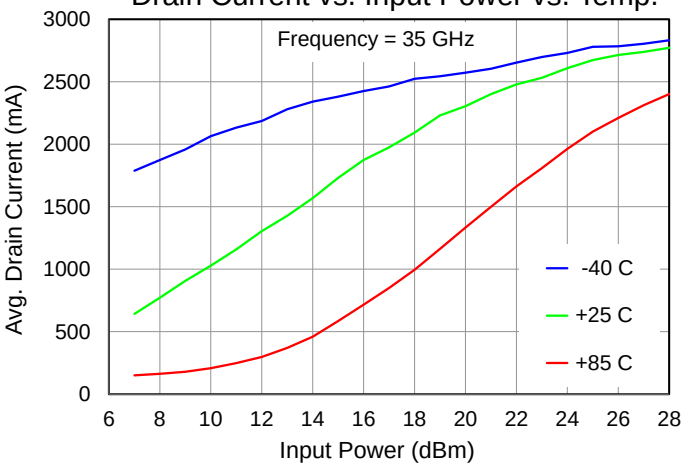
Performance Plots – Large Signal

Test conditions, unless otherwise noted: **Pulsed RF**, V_D = 28 V, I_{DQ} = 100 mA, Duty Cycle = 50%, PW = 50 us, P_{IN} = 28 dBm, T_{BASE} = +25 ºC

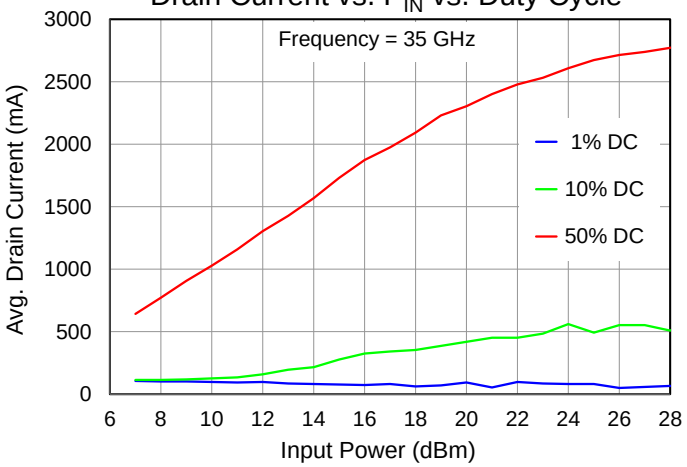
Drain Current vs. Input Power vs. Freq.



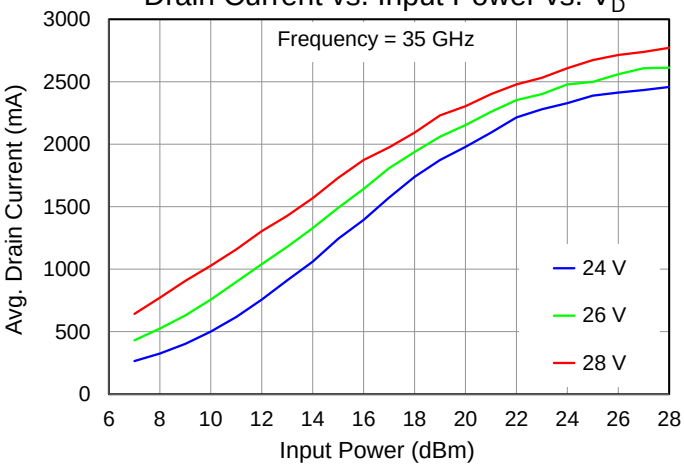
Drain Current vs. Input Power vs. Temp.



Drain Current vs. P_{IN} vs. Duty Cycle



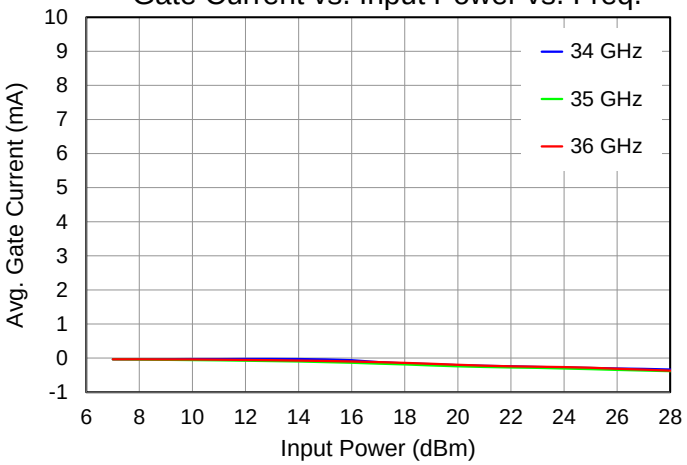
Drain Current vs. Input Power vs. V_D



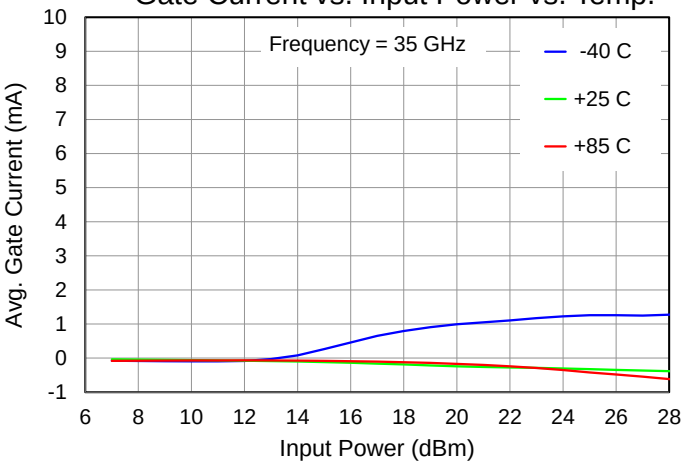
Performance Plots – Large Signal

Test conditions, unless otherwise noted: **Pulsed RF**, V_D = 28 V, I_{DQ} = 100 mA, Duty Cycle = 50%, PW = 50 us, P_{IN} = 28 dBm, T_{BASE} = +25 ºC

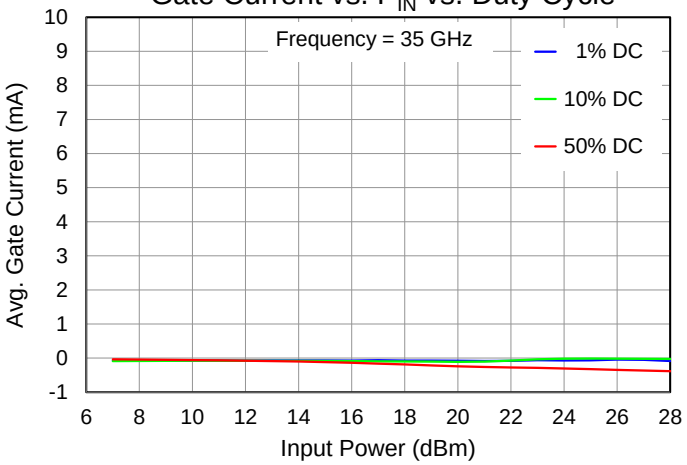
Gate Current vs. Input Power vs. Freq.



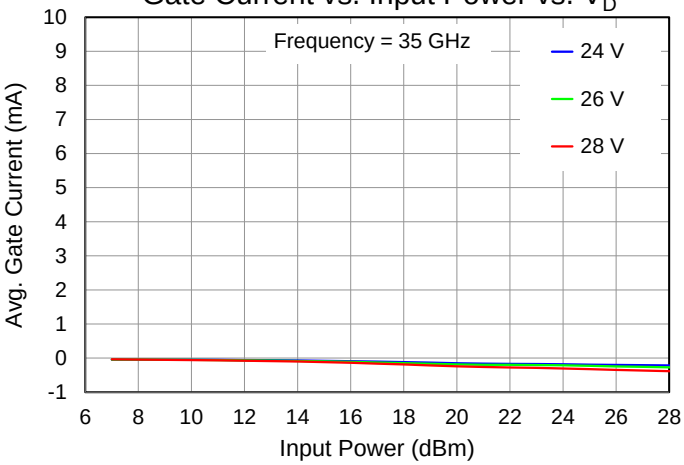
Gate Current vs. Input Power vs. Temp.



Gate Current vs. P_{IN} vs. Duty Cycle

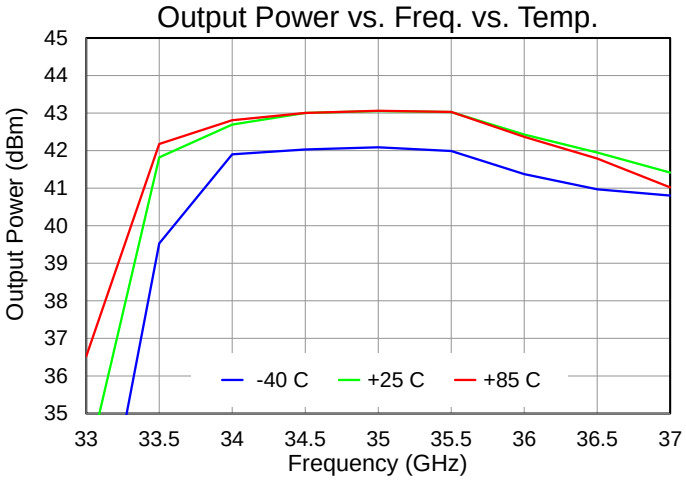


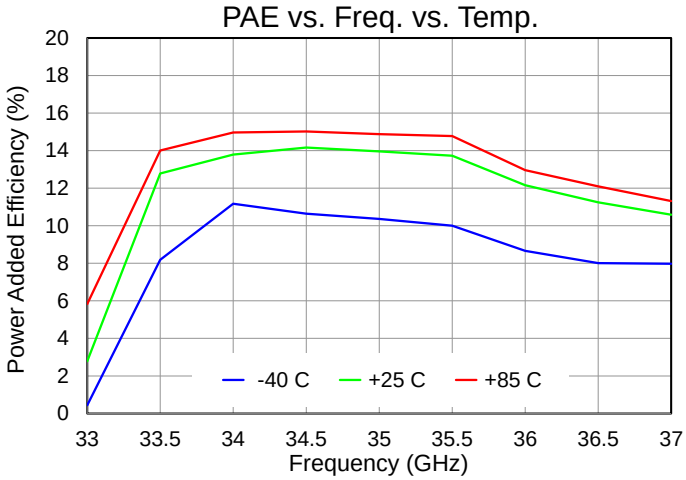
Gate Current vs. Input Power vs. V_D

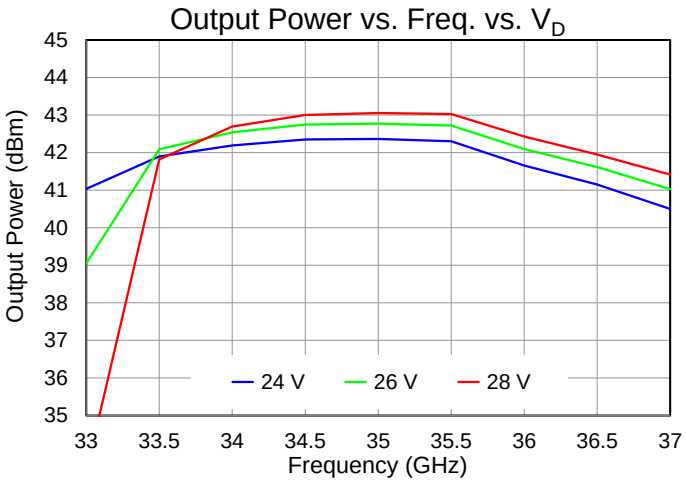


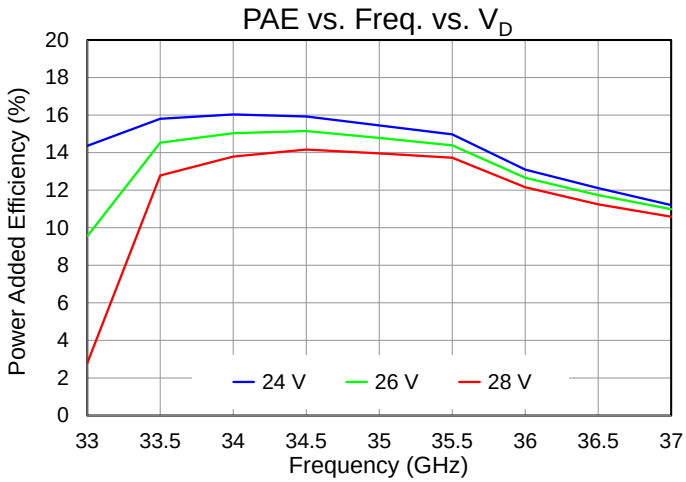
Performance Plots – Large Signal

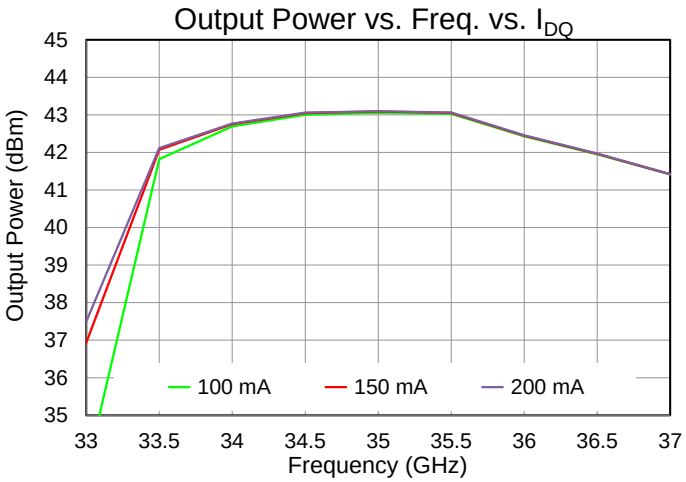
Test conditions, unless otherwise noted: **Pulsed V_D**, V_D = 28 V, I_{DQ} = 100 mA, Duty Cycle = 10%, PW = 200 us, P_{IN} = 28 dBm, T_{BASE} = +25 °C

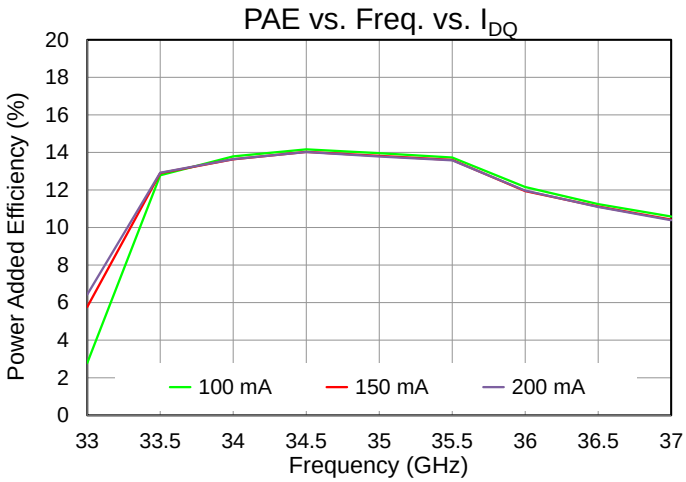












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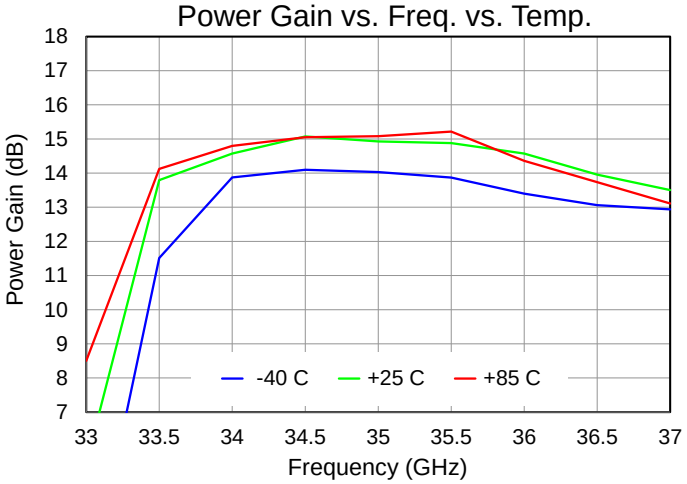
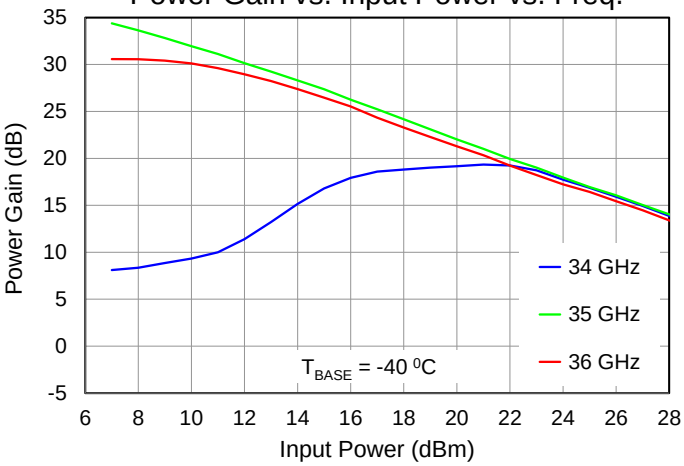
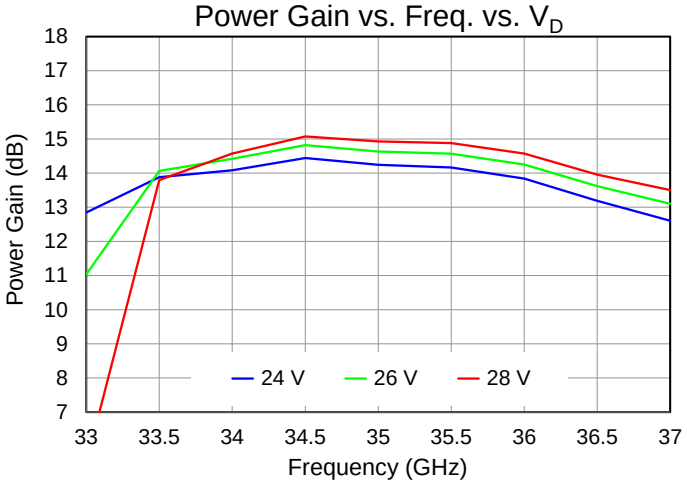
Power Gain vs. Freq. vs. Temp.



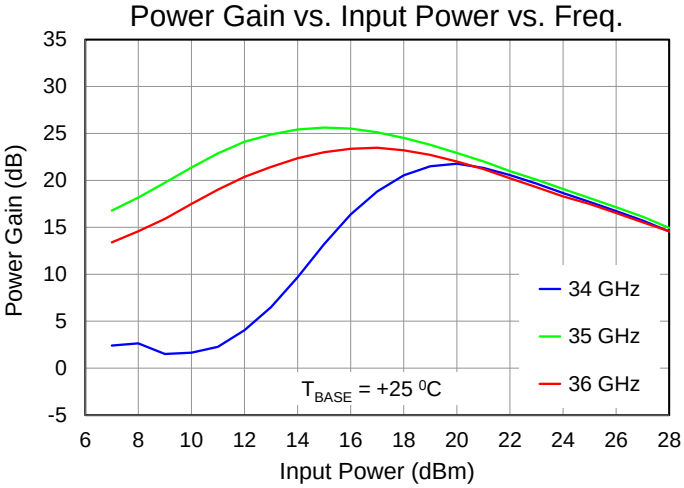
Power Gain vs. Input Power vs. Freq.



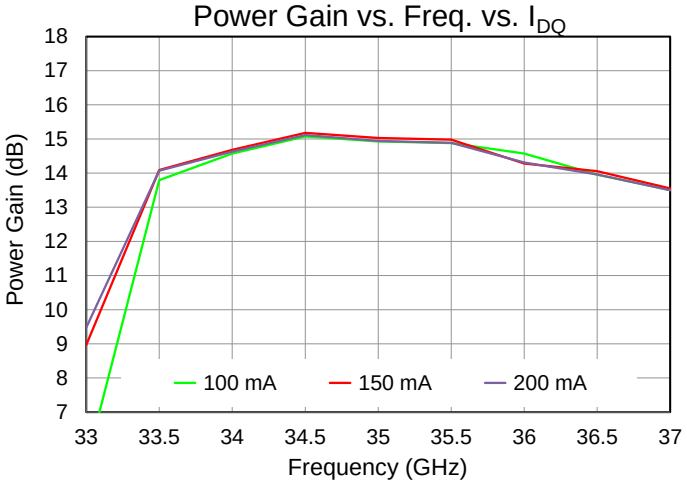
Power Gain vs. Freq. vs. V_D



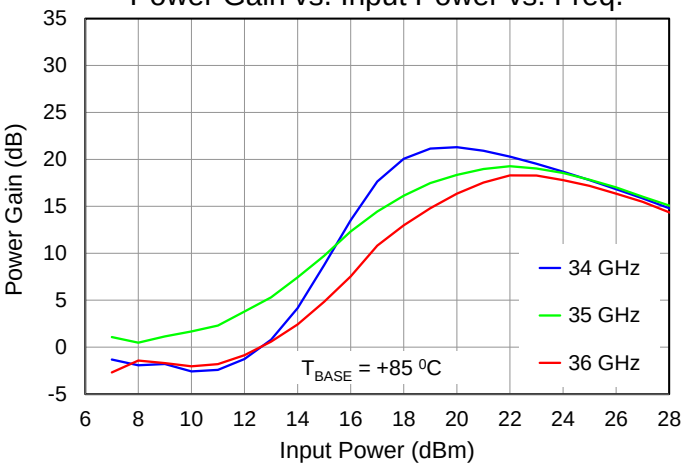
Power Gain vs. Input Power vs. Freq.



Power Gain vs. Freq. vs. I_{DQ}

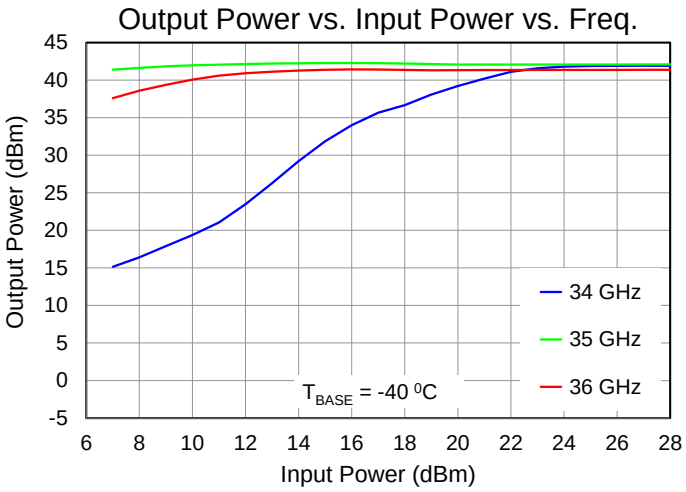


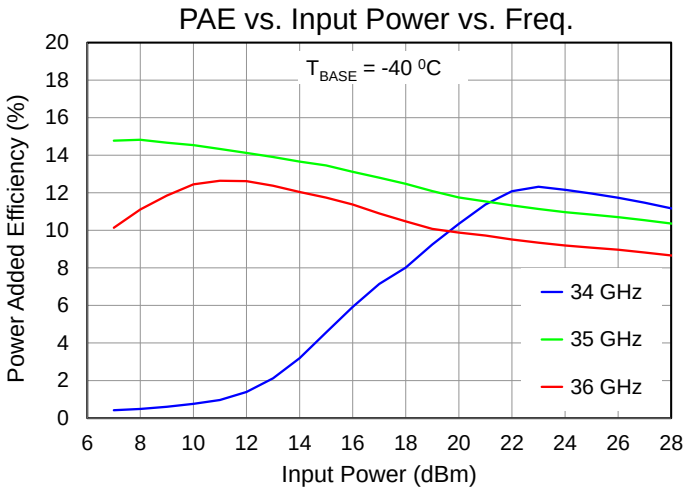
Power Gain vs. Input Power vs. Freq.

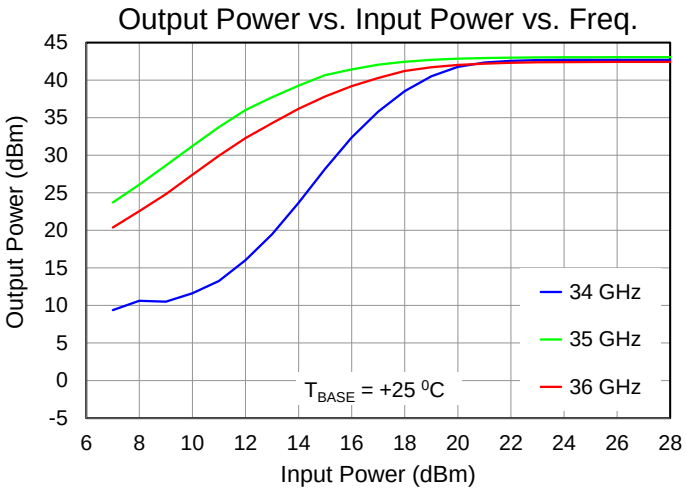


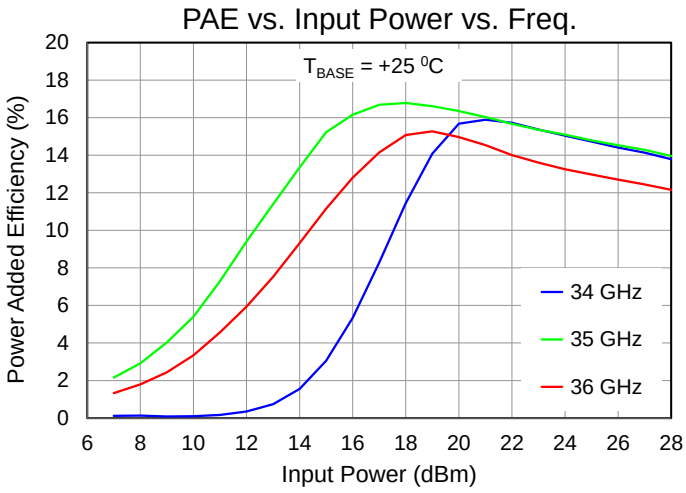
Performance Plots – Large Signal

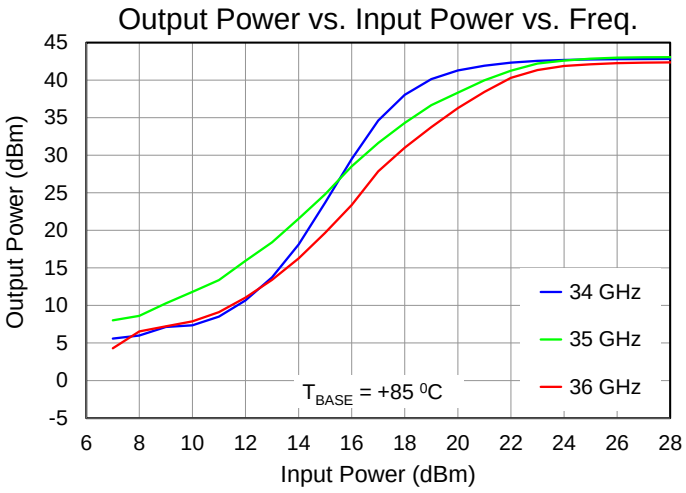
Test conditions, unless otherwise noted: **Pulsed V_D**, V_D = 28 V, I_{DQ} = 100 mA, Duty Cycle = 10%, PW = 200 us, P_{IN} = 28 dBm, T_{BASE} = +25 ºC

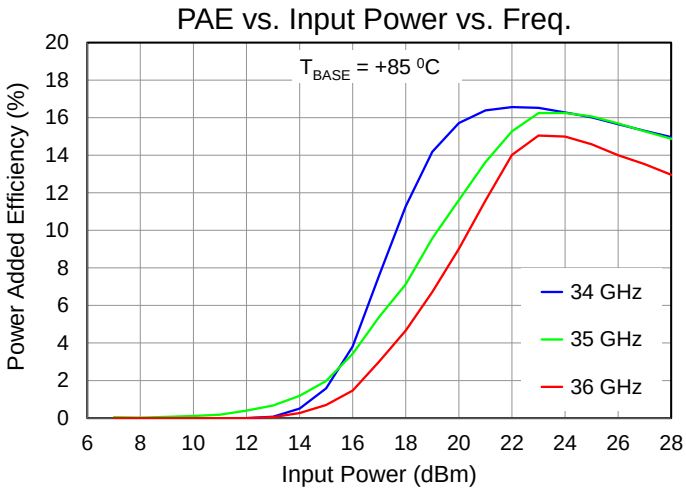








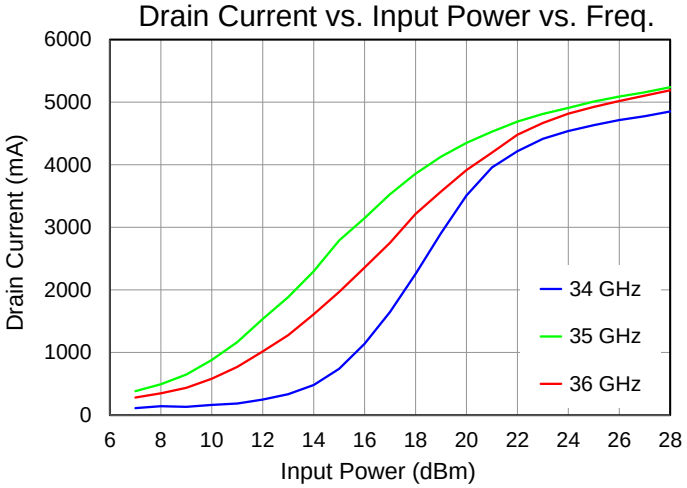




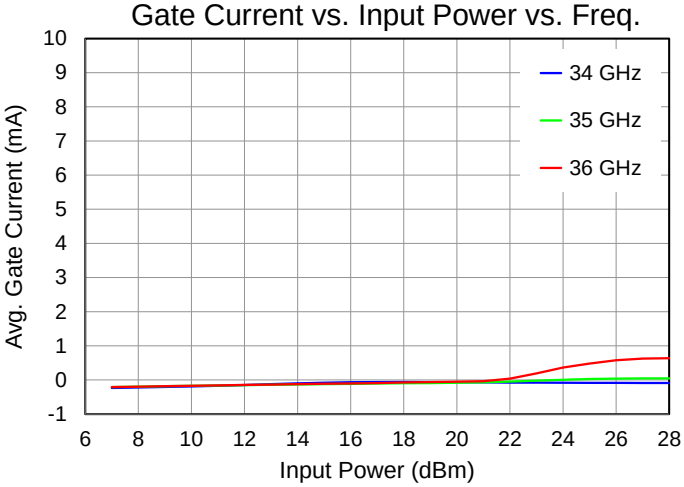
Performance Plots – Large Signal

Test conditions, unless otherwise noted: **Pulsed V_D**, V_D = 28 V, I_{DQ} = 100 mA, Duty Cycle = 10%, PW = 200 us, P_{IN} = 28 dBm, T_{BASE} = +25 ºC

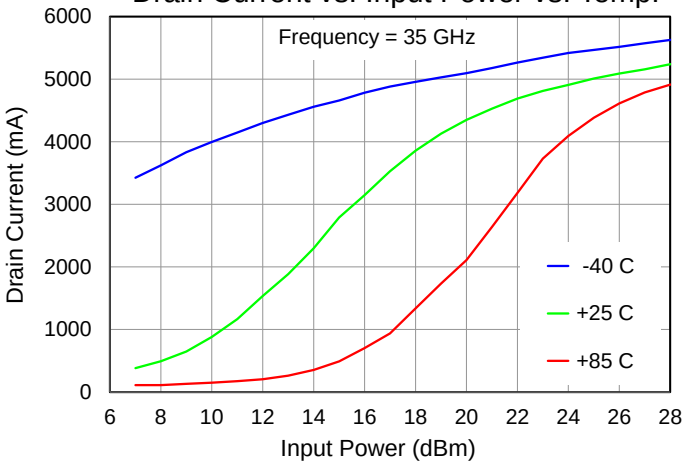
Drain Current vs. Input Power vs. Freq.



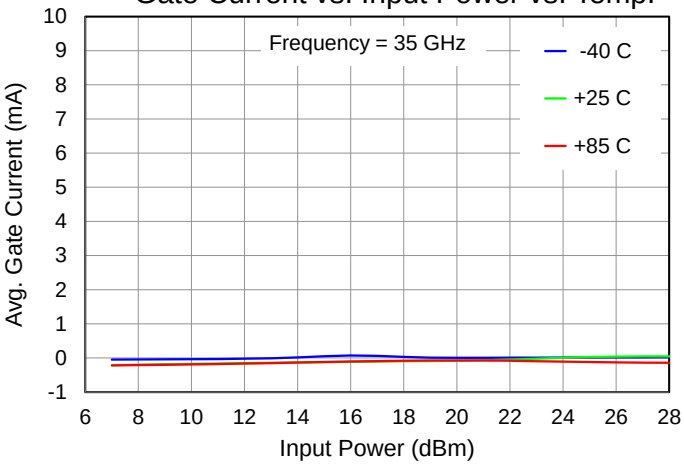
Gate Current vs. Input Power vs. Freq.



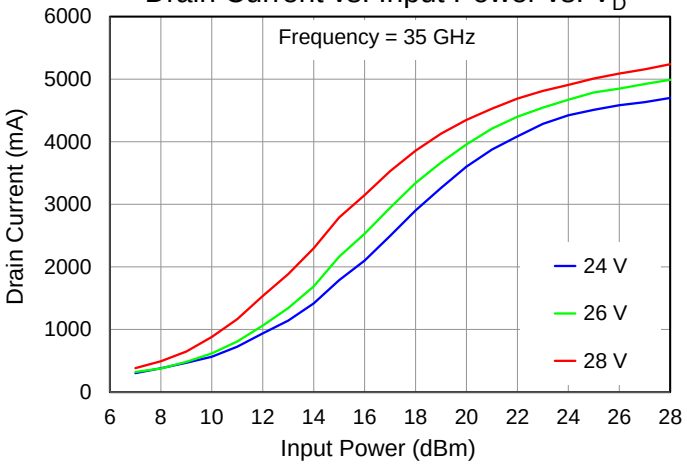
Drain Current vs. Input Power vs. Temp.



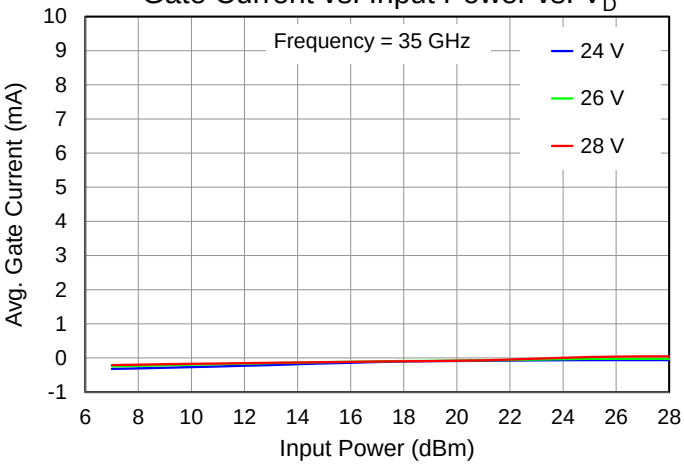
Gate Current vs. Input Power vs. Temp.



Drain Current vs. Input Power vs. V_D



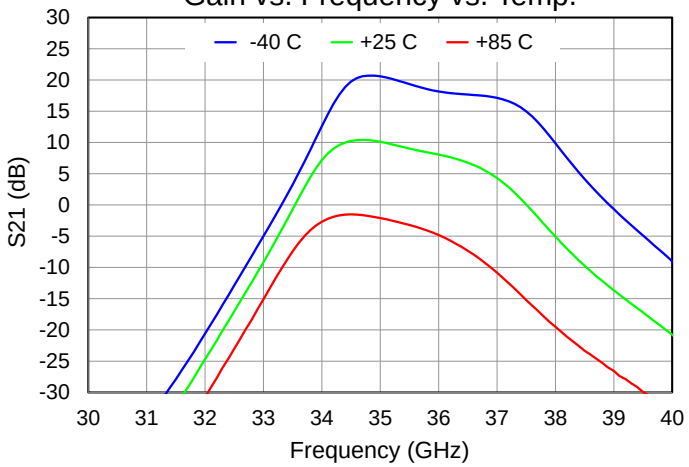
Gate Current vs. Input Power vs. V_D



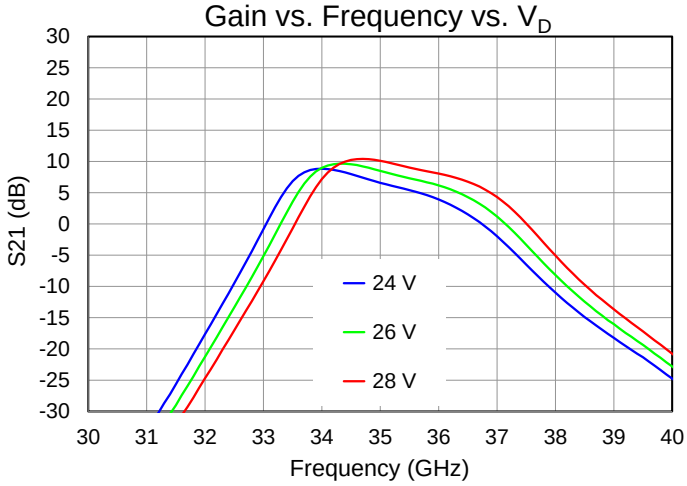
Performance Plots – Small Signal

Test conditions, unless otherwise noted: CW, V_D = 28 V, I_{DQ} = 100 mA, T_{BASE} = +25 ºC

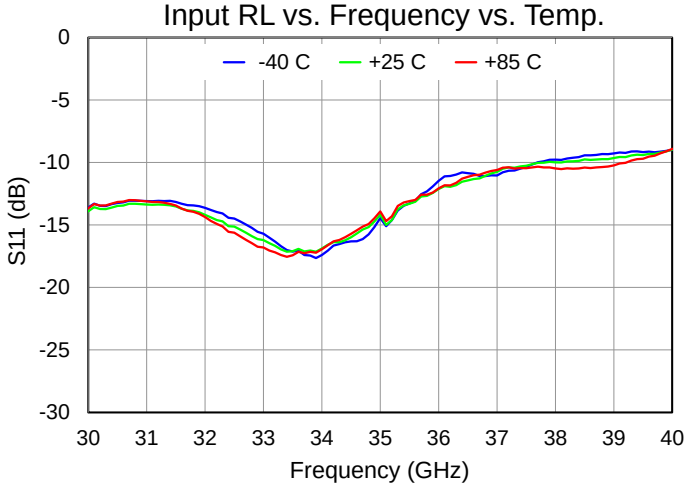
Gain vs. Frequency vs. Temp.



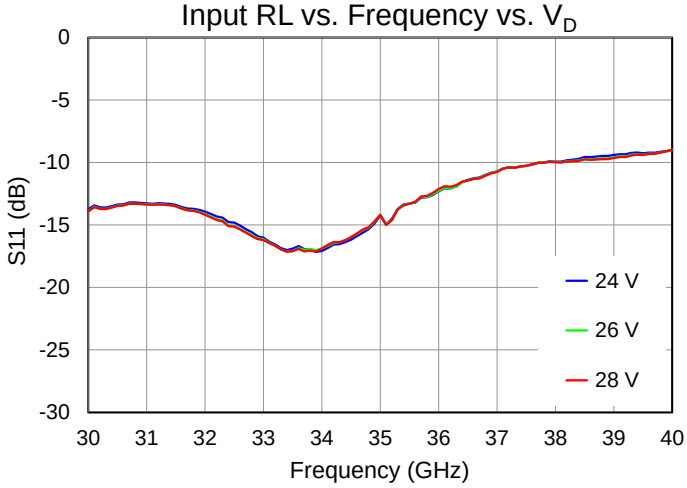
Gain vs. Frequency vs. V_D



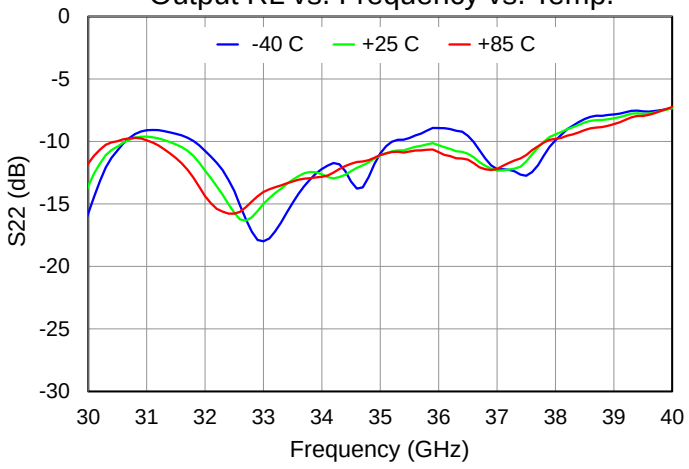
Input RL vs. Frequency vs. Temp.



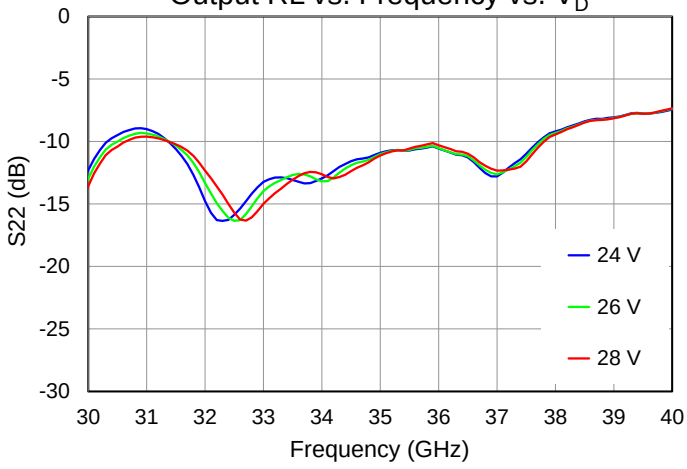
Input RL vs. Frequency vs. V_D



Output RL vs. Frequency vs. Temp.

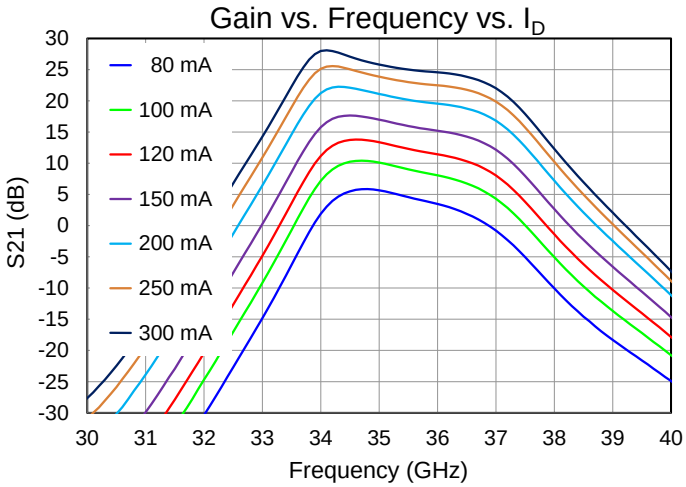


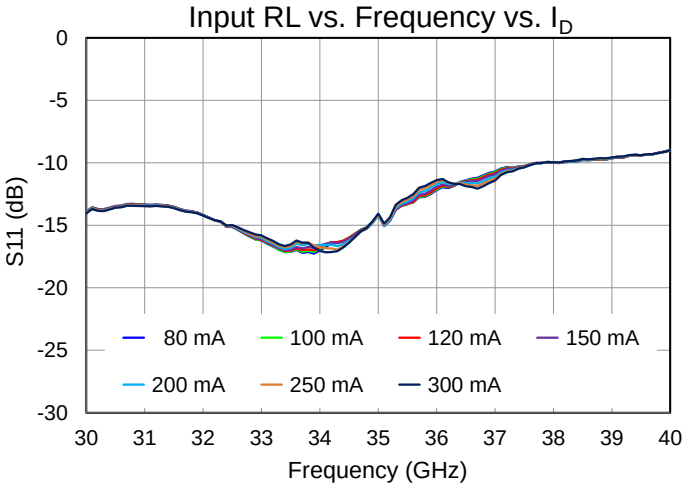
Output RL vs. Frequency vs. V_D

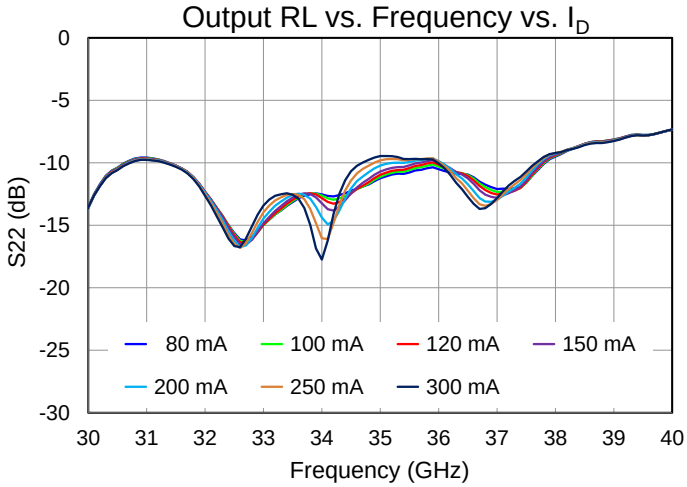


Performance Plots – Small Signal

Test conditions, unless otherwise noted: CW, V_D = 28 V, I_{DQ} = 100 mA, T_{BASE} = +25 ºC







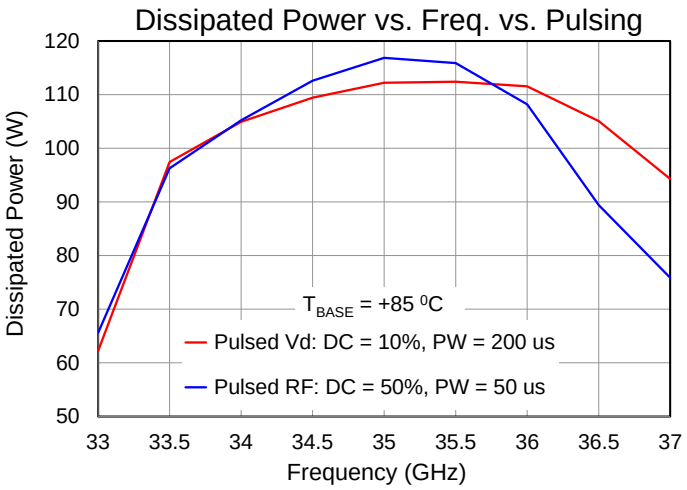
Thermal and Reliability Information

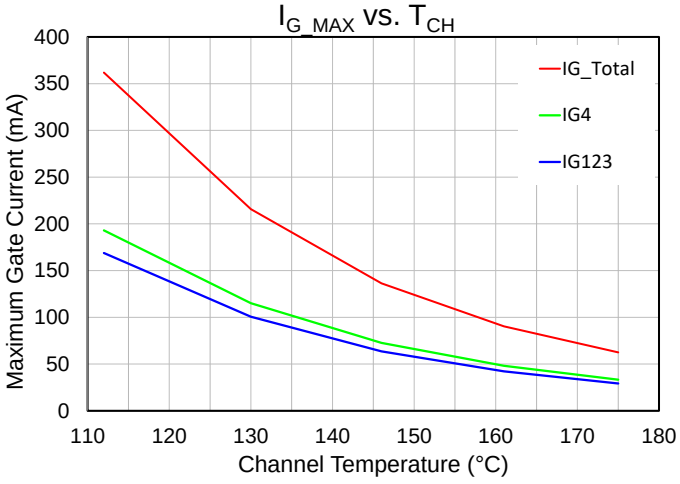
Parameter	Test Conditions	Value	Units
Thermal Resistance, θ_{JC} (1)	Quiescent T_{BASE} = 85 °C, V_D = 28 V, I_{DQ} = 100 mA P_{DISS} = 2.8 W	1.0	ºC/W
Channel Temperature, T_{CH} (2)		88	°C
Thermal Resistance, θ_{JC} (1)	Pulsed RF, T_{BASE} = 85 °C, V_D = 28 V, I_{DQ} = 100 mA, Freq = 35 GHz, I_{D_Drive} = 4.8 A, DC = 50%, PW = 50 us, P_{IN} = 28 dBm, P_{OUT} = 42.5 dBm P_{DISS} = 117 W	0.85	ºC/W
Channel Temperature, T_{CH} (2)		185	°C
Thermal Resistance, θ_{JC} (1)	Pulsed V_D, T_{BASE} = 85 °C, V_D = 28 V (27 V at DUT), I_{DQ} = 100 mA, Freq = 35 GHz, I_{D_Drive} = 4.9 A, DC = 10%, PW = 200 us, P_{IN} = 28 dBm, P_{OUT} = 43 dBm, P_{DISS} = 113 W	0.80	ºC/W
Channel Temperature, T_{CH} (2)		175	°C

Notes:

1. Thermal resistance determined to the back of carrier plate CuMo
2. Channel temperature indicated is an IR scan equivalent temperature. Thermal resistance is calculated using this value. Additional information can be found in the Qorvo Applications Note “GaN Device TCHMAX Theta-JC and Reliability Estimates,” located here https://www.qorvo.com/products/d/da006480

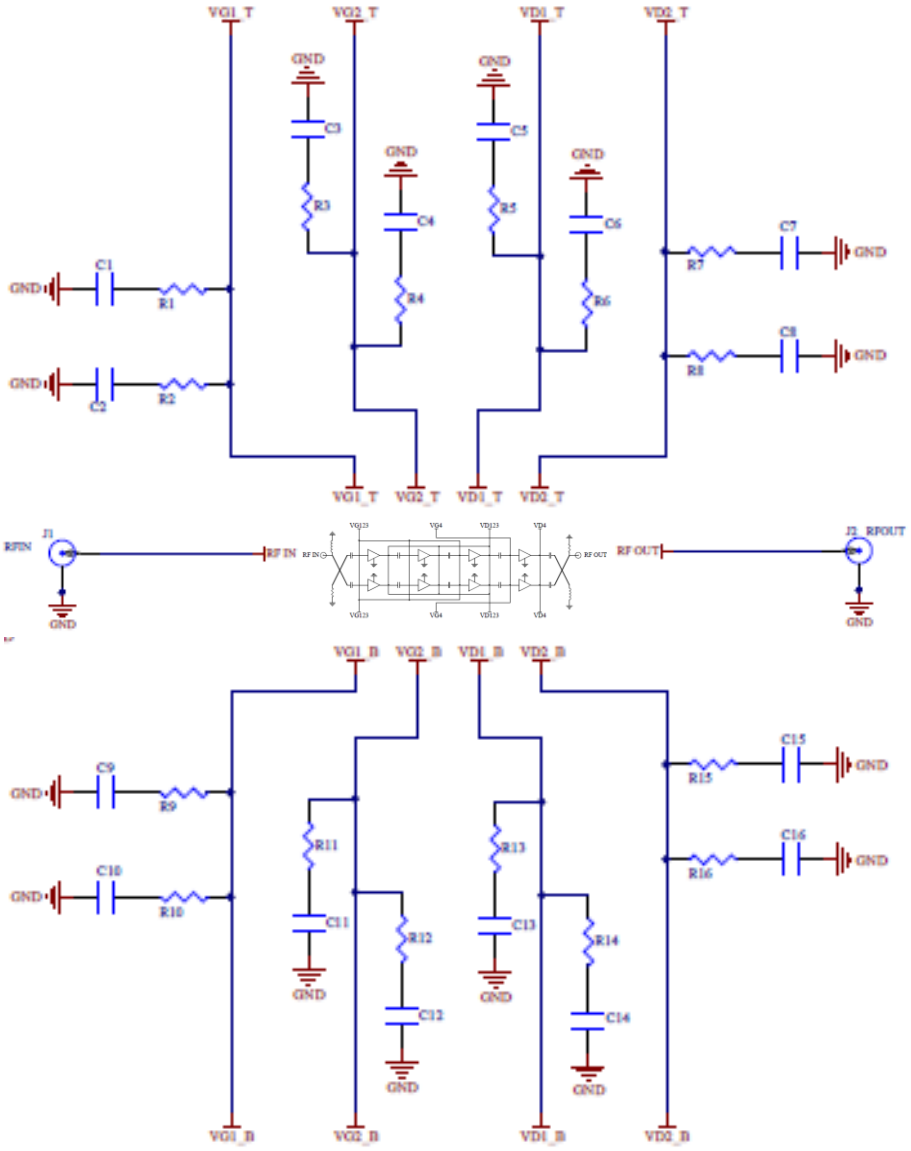
Dissipated Power and Maximum Gate Current





Test conditions, unless otherwise noted: Pulsed, V_D = 28 V, I_{DQ} = 100 mA, P_{IN} = 28 dBm, T_{BASE} = +85 ºC
Channel Temperature is of thermal modeling, not an IR scan

Applications Information



DC can be applied from top, bottom, or both sides of the die;
External bypassing required on both sides

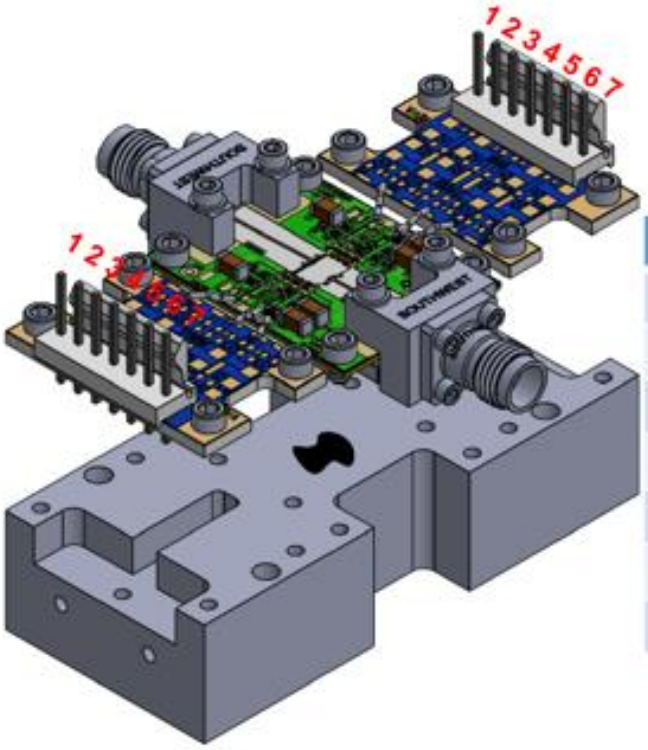
Bias-Up Procedure

1. Set I_D limit to 6.4 A, I_G limit to 30 mA
2. Set V_G to −4.0 V
3. Set V_D +28 V. Ensure I_{DQ} ~ 0 mA
4. Adjust V_G more positive until I_{DQ} = 100 mA (V_G ≈ -2.5V +/- typical)
5. Apply RF signal

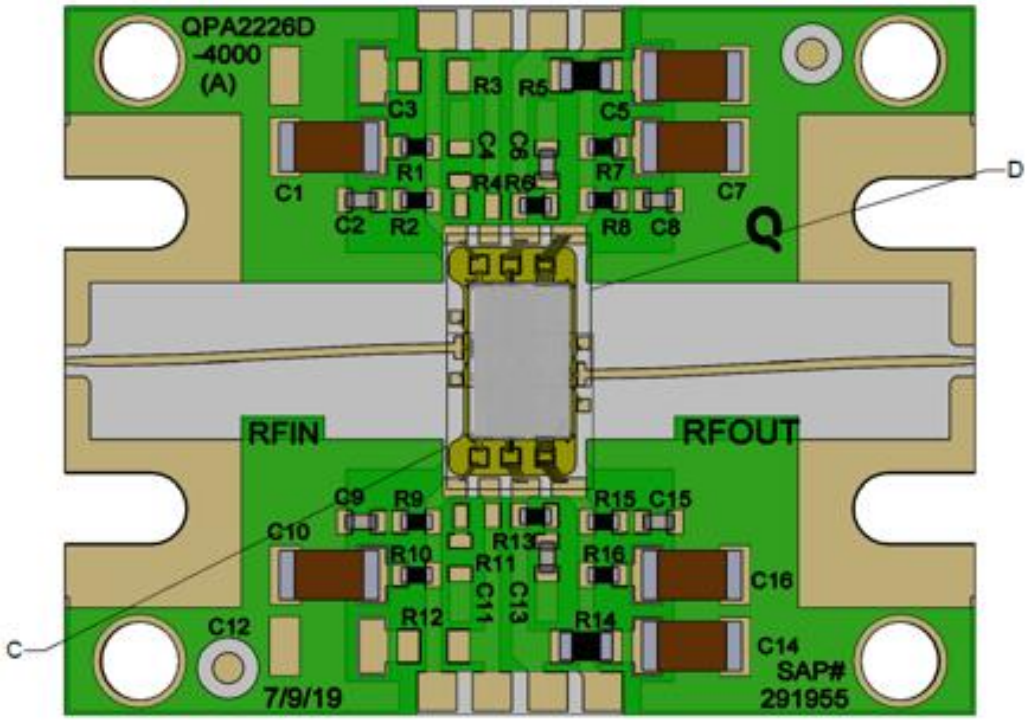
Bias-Down Procedure

1. Turn off RF signal
2. Reduce V_G to −4.0 V. Ensure I_{DQ} ~ 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

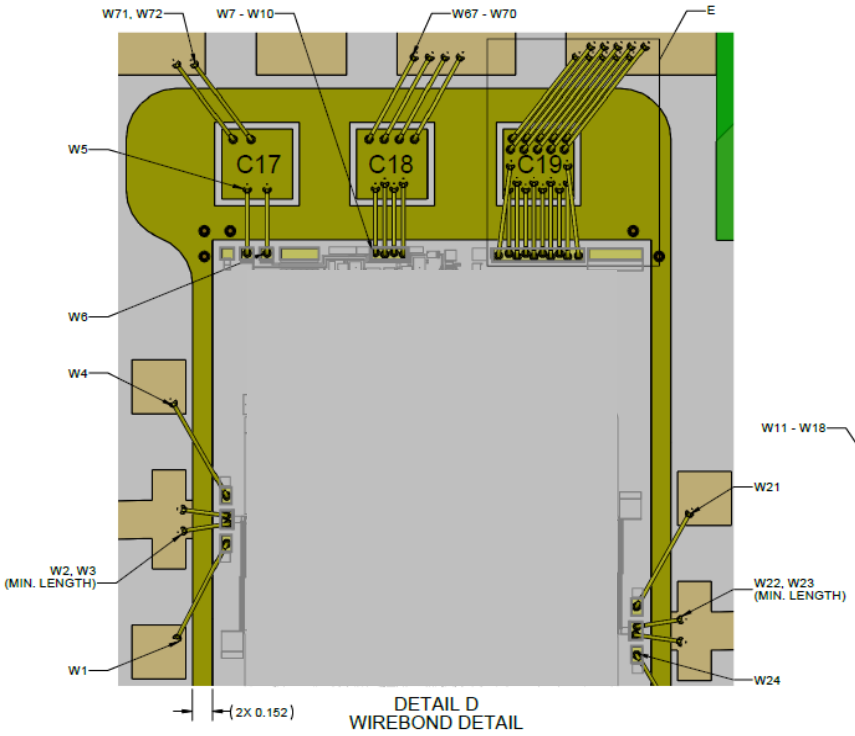
Evaluation Board (EVB) Layout – V_D Pulsed

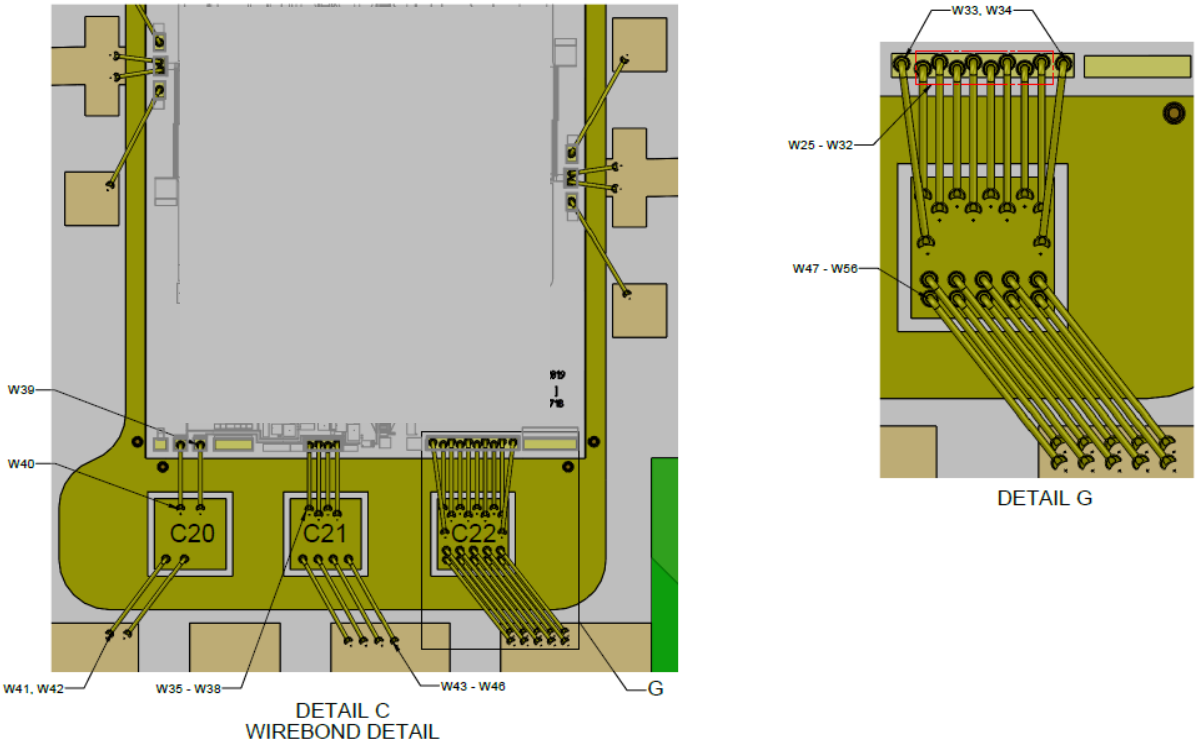


Pin	Name
1	Ground
2	V_G
3	n/c
4	Ground
5	V_D
6	V_D
7	Ground



Evaluation Board (EVB) Layout – V_D Pulsed (con't)



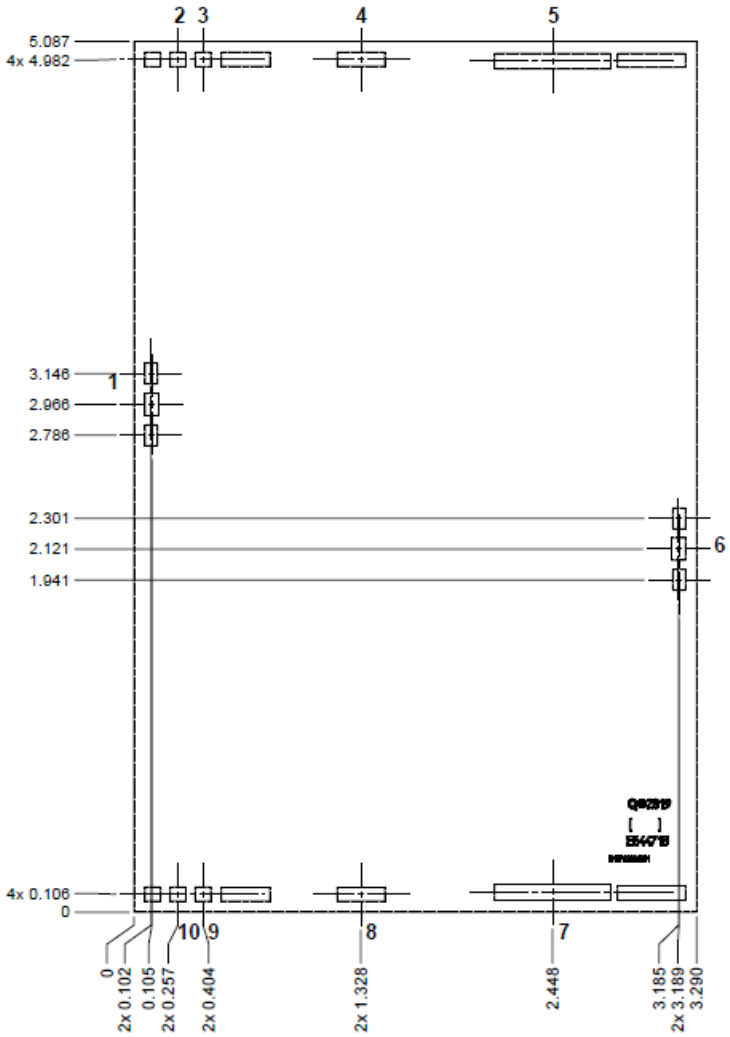


Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C1, C10	10 uF	CAP, 10uF, 20%, 50V, 20%, X5R, 1206	Various	
C2, C6, C8, C9, C13, C15	0.01 uF	CAP, 0.01uF, ±10%, 50V, X7R, 0402	Various	
C5, C7, C14, C16 *	1 uF	For V_D pulsed; CAP, 1uF, ±5%, 50V, X7R, 1206	Various	
	10 uF	For RF pulsed; CAP, 10uF, 20%, 50V, 20%, X5R, 1206	Various	
C17 – C22	820 pF	CAP, 820pF, ±10%, 50V, SL	Various	
R1, R2, R9, R10	5.1 Ω	RES, 5.1 Ohm, 5%, 50V, 0402	Various	
R5, R14	0 Ω	RES, 0 Ohm, 1/10W, 0603	Various	
R6, R7, R8, R13, R15, R16	0 Ω	RES, 0 Ohm, JMPR, 0402	Various	
H1, H2	-	CONN, HDR, Male-vert, 7 PIN, 1 RAW, MTA	Various	
J1, J2	-	Connector, RF 2.4mm, 1492-04A-5	Southwest Microwave	1492-04A-5
CP	-	Carrier Plate, CuMo, 0.9 x 1.15 x 0.02T	Various	Custom
PCB_MMIC	-	PCB for MMIC, Rogers 6202 0.005in, 0.5oz Ni/Au plating both sides, total thickness 0.009in	Various	Custom
PCB,_Bias	-	PCB for DC Bias	Various	Custom
H-Block	-	H-Block, Copper C110, 1.14 x 2.49 x 0.59T	Various	Custom
AuSn	-	AuSn Solder preform		
Epoxy	-	Epoxy preform		
Ablebond	-	Epoxy, Ablebond 84-1LMI		
Solder	-	Paste, solder, Syntech, Sn62/Pb36/Ag2		
TC	-	Thermal Compound, Silver 5GR		
S1 – S12	-	Screw, Cap, Socket Head, 2-56X1/8”		

* Qorvo EVB is for V_D pulsed

Mechanical Information



Dimensions: mm; Thickness: 0.05 mm; Die x, y size tolerance: ± 0.050; Ground is backside of die

Bond Pad Description

Pad No.	Symbol	Pad Size (mm)	Description
1	RF_{IN}	0.081 x 0.131	RF Input. Matched to 50 Ω, DC blocked, DC shorted to ground
2, 10	V_{G123}	0.091 x 0.082	Gate voltage for stage 1, 2, 3. External bypassing required; refer to page 18 for recommendation
3, 9	V_{G4}	0.091 x 0.082	Gate voltage for stage 4. External bypassing required; refer to page 18 for recommendation
4, 8	V_{D123}	0.279 x 0.081	Drain voltage for stage 1, 2, 3. External bypassing required; refer to page 18 for recommendation
5, 7	V_{D4}	0.614 x 0.091	Drain voltage for stage 4. External bypassing required; refer to page 18 for recommendation
6	RF_{OUT}	0.081 x 0.131	RF Output. Matched to 50 Ω, DC blocked, DC shorted to ground

Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300 °C to 3 – 4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonic are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1C	ANSI/ESD/JEDEC JS-001

Caution!

ESD-Sensitive Device

Solderability

Use only AuSn (80/20) solder, and limit exposure to temperatures above 300 °C to 3 – 4 minutes, maximum.

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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