TGA4548

17 - 20 GHz 10 W GaN Power Amplifier

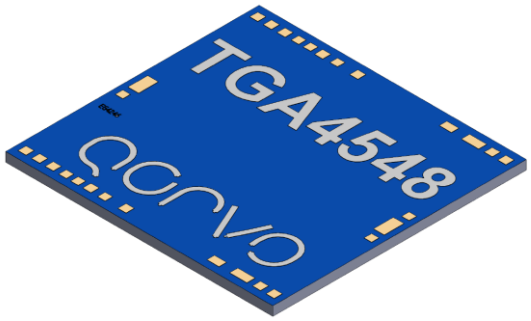
Product Overview

Qorvo's TGA4548 is a high frequency, high power MMIC amplifier fabricated on Qorvo's production 0.15um GaN on SiC process (QGaN15). The TGA4548 operates from 17 – 20 GHz and typically provides 10 W saturated output power with power-added efficiency of 25% and large-signal gain of 18 dB. This combination of high frequency performance provides the flexibility designers are looking for to improve system performance while reducing size and cost. The TGA4548 also has an integrated power detector to support system diagnostics and other needs.

The TGA4548 is matched to 50Ω with integrated DC blocking capacitors on both RF I/O ports simplifying system integration. The frequency coverage and operational flexibility allows it support satellite communication as well as point to point data links.

The TGA4548 is 100% DC and RF tested on-wafer to ensure compliance to electrical specifications.

Lead-free and RoHS compliant.



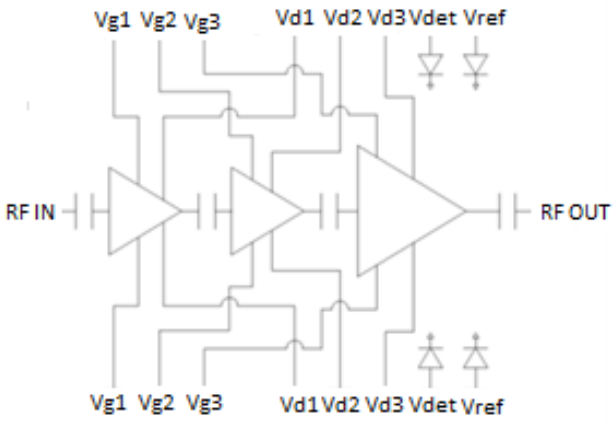
2.95 x 2.80 x .10 mm Die Size

Key Features

- Frequency Range: 17 – 20 GHz
- P_{SAT} (P_{IN}=22 dBm): 40 dBm
- PAE (P_{IN}=22 dBm): 25 %
- Small Signal Gain: 30 dB
- Integrated Power Detector
- Bias: $V_{D1} = V_{D2} = V_{D3}$ = +28 V, $I_{D1} + I_{D2} + I_{D3}$ = 300 mA
- Chip Dimensions: 2.95 x 2.80 x 0.10 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Applications

- Point-to-Point Radio
- Satellite Communications

Ordering Information

Part No.	Description
TGA4548	Waffle tray with 25 pcs
TGA4548EVB	Evaluation board
QPA4548S	Space Inspected Version; contact Sales

Absolute Maximum Ratings

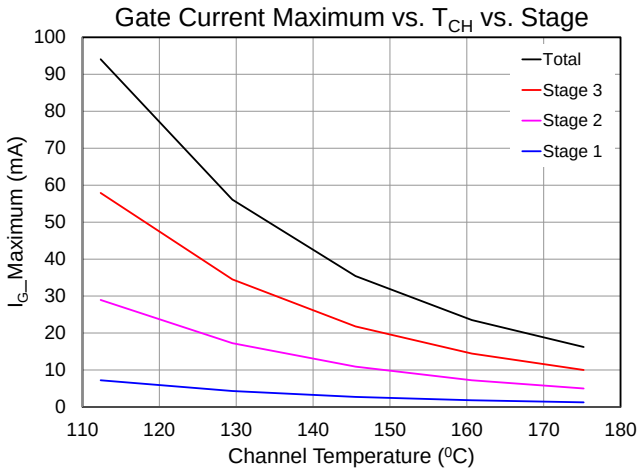
Parameter	Rating
Drain Voltage (V_D)	29.5 V
Gate Voltage Range (V_G)	-8 to 0 V
Drain Current Stage 1 (I_{D1}), Top or Bottom	500 mA
Drain Current Stage 2 (I_{D2}), Top or Bottom	500 mA
Drain Current Stage 3 (I_{D3}), Top and Bottom	2 A
Gate Current (I_G),	See chart
RF Input Power, CW, 50 Ω, T_{BASE} = 25 °C	26 dBm
Dissipated Power (P_{DISS}), CW, T_{BASE} = 85°C	43 W
Reference Power Detect (I_{ref})	4 mA
Power Detect Diode (I_{det})	4 mA
Storage Temperature	−55 to +150 °C
Mounting Temperature (30 seconds)	320 °C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ.	Max	Units
Drain Voltage (V_D)		+28		V
Drain Current, Quiescent (I_{DQ})		300		mA
Drain Current, RF (I_{D_Drive})	See chart page 5			mA
Gate Voltage Typ. Range (V_G)	−2.1 to -2.8			V
Operating Temp. Range	−40	+25	+85	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.



Electrical Specifications

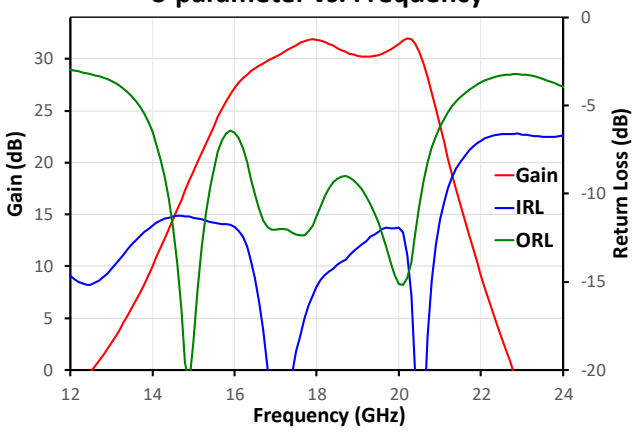
Parameter	Conditions [1]	Min	Typ.	Max	Units
Operational Frequency Range	Unless Otherwise	17		20	GHz
Output Power at Saturation, P_{SAT}	P_{IN} = +22 dBm		40		dBm
Power Added Efficiency, PAE	P_{IN} = +22 dBm		25		%
Small Signal Gain			30		dB
Input Return Loss			15		dB
Output Return Loss			12		dB
Third Order Intermodulation, IM3	Pout = +34 dBm/tone		-25		dBc
S21 Temperature Coefficient	T_{diff} = (85 – (-40)) °C		-0.06		dB/°C
P_{SAT} Temperature Coefficient	T_{diff} = (85 – (-40)) °C, P_{in} = +22 dBm		-0.02		dBm/°C

Notes:
1. Test conditions unless otherwise noted: CW, $V_{D1} = V_{D2} = V_{D3}$ = 28V, $I_{D1} + I_{D2} + I_{D3}$ = 300mA, adjusting $V_{G1} = V_{G2} = V_{G3}$, T_{BASE} = +25 °C, Z_0 = 50 Ω
2. T_{BASE} is back side of carrier plate

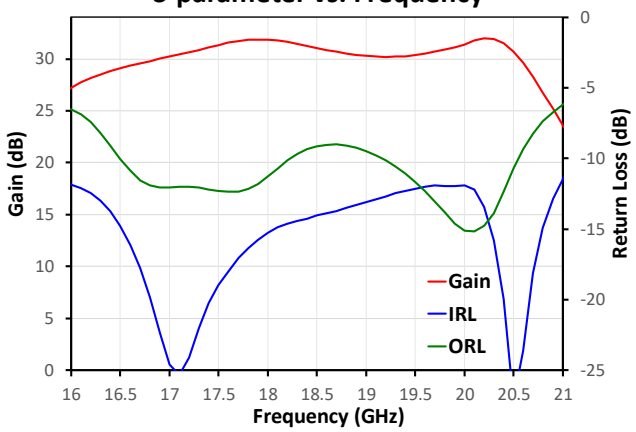
Performance Plots

Test conditions unless otherwise noted: CW, $V_{D1} = V_{D2} = V_{D3} = 28V$, $I_{D1} + I_{D2} + I_{D3} = 300mA$, adjusting $V_{G1} = V_{G2} = V_{G3}$, $T_{BASE} = +25\,°C$, $Z_0 = 50\,\Omega$

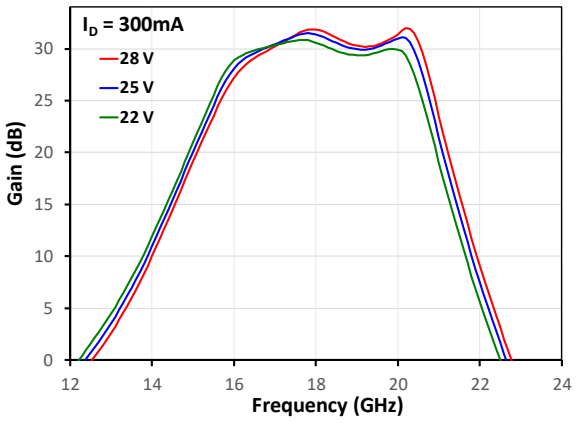
S-parameter vs. Frequency



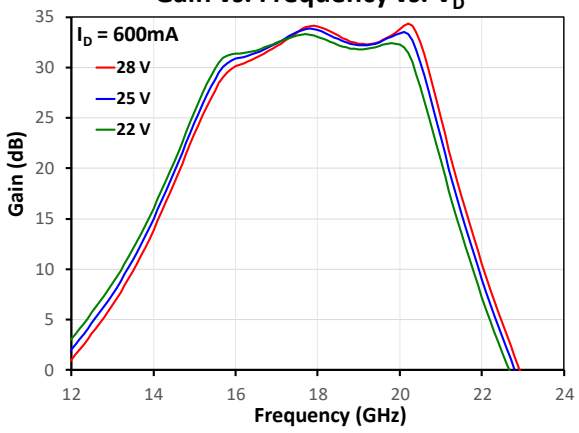
S-parameter vs. Frequency



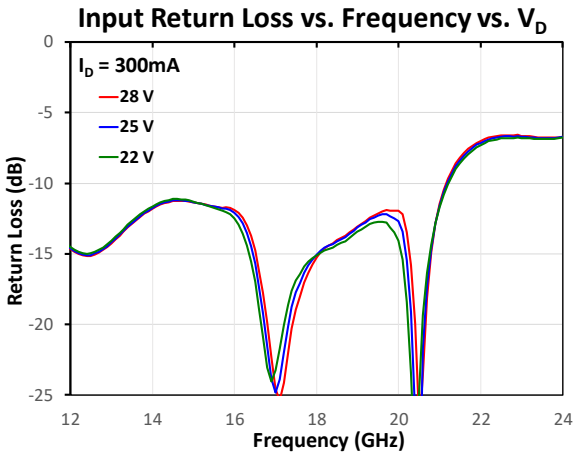
Gain vs. Frequency vs. V_D



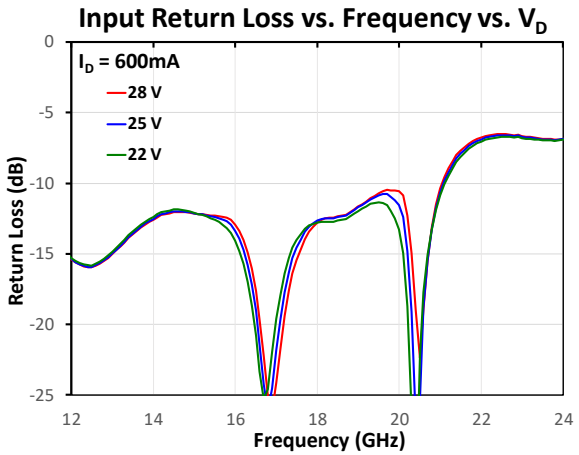
Gain vs. Frequency vs. V_D



Input Return Loss vs. Frequency vs. V_D



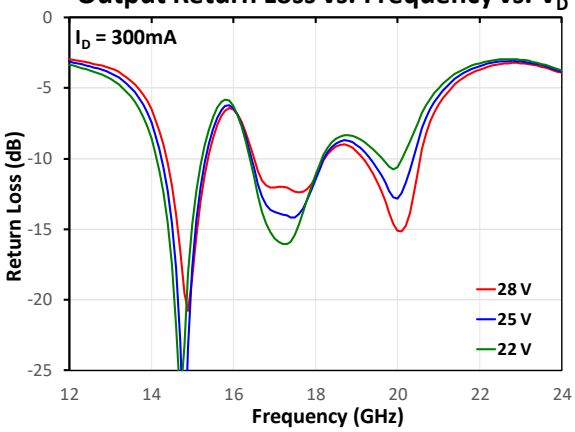
Input Return Loss vs. Frequency vs. V_D



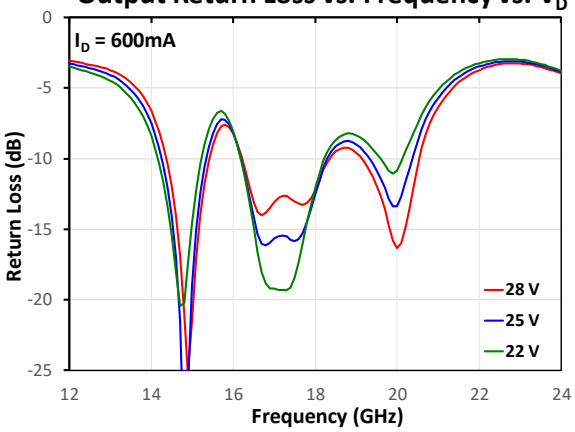
Performance Plots

Test conditions unless otherwise noted: CW, $V_{D1} = V_{D2} = V_{D3} = 28V$, $I_{D1} + I_{D2} + I_{D3} = 300mA$, adjusting $V_{G1} = V_{G2} = V_{G3}$, $T_{BASE} = +25\,°C$, $Z_0 = 50\,\Omega$

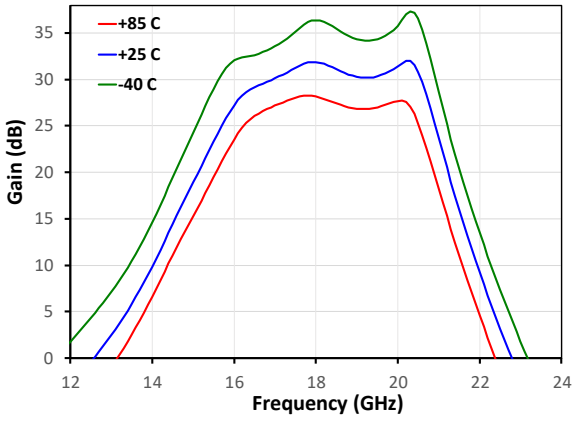
Output Return Loss vs. Frequency vs. V_D



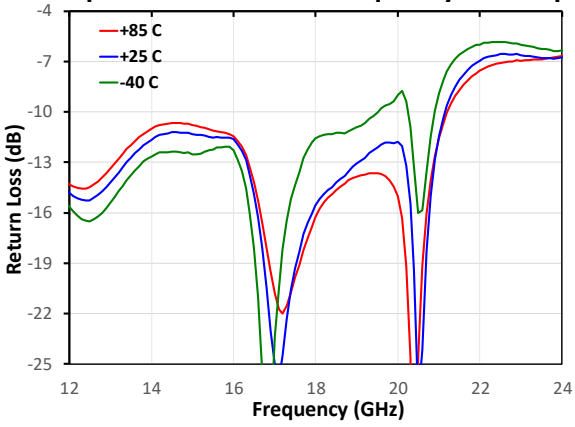
Output Return Loss vs. Frequency vs. V_D



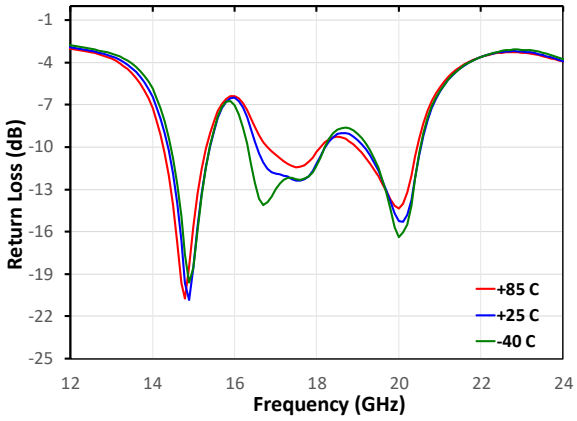
Gain vs. Frequency vs. Temp.



Input Return Loss vs. Frequency vs. Temp.



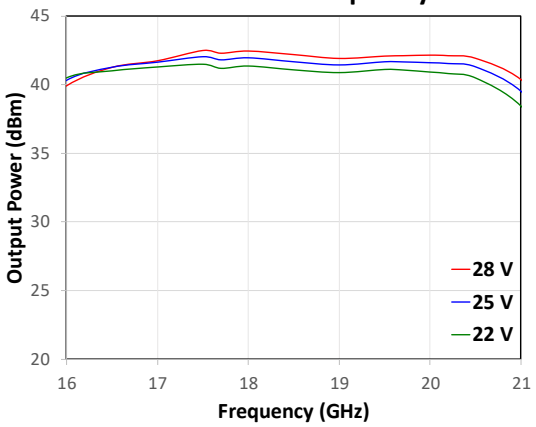
Output Return Loss vs. Frequency vs. Temp.



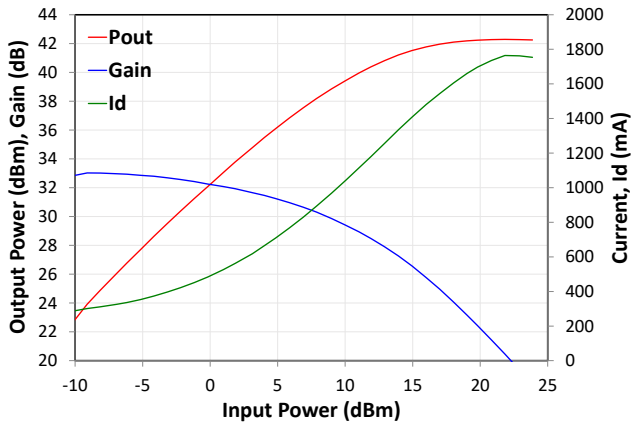
Performance Plots

Test conditions unless otherwise noted: CW, $V_{D1} = V_{D2} = V_{D3} = 28V$, $I_{D1} + I_{D2} + I_{D3} = 300mA$, adjusting $V_{G1} = V_{G2} = V_{G3}$, $P_{IN} = +22dBm$, $T_{BASE} = +25\,°C$, $Z_0 = 50\,\Omega$

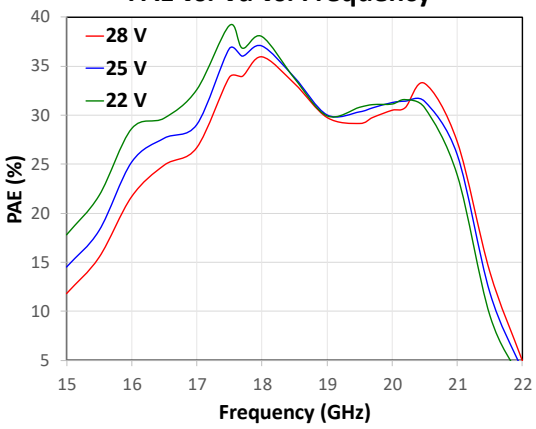
Psat vs. Vd vs. Frequency



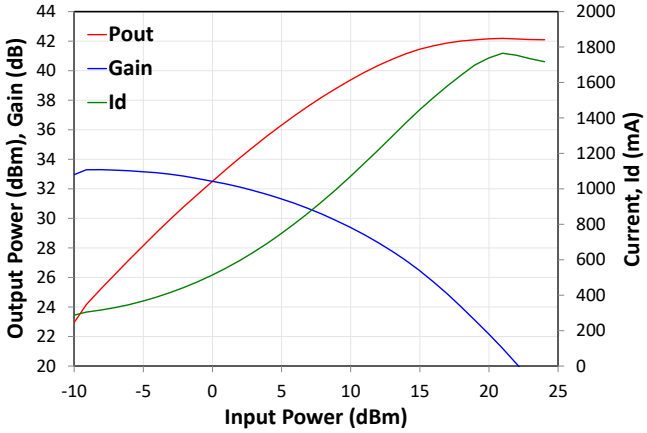
Pout, Gain, Id vs. Pin @ 17.7 GHz



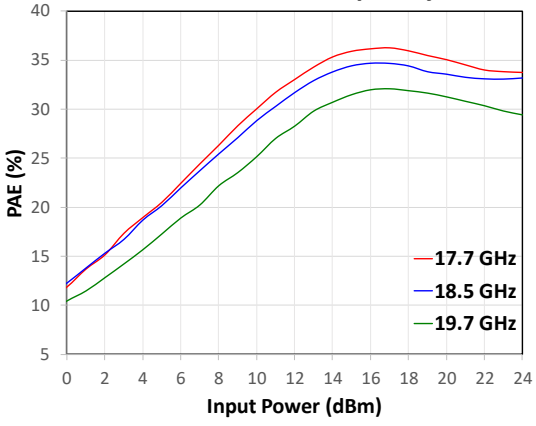
PAE vs. Vd vs. Frequency



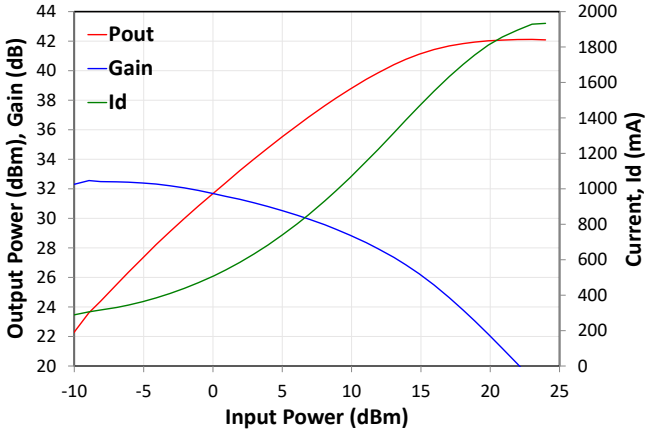
Pout, Gain, Id vs. Pin @ 18.5 GHz



PAE vs. Pin vs. Frequency

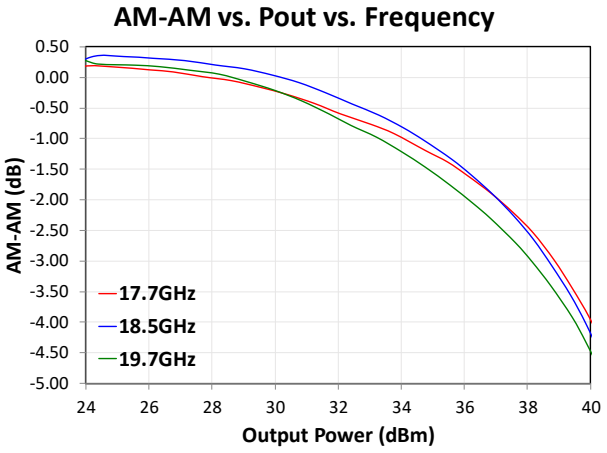


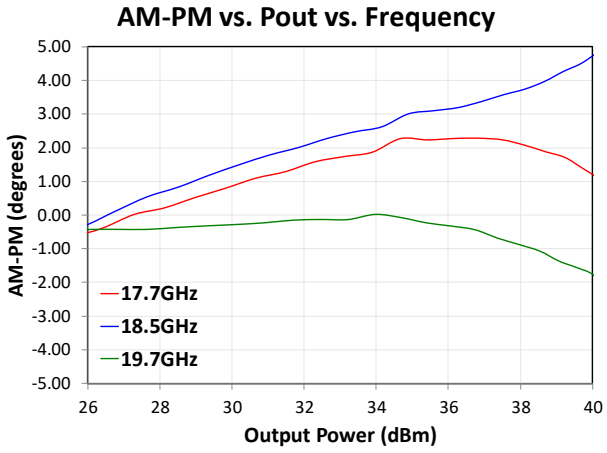
Pout, Gain, Id vs. Pin @ 19.7 GHz

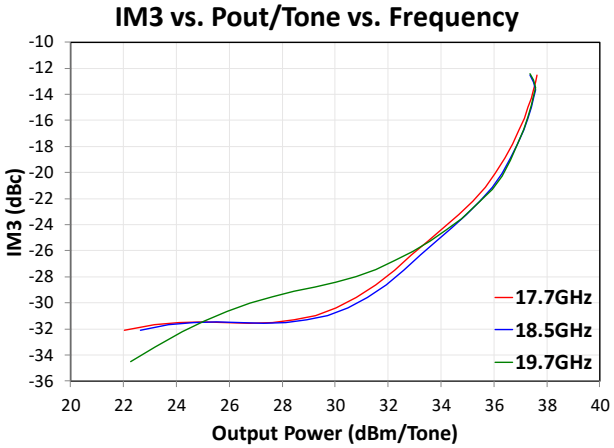


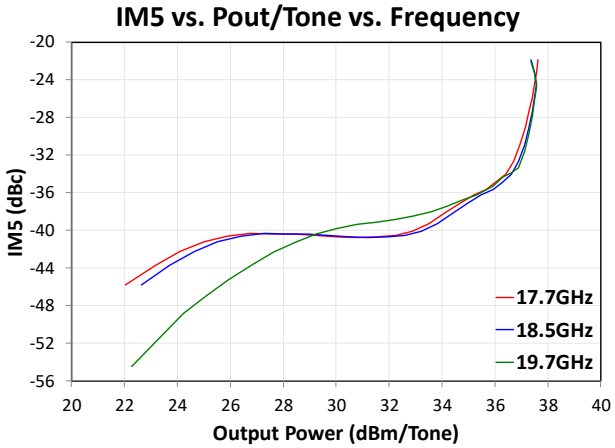
Performance Plots

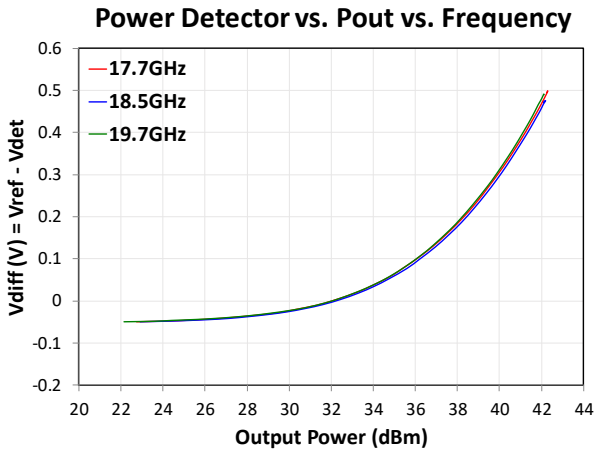
Test conditions unless otherwise noted: CW, $V_{D1} = V_{D2} = V_{D3} = 28V$, $I_{D1} + I_{D2} + I_{D3} = 300mA$, adjusting $V_{G1} = V_{G2} = V_{G3}$, $T_{BASE} = +25\,°C$, $Z_0 = 50\,\Omega$









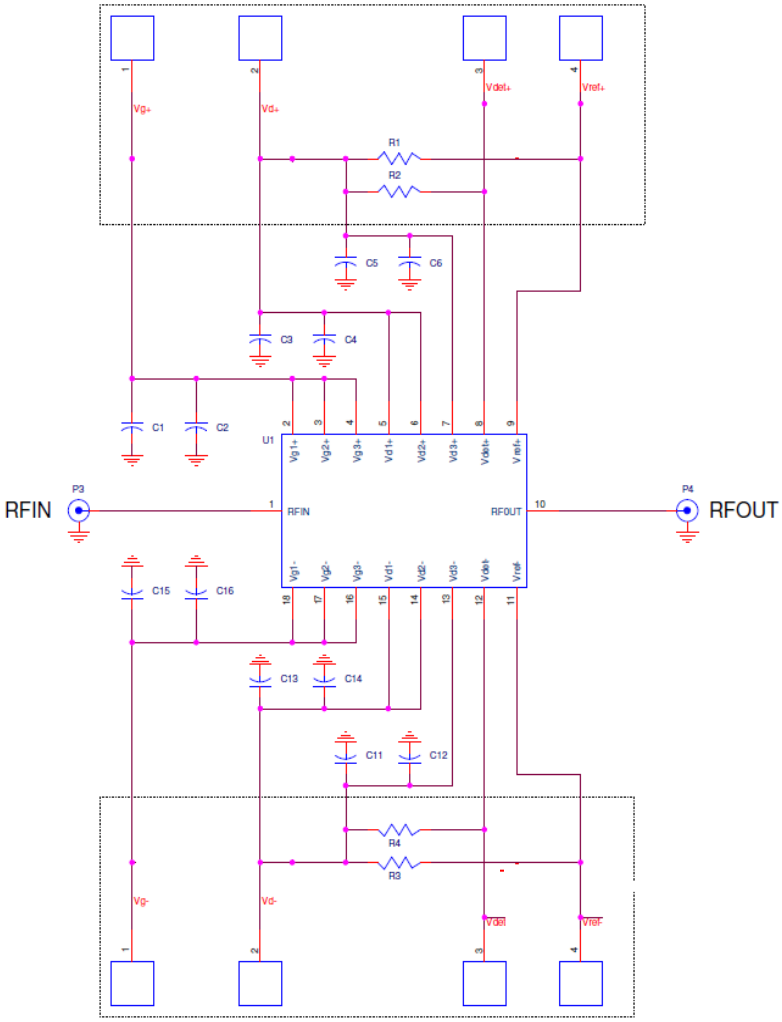


Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85 °C, V_D = 28 V, I_{DQ} = 300 mA, Freq = 20 GHz, P_{DISS} = 8.4 W	2.62	ºC/W
Channel Temperature, T_{CH} (Under RF) (2)		107	°C
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85 °C, V_D = 28 V, I_{DQ} = 300 mA, Freq = 20 GHz, I_{D_DRIVE} ≈ 1.45 A, P_{IN} = 22 dBm, P_{OUT} ≈ 40 dBm, P_{DISS} = 31 W	2.77	ºC/W
Channel Temperature, T_{CH} (Under RF) (2)		171	°C

Notes:
1. Thermal resistance determined to the back of 40 mils carrier plate, T_{BASE} = 85 °C
2. Channel temperature indicated is an IR scan equivalent temperature. Thermal resistance is calculated using this value. Additional information can be found in the Qorvo Applications Note “GaN Device TCHMAX Theta-JC and Reliability Estimates,” located here https://www.qorvo.com/products/d/da006480

Application Circuit



Notes:

1. V_{G1}, V_{G2}, and V_{G3} can be biased from either top side or bottom side; the non-biased side can be left open but bias network is required
2. V_{D1}, V_{D2}, and V_{D3} must be biased from both sides.
3. Tied all V_D's together; tied all V_G's together

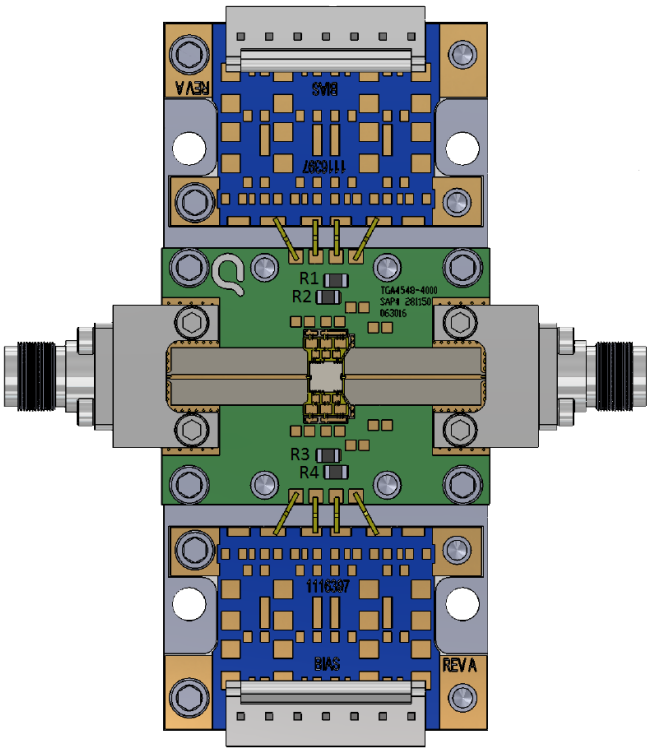
Bias Up Procedure

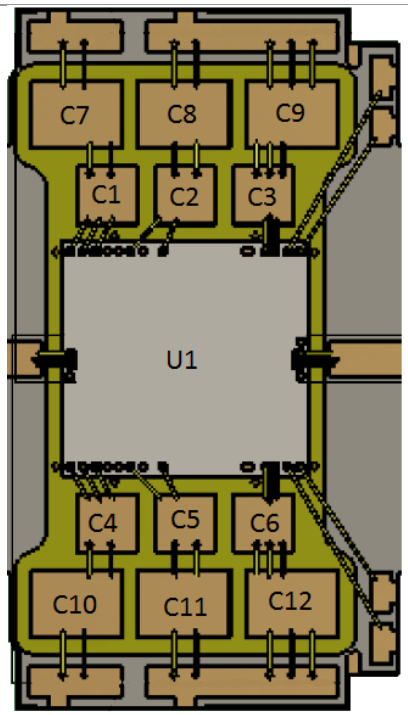
1. Set I_D limit to 3000 mA, I_G limit to 40 mA
2. Apply −5 V to V_G
3. Apply +28 V to V_D; ensure I_{DQ} is approx. 0 mA
4. Adjust V_G until I_{DQ} = 300 mA (V_G ~ −2.5 +/- 0.4 V Typ.)
5. Turn on RF supply

Bias Down Procedure

1. Turn off RF supply
2. Reduce V_G to −5 V; ensure I_{DQ} is approx. 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

Evaluation Board (EVB) Layout Assembly





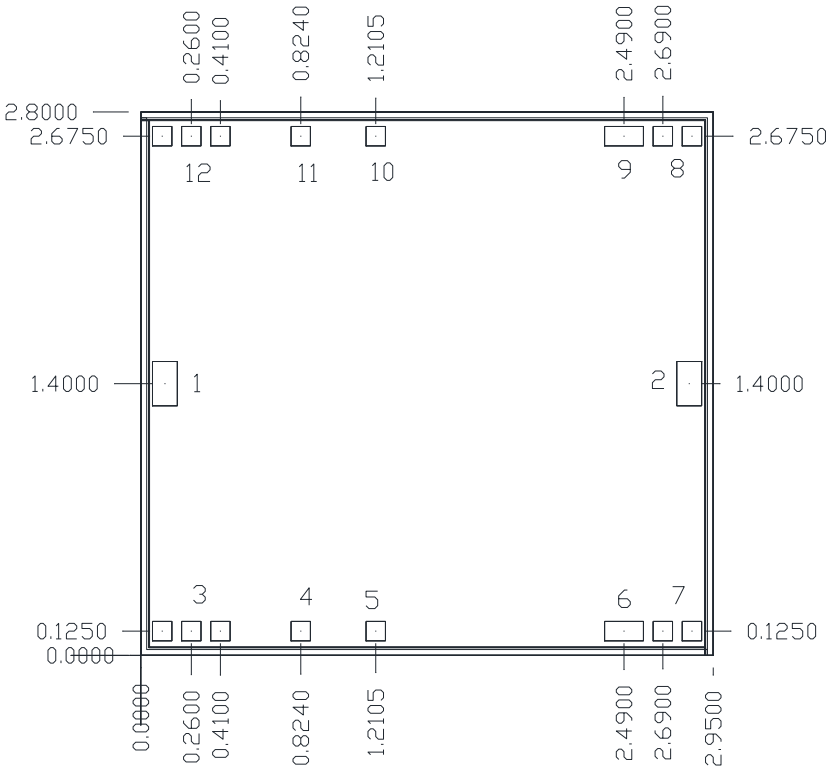
Note: PCB is a multilayer

1. All 4 metal thicknesses are 0.5 oz
2. Upper core 1 is Rogers 4003C
3. Pre-Preg is an epoxy coated glass fabric

Bill of Material – TGA4548 Evaluation board

Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	Qorvo	
U1	n/a	17 – 20 GHz Power Amplifier	Qorvo	TGA4548
C1-C6	100pF	Cap, 100pF	various	
C7-C12	0.01uF	Cap, 0.01uF	various	
R1-R4	20kΩ	Res 20K OHM 1/8W +/-1% 0805 NON-ROHS	various	

Mechanical Information



Notes:
Units: millimeters
Ground is backside of die

Bond Pad Description

Pad No.	Symbol	Pad Size (mm)	Description
1	RF IN	0.100 x 0.200	RF Input; matched to 50 Ω, DC blocked
3, 12	V_{G123}	0.100 x 0.100	Gate voltage for stage 1, 2, & 3, bias network is required; see Application Circuit on page 8 as an example.
4, 11	V_{D1}	0.100 x 0.100	Drain voltage for stage 1, bias network is required; see Application Circuit on page 8 as an example.
5, 10	V_{D2}	0.100 x 0.100	Drain voltage for stage 2, bias network is required; see Application Circuit on page 8 as an example.
6, 9	V_{D3}	0.200 x 0.100	Drain voltage for stage 3, bias network is required; see Application Circuit on page 8 as an example.
7, 8	V_{DET}, V_{REF}	0.100 x 0.100	Power detector and reference voltage
2	RF OUT	0.100 x 0.200	RF Output; matched to 50 Ω, DC blocked

Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment (i.e. epoxy) can be used in low-power applications and for die attach to soft substrates.
- Curing should be done in a convection oven; proper exhaust is a safety concern.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300 °C to 3 – 4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1A	ANSI/ESD/JEDEC JS-001
ESD – Charged Device Model (CDM)	C2	ANSI/ESD/JEDEC JS-002

Caution!
ESD-Sensitive Device

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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