TGA2239-CP

13.4 – 15.5 GHz 50 W GaN Power Amplifier

Product Description

Qorvo's TGA2239-CP is a 3-stage, 50 W power amplifier operating over the 13.4 to 15.5 GHz band. Fabricated on Qorvo's production 0.15 um GaN on SiC technology, this high performance amplifier offers greater than 30 dB small-signal gain and greater than 31 % power-added efficiency, allowing the system designer to achieve superior performance levels in a cost efficient manner.

The TGA2239-CP is offered in a 10-lead 15 x 15 mm bolt-down package. Assembled with a pure-copper base, coupled with its high efficiency, the TGA2239-CP minimizes the strain on the system-level cooling requirements, further reducing system operating costs. Superior electrical performance and thermal management makes the TGA2239-CP ideal for supporting communications and radar applications in both commercial and military markets.

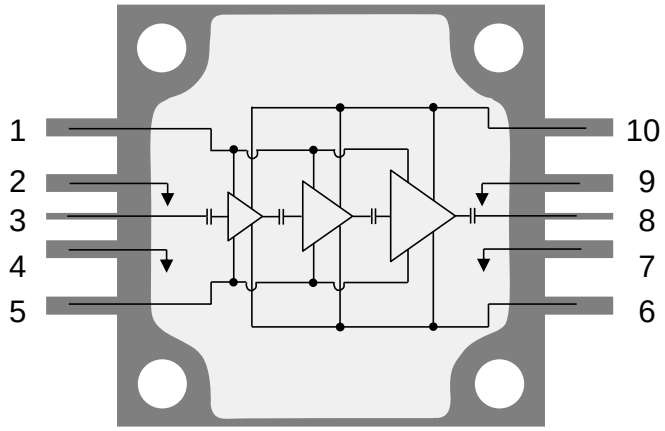
Both RF ports have integrated DC blocking capacitors and are fully matched to 50 Ohms.

RoHS compliant.

Product Features

- Frequency Range: 13.4 – 15.5 GHz
- P_{OUT}: >45.5 dBm (P_{IN} = 22 dBm)
- PAE: > 31 % (P_{IN} = 22 dBm)
- Small Signal Gain: > 30 dB
- IM3: < −19 dBc @ 38 dBm P_{OUT} / Tone
- Bias: V_D = +28 V, I_{DQ} = 900 mA, V_G = −2.7 V Typical
- Package Dimensions: 15.2 x 15.2 x 3.5 mm
- Process Technology: QGaN15
- Package base is pure Cu offering superior thermal management

Functional Block Diagram



Applications

- Commercial VSAT
- Military Satcom
- Datalinks
- Radar

Ordering Information

Part No.	Description
TGA2239-CP	13.4 – 15.5 GHz 50 W GaN Power Amplifier (10 pieces)
TGA2239-CPEVB01	TGA2239-CP Evaluation Board

Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage (V_D)	+29.5 V
Gate Voltage Range (V_G)	−5 to 0 V
Drain Current (I_D)	7.2 A
Forward Gate Current (I_G)	See plot on page 3
Power Dissipation (P_{DISS}), 85 °C	140 W
Input Power (P_{IN}), CW, 50 Ω, V_D = +28 V, 85 °C	33 dBm
Input Power (P_{IN}), CW, 3:1 VSWR, V_D = +28 V, 85 °C	30 dBm
Mounting Temperature	Refer to Assembly Notes, page 13
Storage Temperature	−55 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating

Parameter	Value / Range
Drain Voltage (V_D)	+28 V
Drain Current (I_{DQ})	900 mA
Drain Current Under RF Drive (I_{D_DRIVE})	See plots p. 7
Gate Current Under RF Drive (I_{G_DRIVE})	See plots p. 7
Temperature (T_{BASE})	−40 to 85 °C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter		Min	Typ	Max	Units
Operational Frequency Range		13.4	–	15.5	GHz
Small Signal Gain		–	> 30	–	dB
Input Return Loss		–	> 14	–	dB
Output Return Loss		–	> 9	–	dB
Output Power (P_{IN} = 22 dBm)	13.0 GHz 14.5 GHz 15.5 GHz	46 46 45	46.5 47 47	–	dBm
Power Added Efficiency (P_{IN} = 22 dBm)	13.0 GHz 14.5 GHz 15.5 GHz	25 25 30	30 32 33	–	%
IM3 (P_{OUT} / Tone = 38 dBm / Tone, 1 MHz Spacing)		–	< −19	–	dBc
IM5 (P_{OUT} / Tone = 38 dBm / Tone, 1 MHz Spacing)		–	< −30	–	dBc
Small Signal Gain Temperature Coefficient		–	−0.09	–	dB/°C
Output Power Temperature Coefficient (P_{IN} = 22 dBm) (From 25 °C to 85 °C)		–	−0.014	–	dBm/°C
Recommended Operating Voltage		–	+28	+28	V

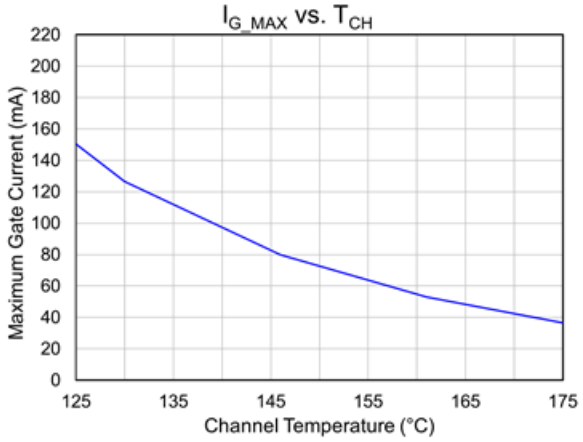
Test conditions unless otherwise noted: 25 °C, V_D = +28 V, I_{DQ} = 900 mA, CW operation

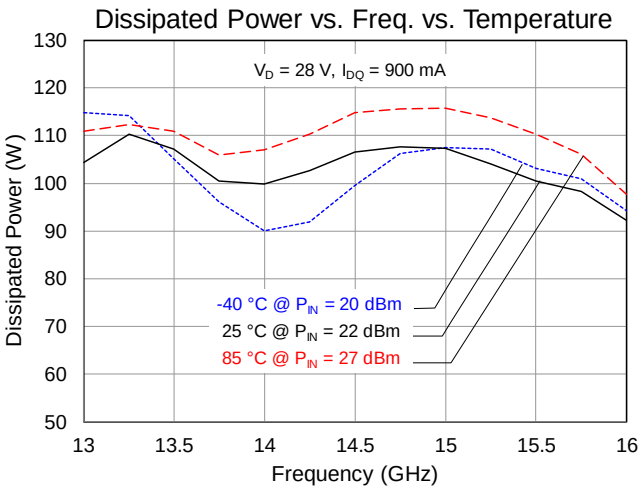
Thermal and Reliability Information

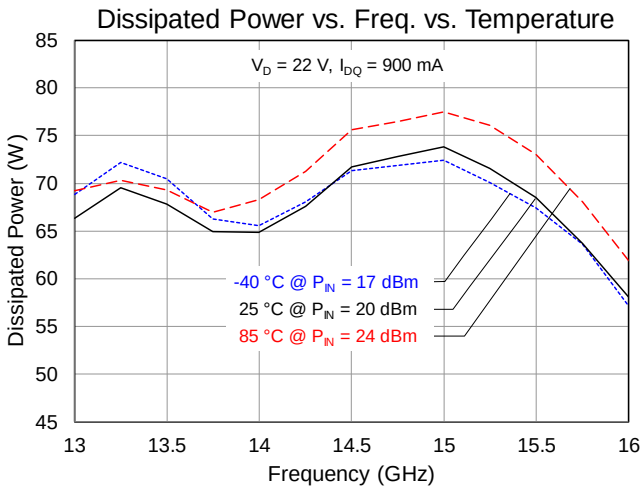
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85°C, V_D = +28 V (CW)	0.52	°C/W
Channel Temperature (T_{CH}) (Quiescent)	At I_{DQ} = 900 mA, P_{DISS} = 25.2 W	98	°C
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85 °C, V_D = +22 V (CW)	0.79	°C/W
Channel Temperature (T_{CH}) (Under RF drive)	At Freq = 15 GHz, P_{IN} = 24 dBm: I_{DQ} = 900 mA, I_{D_Drive} = 5.1 A P_{OUT} = 45.4 dBm, P_{DISS} = 77 W	146	°C
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85 °C, V_D = +28 V (CW)	0.79	°C/W
Channel Temperature (T_{CH}) (Under RF drive)	At Freq = 15 GHz, P_{IN} = 27 dBm: I_{DQ} = 900 mA, I_{D_Drive} = 5.8 A P_{OUT} = 46.7 dBm, P_{DISS} = 116 W	177	°C

Notes:
1. Thermal resistance measured to back of package.
2. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

Dissipated Power



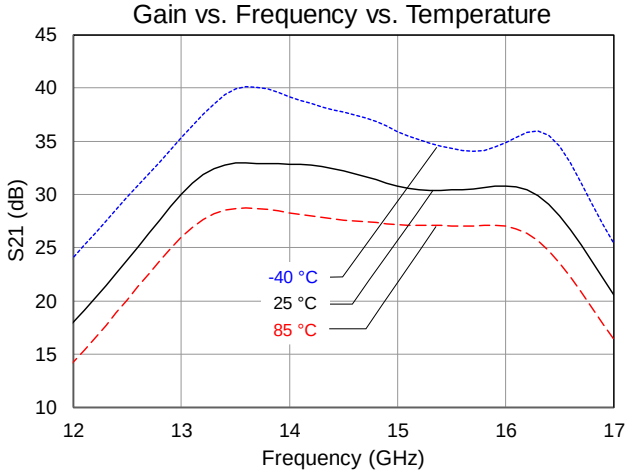




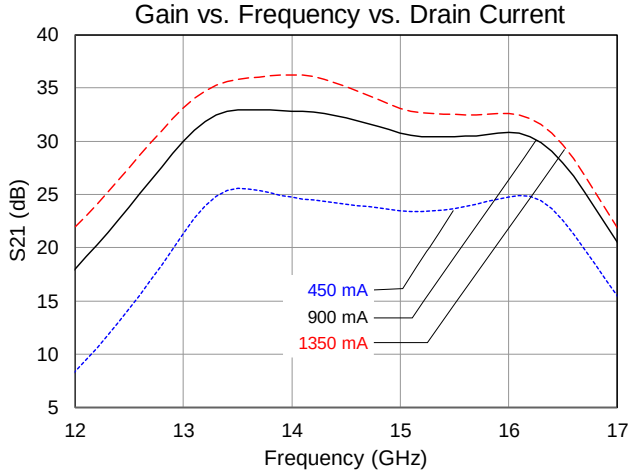
Performance Plots – Small Signal

Conditions unless otherwise specified: V_D = +28 V, I_{DQ} = 900 mA, Temp. = 25 °C, CW operation

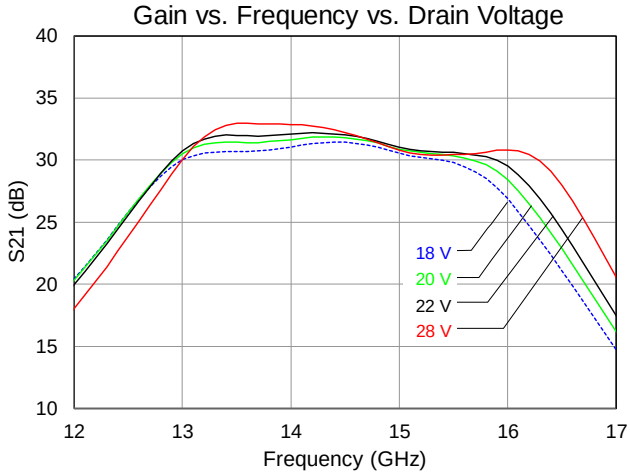
Gain vs. Frequency vs. Temperature



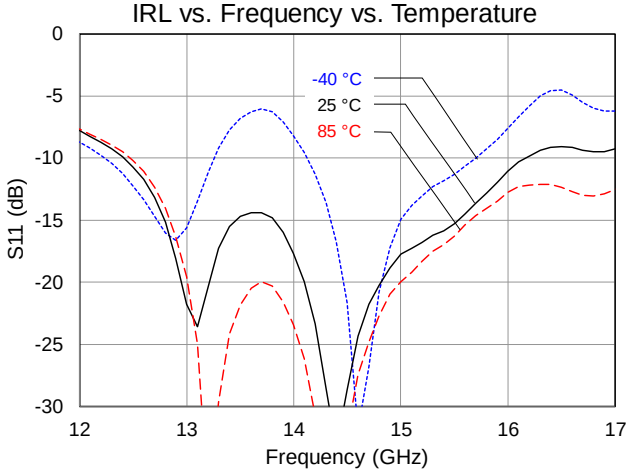
Gain vs. Frequency vs. Drain Current



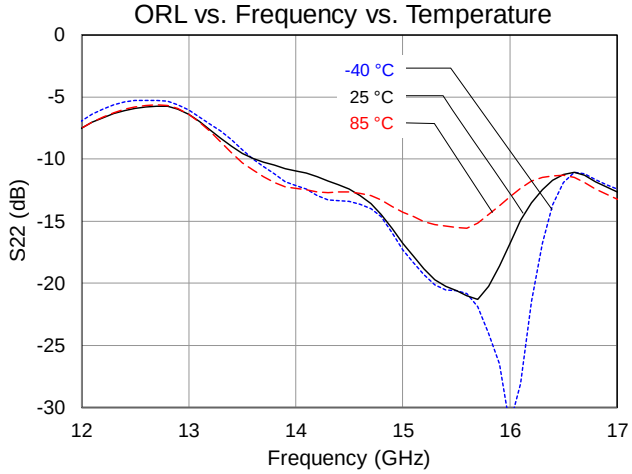
Gain vs. Frequency vs. Drain Voltage



IRL vs. Frequency vs. Temperature



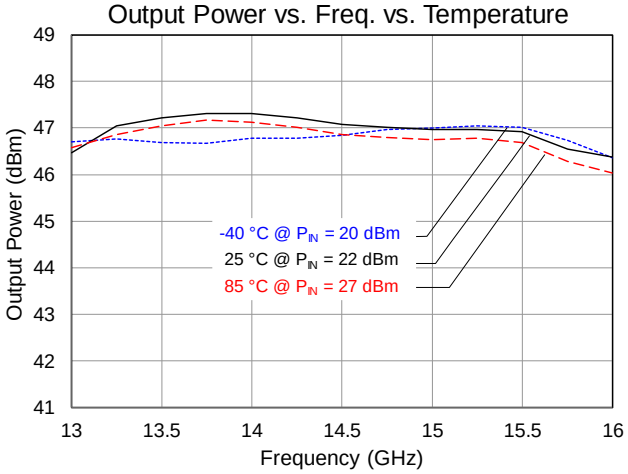
ORL vs. Frequency vs. Temperature



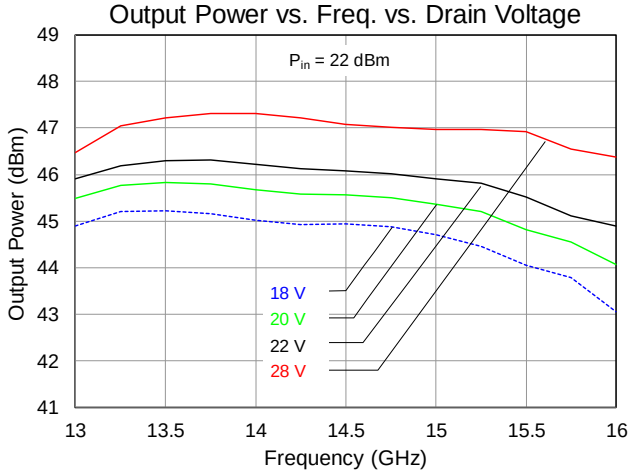
Performance Plots – Large Signal

Conditions unless otherwise specified: V_D = +28 V, I_{DQ} = 900 mA, Temp. = 25 °C, CW operation

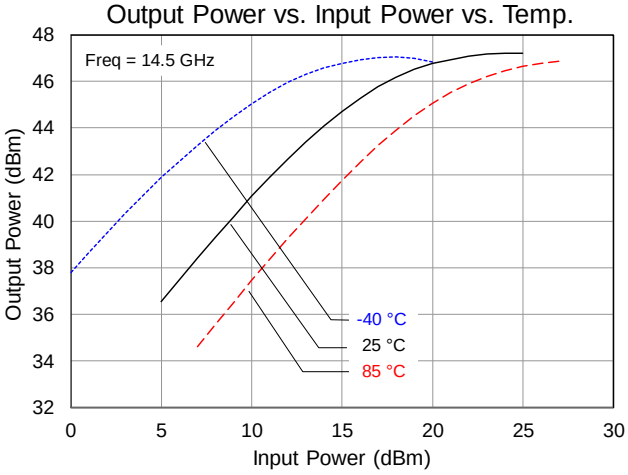
Output Power vs. Freq. vs. Temperature



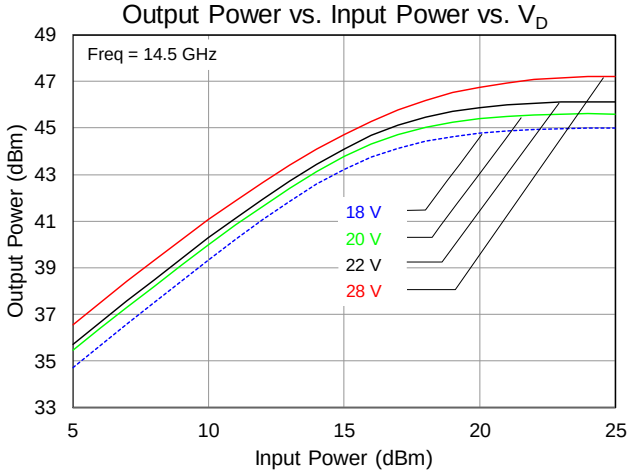
Output Power vs. Freq. vs. Drain Voltage



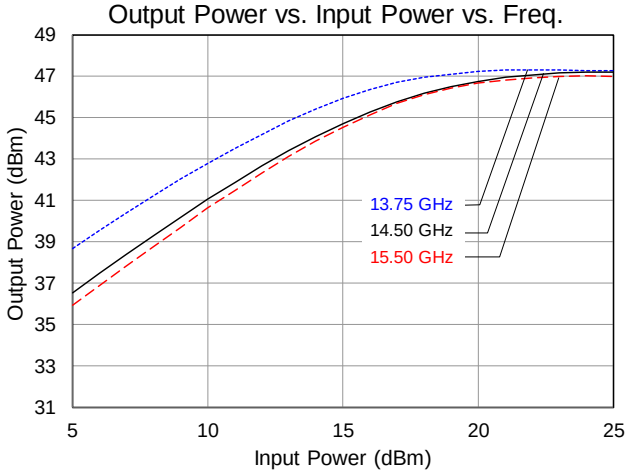
Output Power vs. Input Power vs. Temp.



Output Power vs. Input Power vs. V_D



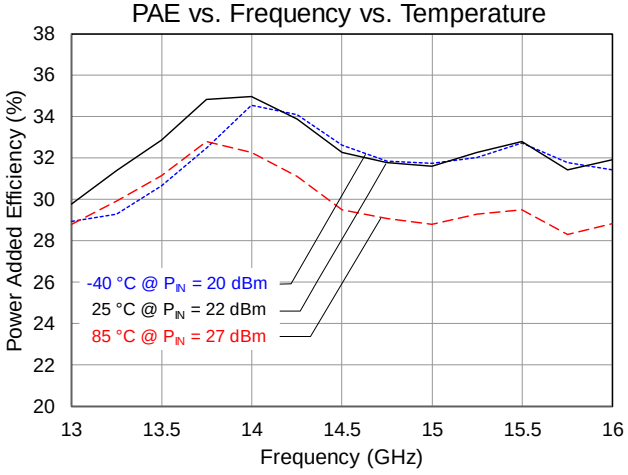
Output Power vs. Input Power vs. Freq.



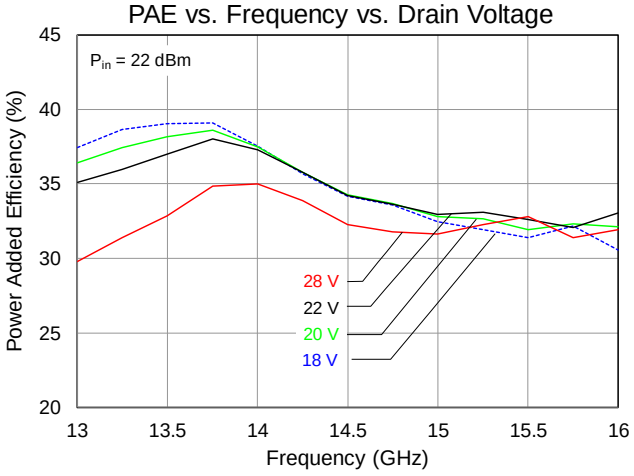
Performance Plots – Large Signal

Conditions unless otherwise specified: V_D = +28 V, I_{DQ} = 900 mA, Temp. = 25 °C, CW operation

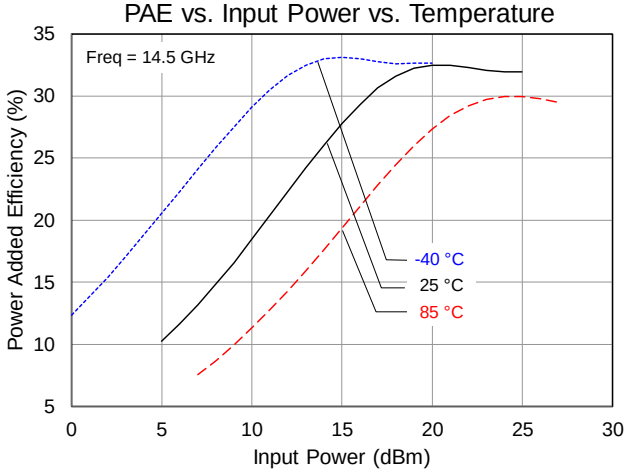
PAE vs. Frequency vs. Temperature



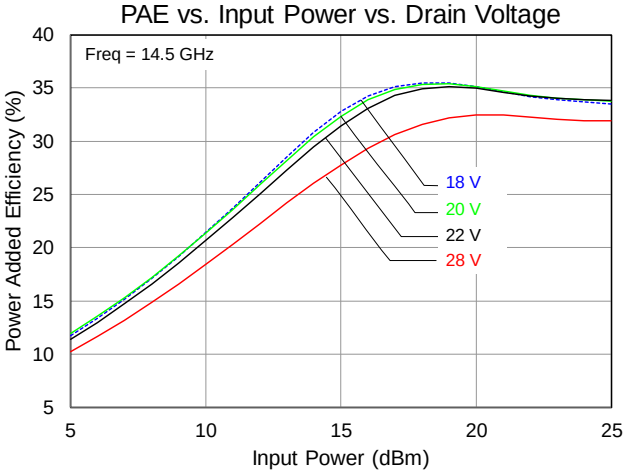
PAE vs. Frequency vs. Drain Voltage



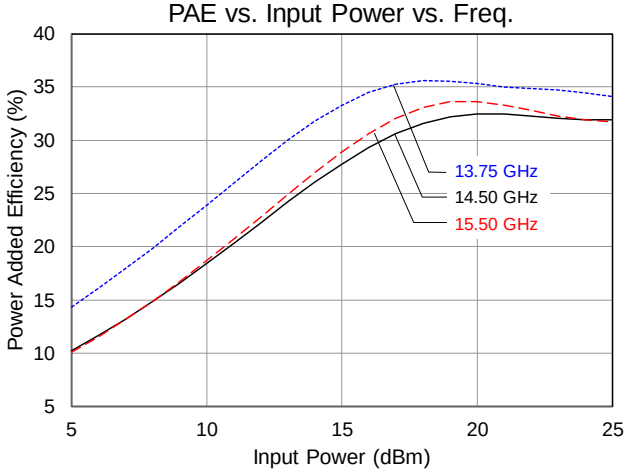
PAE vs. Input Power vs. Temperature



PAE vs. Input Power vs. Drain Voltage



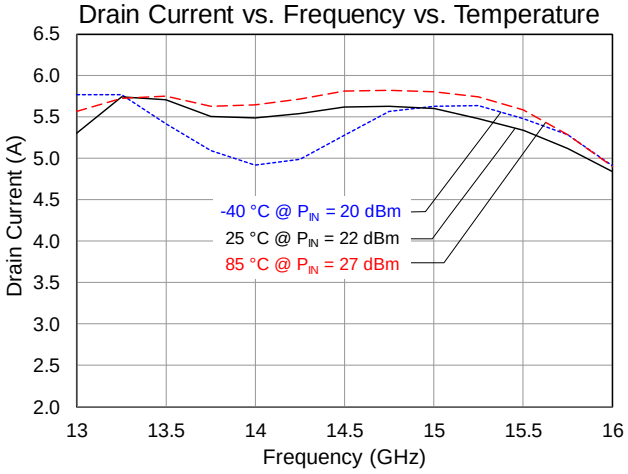
PAE vs. Input Power vs. Freq.



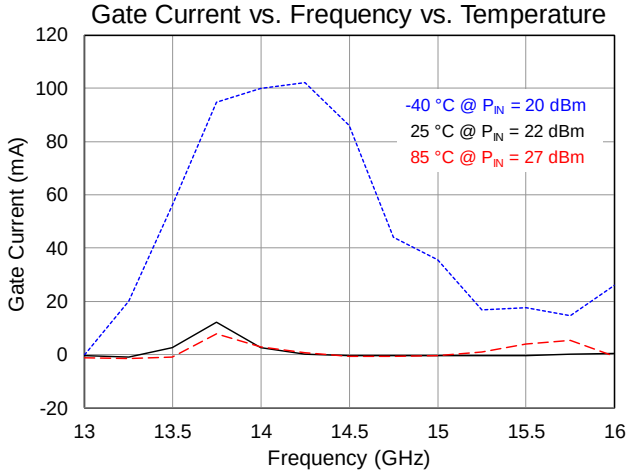
Performance Plots – Large Signal

Conditions unless otherwise specified: V_D = +28 V, I_{DQ} = 900 mA, Temp. = 25 °C, CW operation

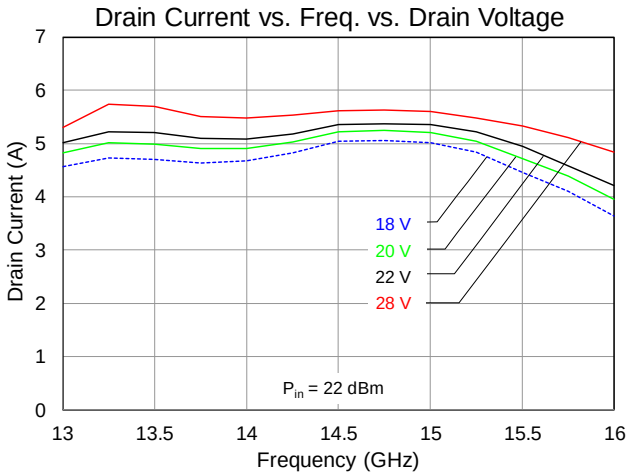
Drain Current vs. Frequency vs. Temperature



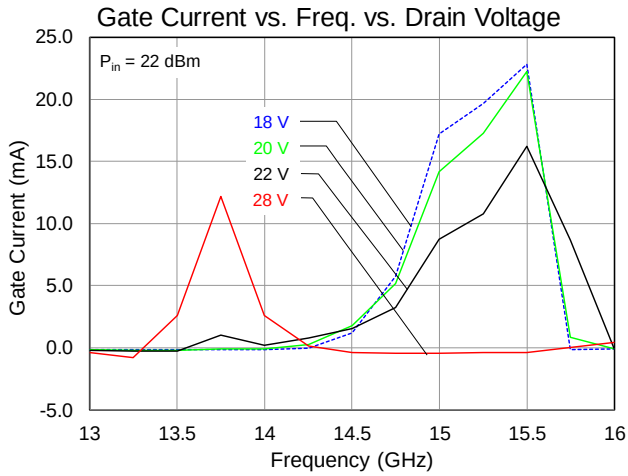
Gate Current vs. Frequency vs. Temperature



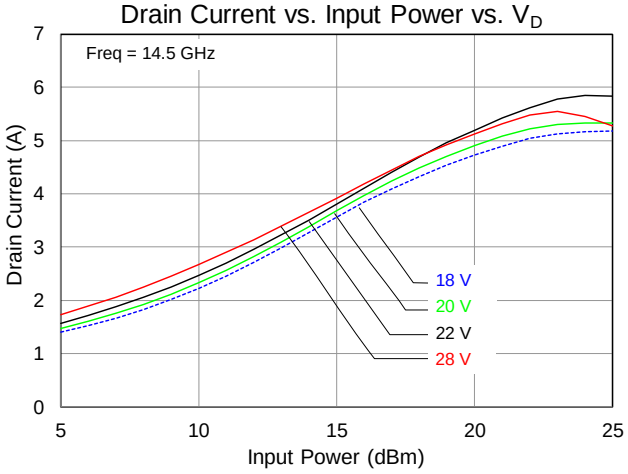
Drain Current vs. Freq. vs. Drain Voltage



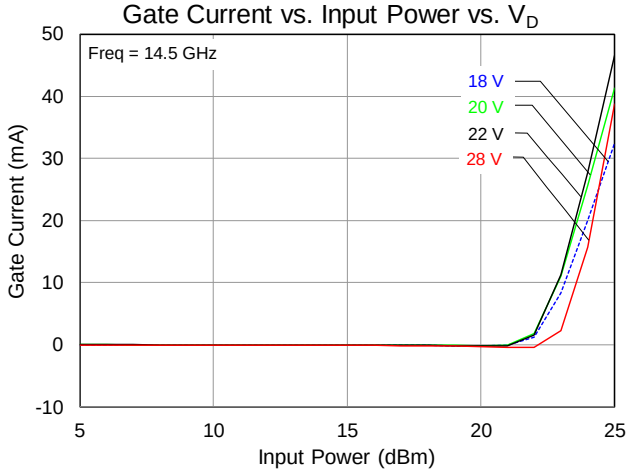
Gate Current vs. Freq. vs. Drain Voltage



Drain Current vs. Input Power vs. V_D



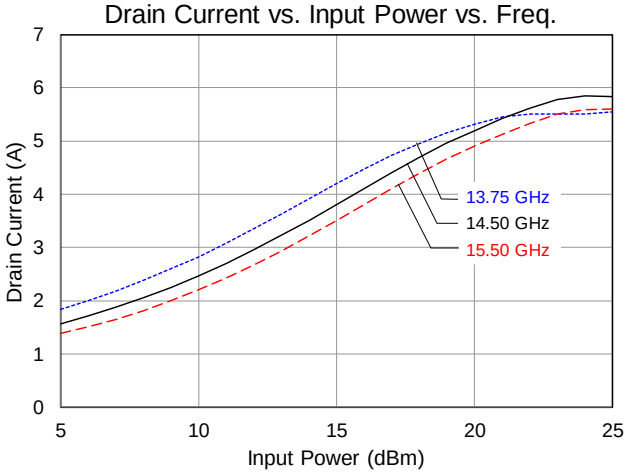
Gate Current vs. Input Power vs. V_D



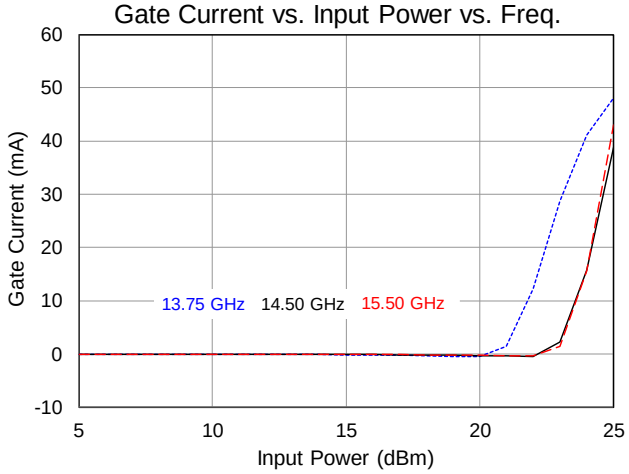
Performance Plots – Large Signal

Conditions unless otherwise specified: V_D = +28 V, I_{DQ} = 900 mA, Temp. = 25 °C, CW operation

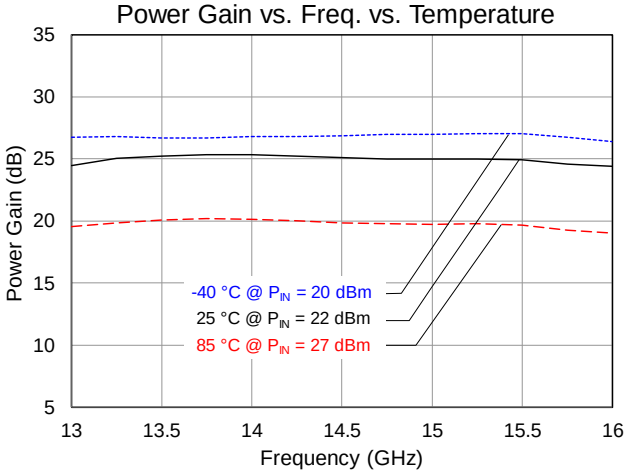
Drain Current vs. Input Power vs. Freq.



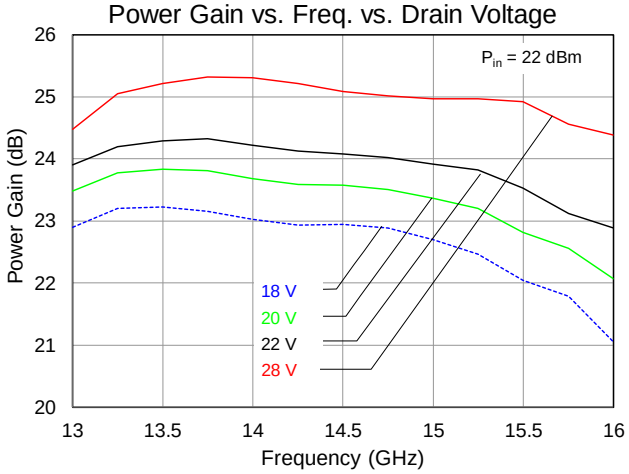
Gate Current vs. Input Power vs. Freq.



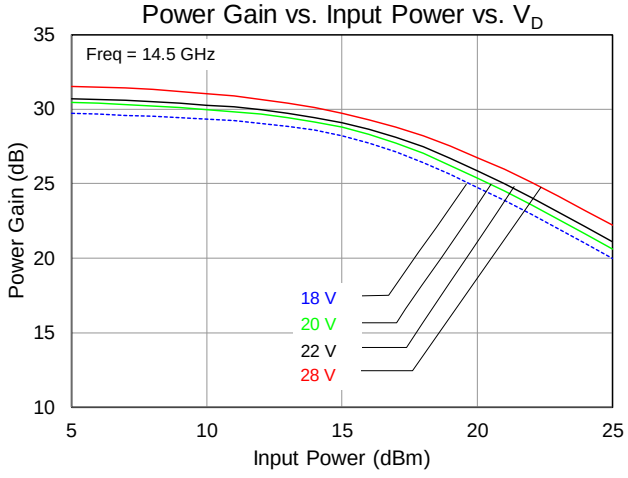
Power Gain vs. Freq. vs. Temperature



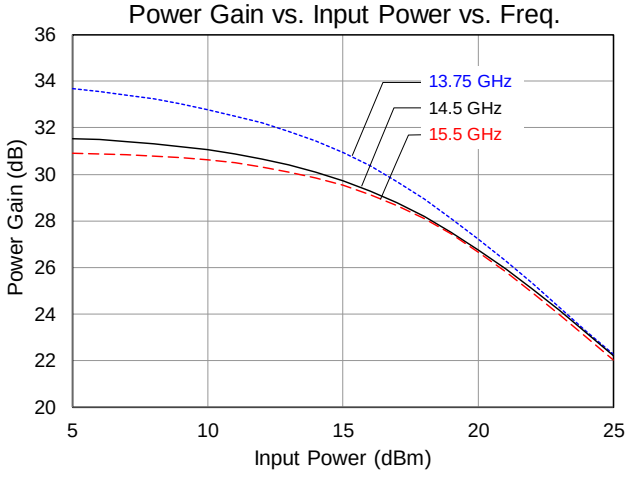
Power Gain vs. Freq. vs. Drain Voltage



Power Gain vs. Input Power vs. V_D



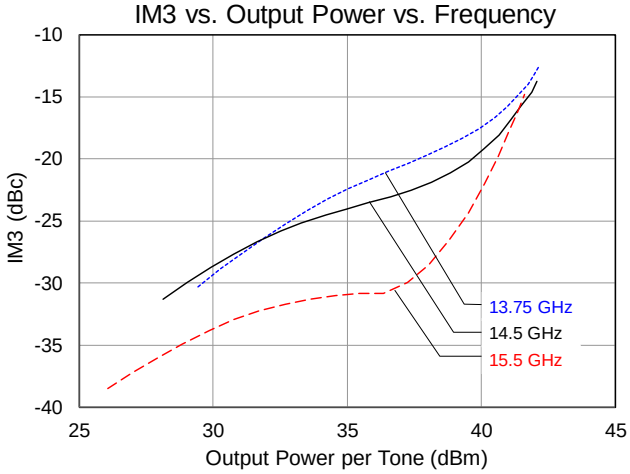
Power Gain vs. Input Power vs. Freq.



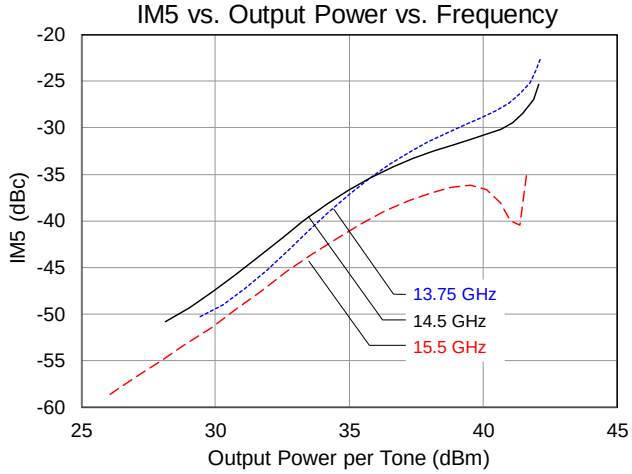
Performance Plots – Linearity

Conditions unless otherwise specified: V_D = +28 V, I_{DQ} = 900 mA, Temp. = 25 °C, CW operation, Input Tone Spacing = 1 MHz

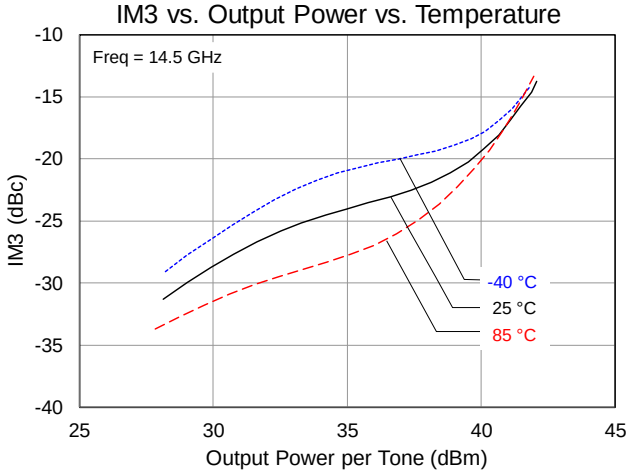
IM3 vs. Output Power vs. Frequency



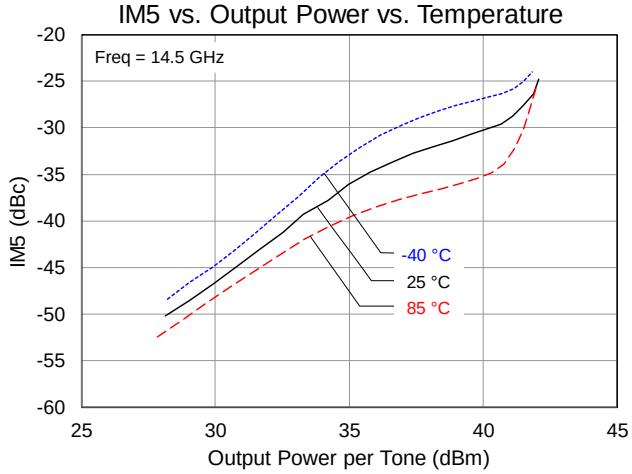
IM5 vs. Output Power vs. Frequency



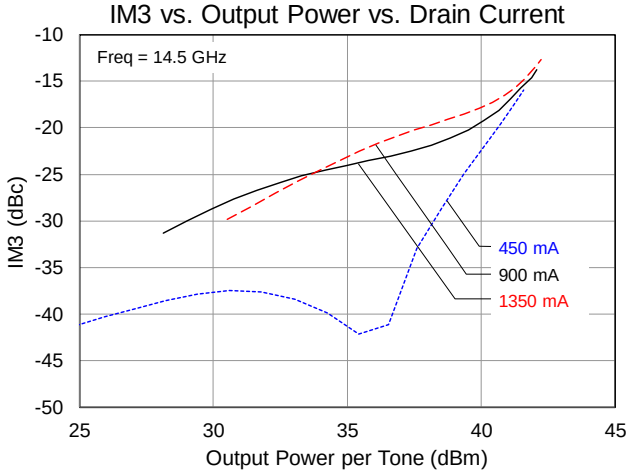
IM3 vs. Output Power vs. Temperature



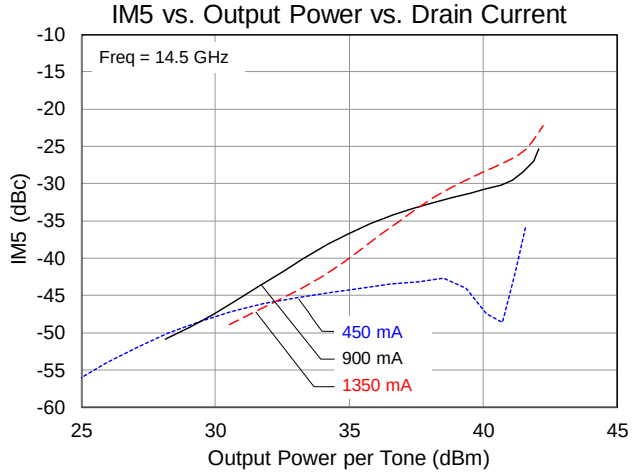
IM5 vs. Output Power vs. Temperature



IM3 vs. Output Power vs. Drain Current



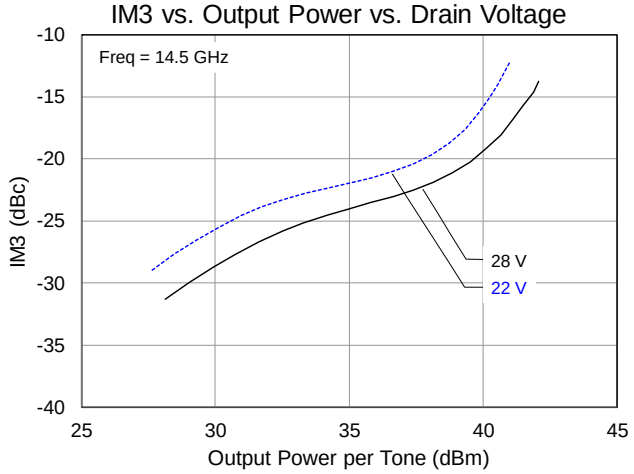
IM5 vs. Output Power vs. Drain Current



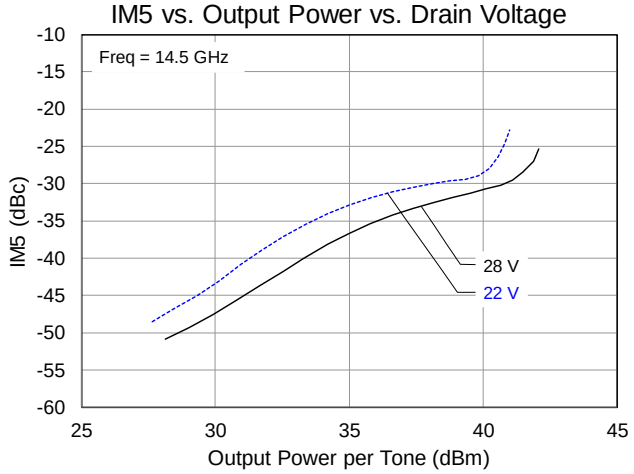
Performance Plots – Linearity

Conditions unless otherwise specified: V_D = +28 V, I_{DQ} = 900 mA, Temp. = 25 °C, CW operation, Input Tone Spacing = 1 MHz

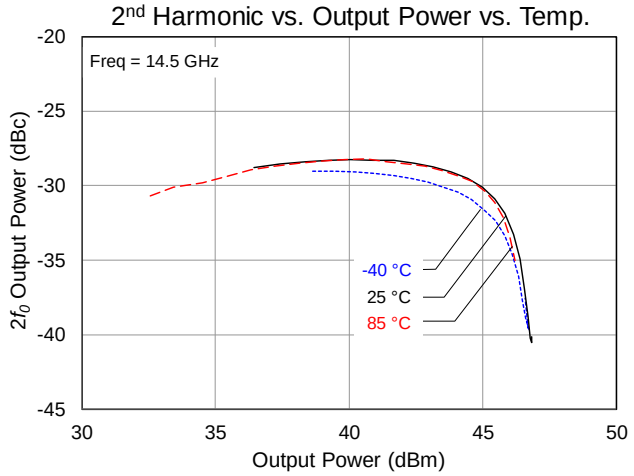
IM3 vs. Output Power vs. Drain Voltage



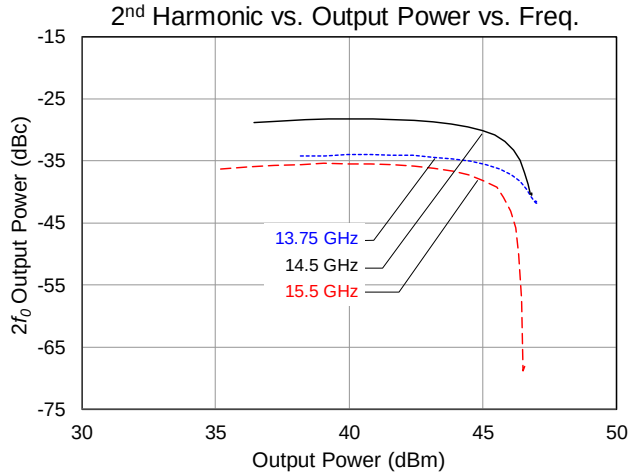
IM5 vs. Output Power vs. Drain Voltage



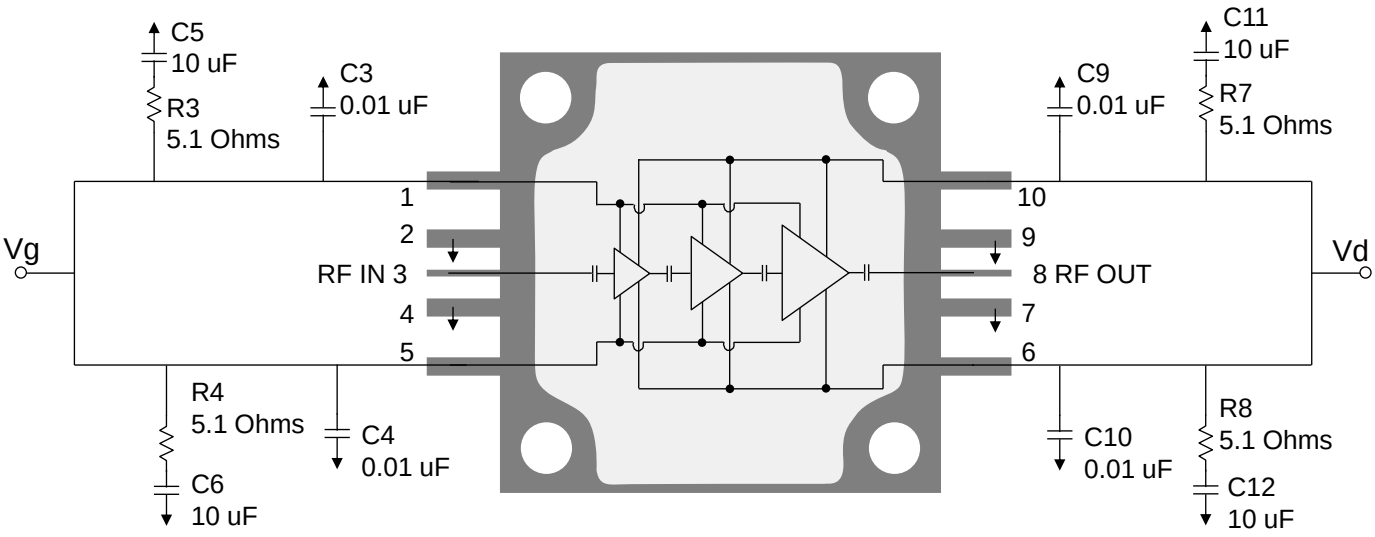
2nd Harmonic vs. Output Power vs. Temp.



2nd Harmonic vs. Output Power vs. Freq.



Applications Information and Pad Layout



Bias Up Procedure

1. Set I_D limit to 6.3 A, I_G limit to 110 mA
2. Apply −5 V to V_G
3. Apply +28 V to V_D; ensure I_{DQ} is approx. 0 mA
4. Adjust V_G until I_{DQ} = 900 mA (V_G ~ −2.7 V Typ.).
5. Turn on RF supply

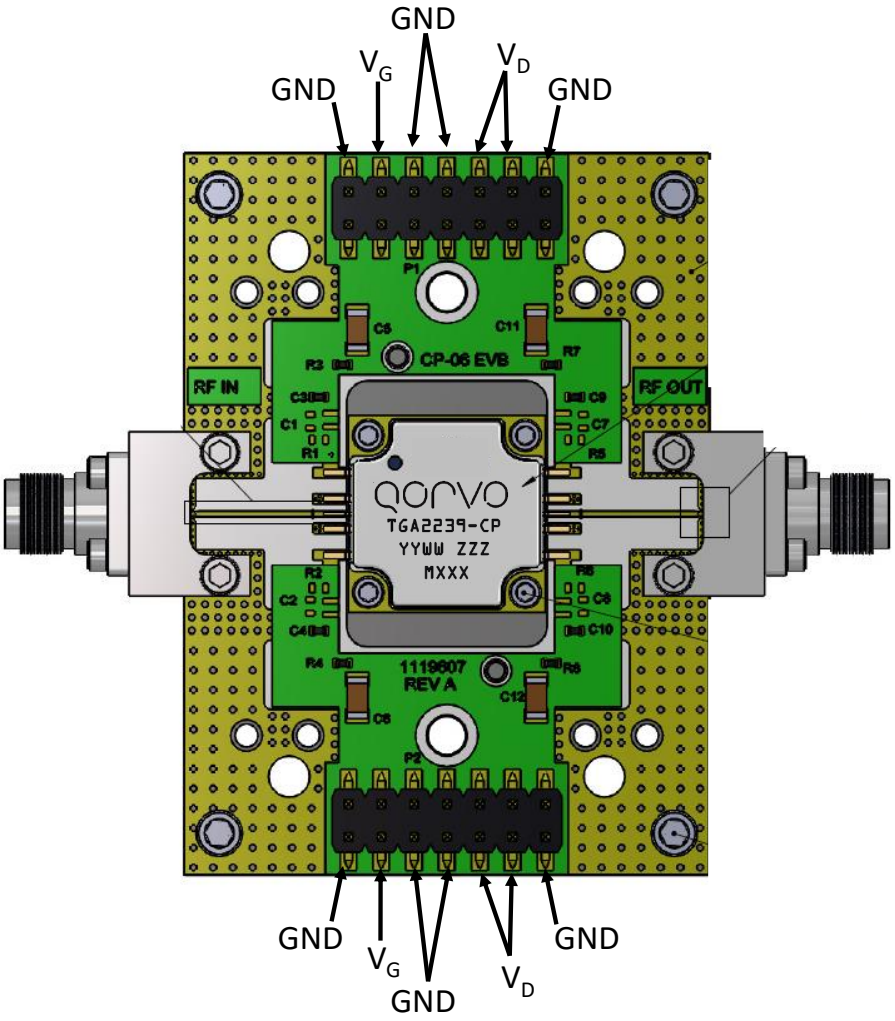
Bias Down Procedure

1. Turn off RF supply
2. Reduce V_G to −5 V; ensure I_{DQ} is approx. 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

Pin Description

Pad No.	Symbol	Description
1,5	V_G	Gate Voltage; Bias network is required; must be biased from both sides; see recommended Application Information above.
3	RF_{IN}	Input; matched to 50 Ω; DC blocked
2,4,7,9	GND	Must be grounded on the PCB.
6,10	V_D	Drain voltage; Bias network is required; must be biased from both sides; see recommended Application Information above.
8	RF_{OUT}	Output; matched to 50 Ω; DC blocked

Evaluation Board



Notes:

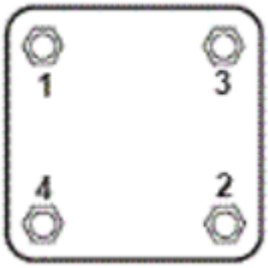
1. Both Top and Bottom Vd and Vg must be biased.

Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C3, C4, C9, C10	0.01 µF	Cap, 0402, 50 V, 10 %, X7R	Various	–
C5, C6, C11, C12	10 µF	Cap, 1206, 50 V, 20 %, X5R	Various	–
R3, R4, R7, R8	5.1 Ohm	Res, 0402, 50 V, 5 %	Various	–

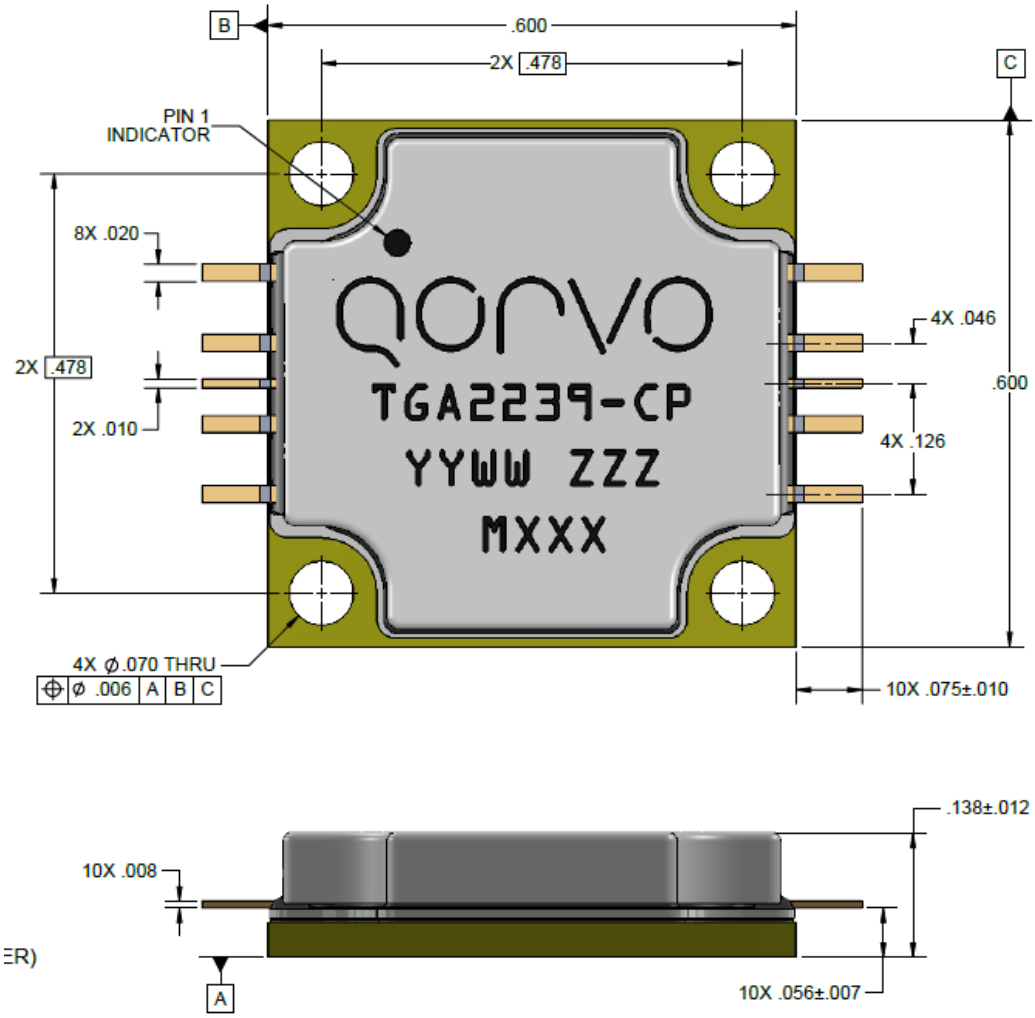
Assembly Notes

1. Carefully clean the PC board and package leads with alcohol. Allow it to dry fully.
2. To improve the thermal and RF performance, Qorvo recommends attaching a heat sink to the bottom of the PCB and apply thermal compound (Arctic Silver 5 recommended) or 4 mil indium shim between the heat sink and the package.
3. (The following is for *information only*. There are many variables in a second level assembly that Qorvo does not control, so Qorvo does not recommend an absolute torque value.) Use screws to attach the component to the heat sink. A suggested torque value is 16 in-oz. for a 0-80 screw. Start with screws finger tight, then torque to 8 in-oz., then torque to final value. Use the following tightening pattern:



4. The component leads should be manually soldered. Apply a low residue solder alloy meeting J-STD-001 (ROL0, ROL1 or equivalent) with a liquidus temperature below 220 C to each pin of the TGA2239-CP. The use of low residue/no-clean flux (ROL0, ROL1) is recommended. Adding flux during hand soldering of the component leads with localized spot cleaning is acceptable. Soldering irons meeting the requirements of J-STD-001, Appendix A are acceptable. The packaged part should not be subjected to conventional SMT automated solder reflow processes.

Mechanical Information



Units: inches
Tolerances: unless specified
x.xx = ± 0.01
x.xxx = ± 0.005
Materials:
Base: Copper
Lid: Plastic
All metalized features are gold plated
Part is epoxy sealed
Marking:
2239: Part number
YY: Part Assembly year
WW: Part Assembly week
ZZZ: Serial Number
MXXX: Batch ID

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B	JEDEC Standard JESD22 A114
MSL – Moisture Sensitivity Level	N/A	

Caution!
ESD-Sensitive Device

Solderability

The component leads should be manually soldered, and the package cannot be subjected to conventional reflow processes. The use of no-clean solder to avoid washing after soldering is recommended.

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU. This product also has the following attributes:

- Product uses RoHS Exemption 7c-1 to meet RoHS Compliance requirements
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_40_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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