10-16GHz Low Noise Amplifier

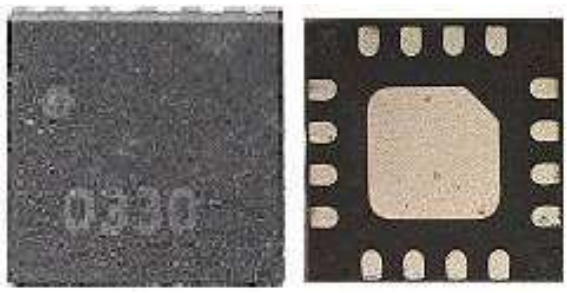
GaAs Monolithic Microwave IC in SMD leadless package

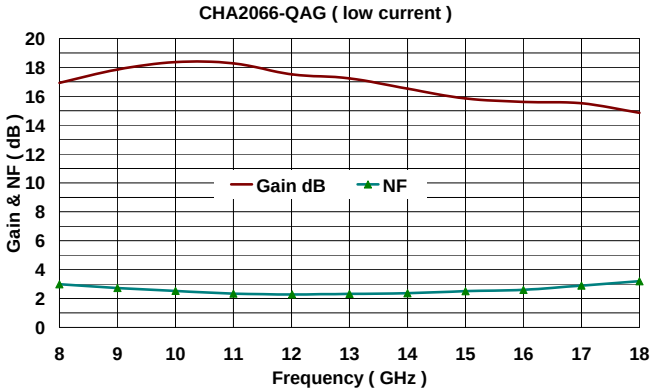
Description

The CHA2066-QAG is a two-stage wide band monolithic low noise amplifier. Typical applications range from telecommunication (point to point, point to multi-point, VSAT) to ISM and military markets.

The circuit is manufactured with a standard P-HEMT process: 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is supplied in lead-free SMD package.





Main Features

- Broadband performance 10-16GHz
- 2.5dB noise figure, 10-16GHz (BD)
- 16dB gain, ± 1.5dB gain flatness
- Low DC power consumption.
- 20dBm 3rd order intercept point (BE)
- 16L-QFN3x3 SMD package

(BD & BE refer to biasing conditions)

Main Characteristics

Tamb = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
NF	Noise figure, 10-16GHz (BD)		2.5	3.0	dB
G	Gain	14	16		dB
IP3	3rd order intercept point (BE)	20	21		dBm

ESD Protections: Electrostatic discharge sensitive device observe handling precautions!

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Electrical Characteristics (BD: Low current biasing)

Tamb = +25℃, Vd = +4V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	10		16	Ghz
G	Gain	14	16		dB
ΔG	Gain flatness		± 1.5	± 2.0	dB
NF	Noise figure		2.5	3.0	dB
VSWRin	Input VSWR		2.0 :1	3.0:1	
VSWRout	Ouput VSWR (11 to 16 GHz)		1.5:1	2.0:1	
IP3	3rd order intercept point	17	18		dBm
P1dB	Output power at 1dB gain compression	9.0	10		dBm
Id	Drain bias current		50	65	mA

These values are representative of onboard measurements based on the propose characterization board.

Absolute Maximum Ratings (1)

Tamb = +25℃

Symbol	Parameter (1)	Values	Unit
Vd	Drain bias voltage (2)	4.5	V
Pin	Maximum input power overdrive	-3.0	dBm
Rth_BD	Thermal Resistance channel to ground paddle (3)	155	℃/W
Rth_BE	Thermal Resistance channel to ground paddle (3)	195	℃/W
Top	Operating temperature range	-40 to +85	℃
Tstg	Storage temperature range	-55 to +125	℃

(1) Operation of this device above anyone of these paramaters may cause permanent damage.
(2) For a typical biasing circuit: B & D grounded. See chip biasing option page 9/12.
(3) Thermal resistance for Tamb. = +85℃ and a Tj max = +175℃.

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Electrical Characteristics (BE: High current biasing)

Tamb = +25°C, Vd = +4V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	10		16	Ghz
G	Gain	14	16		dB
ΔG	Gain flatness		± 1.5	± 2.0	dB
NF	Noise figure		3.0	3.5	dB
VSWRin	Input VSWR		2.0 :1	3.0:1	
VSWRout	Ouput VSWR (11 to 16 GHz)		1.5:1	2.0:1	
IP3	3rd order intercept point	20	21		dBm
P1dB	Output power at 1dB gain compression	13	14		dBm
Id	Drain bias current		70	80	mA

These values are representative of onboard measurements based on the propose characterization board.

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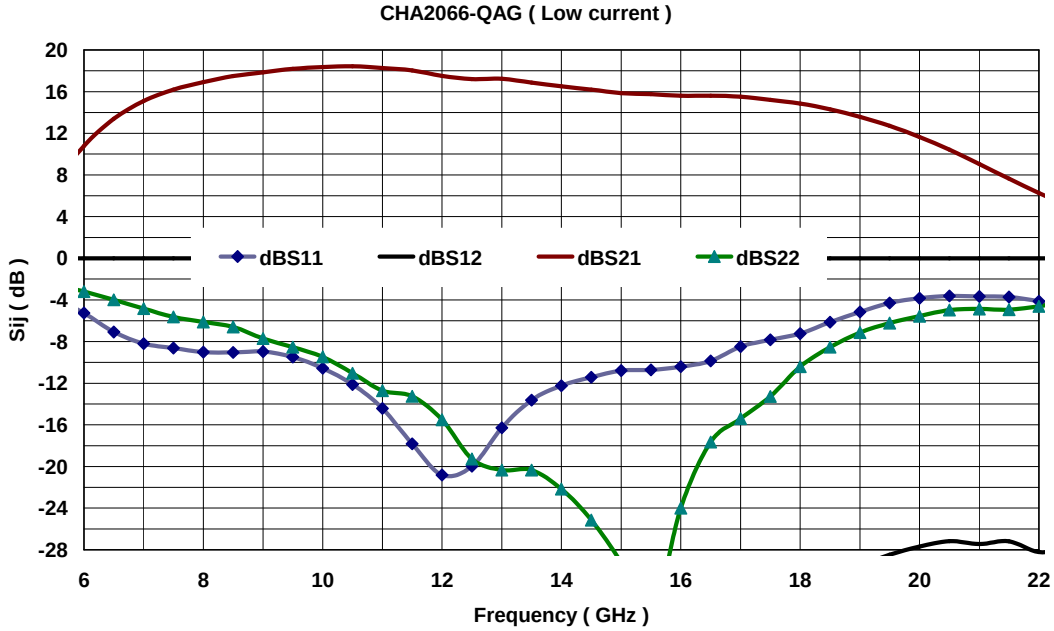
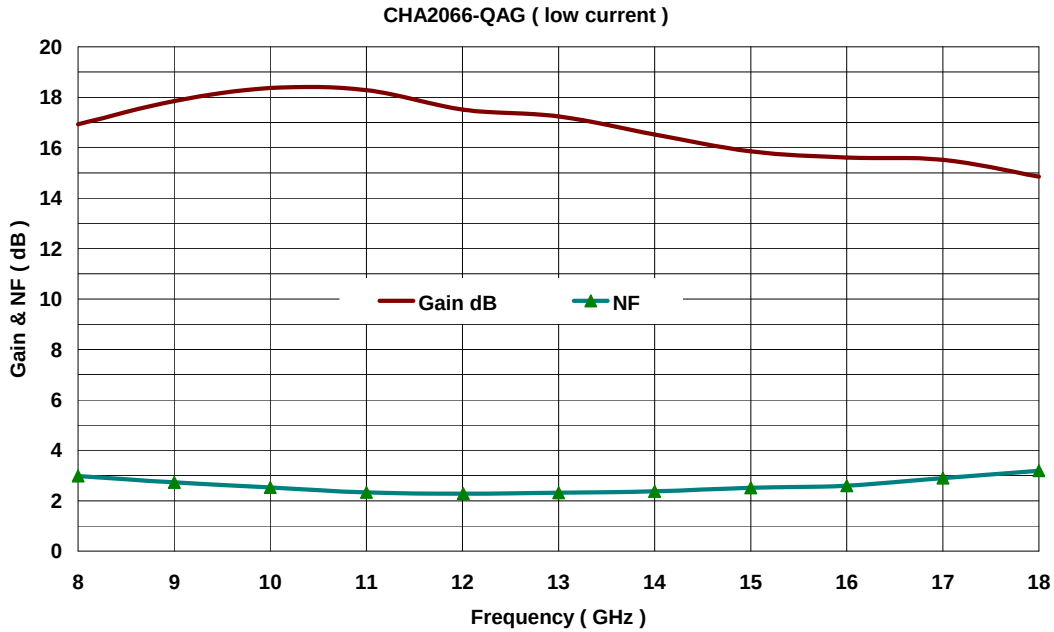
Typical PCB Measured Performance

BD: Low Noise & Low Consumption (T amb. 25°C; B & D grounded)

Tamb = +25°C, Vd = +4V



Sij in the package access plans, using the proposed land patern & board.



Gain & NF in the package, using the proposed land patern & board.

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Typical Package Sij parametres

BD: Low Noise & Low Consumption (T amb. 25°C; B & D grounded)

Tamb = +25°C, Vd = +4V

Freq (GHz)	dBS11	PS11	dBS12	PS12	dBS21	PS21	dBS22	PS22
1.00	-0.07	-32.81	-63.73	155.32	-45.04	-130.29	0.22	-22.46
2.00	-0.45	-65.34	-65.72	131.09	-43.50	173.73	0.11	-46.01
3.00	-0.88	-98.76	-55.17	81.01	-28.86	-84.51	-0.49	-70.41
4.00	-1.40	-137.64	-53.89	101.44	-9.03	-127.43	-1.62	-88.42
5.00	-2.92	174.92	-50.86	67.72	2.29	170.98	-1.91	-109.44
6.00	-5.26	114.65	-53.58	27.26	10.78	97.39	-3.20	-134.57
7.00	-8.21	49.08	-53.95	102.90	15.10	22.29	-4.84	-151.54
8.00	-9.01	-4.96	-42.49	83.25	16.93	-42.88	-6.12	-173.88
9.00	-8.96	-53.79	-38.52	49.24	17.85	-99.72	-7.71	158.77
10.00	-10.57	-99.92	-35.09	21.84	18.37	-151.89	-9.47	121.42
11.00	-14.43	-148.00	-32.70	-13.00	18.28	158.56	-12.71	72.56
12.00	-20.81	138.33	-30.58	-49.54	17.51	113.02	-15.50	19.69
13.00	-16.28	73.75	-31.37	-83.26	17.24	73.36	-20.34	-5.61
14.00	-12.25	24.06	-31.27	-109.01	16.52	33.07	-22.16	-29.50
15.00	-10.79	-4.78	-31.18	-131.65	15.85	-4.32	-29.27	-48.96
16.00	-10.41	-17.87	-30.83	-156.53	15.61	-40.93	-24.00	71.70
17.00	-8.49	-27.44	-31.91	173.64	15.52	-80.78	-15.41	45.23
18.00	-7.23	-40.10	-31.20	172.53	14.85	-123.20	-10.41	28.78
19.00	-5.15	-61.69	-29.59	153.69	13.57	-166.84	-7.13	2.09
20.00	-3.83	-87.40	-27.70	125.70	11.65	150.73	-5.57	-28.15
21.00	-3.66	-115.49	-27.45	94.93	9.04	111.11	-4.87	-54.30
22.00	-4.12	-138.34	-28.22	69.02	6.26	76.39	-4.61	-75.71
23.00	-5.14	-158.51	-27.99	46.60	3.63	43.54	-4.03	-94.54
24.00	-6.57	-170.13	-28.22	26.29	0.88	10.62	-3.53	-111.54
25.00	-7.93	-173.76	-28.81	2.91	-2.22	-22.25	-2.63	-126.44
26.00	-7.57	-165.83	-29.57	-22.04	-6.10	-54.04	-2.08	-141.15
27.00	-5.73	-166.05	-31.13	-34.87	-10.73	-78.74	-1.64	-154.74
28.00	-3.48	-172.97	-31.61	-56.30	-15.64	-97.73	-1.05	-166.34
29.00	-2.24	176.23	-33.44	-68.53	-20.49	-104.47	-0.77	-176.68
30.00	-1.67	166.40	-34.06	-82.14	-24.09	-106.27	-0.27	173.66

Refere to the “definition of the Sij reference plans” section below.

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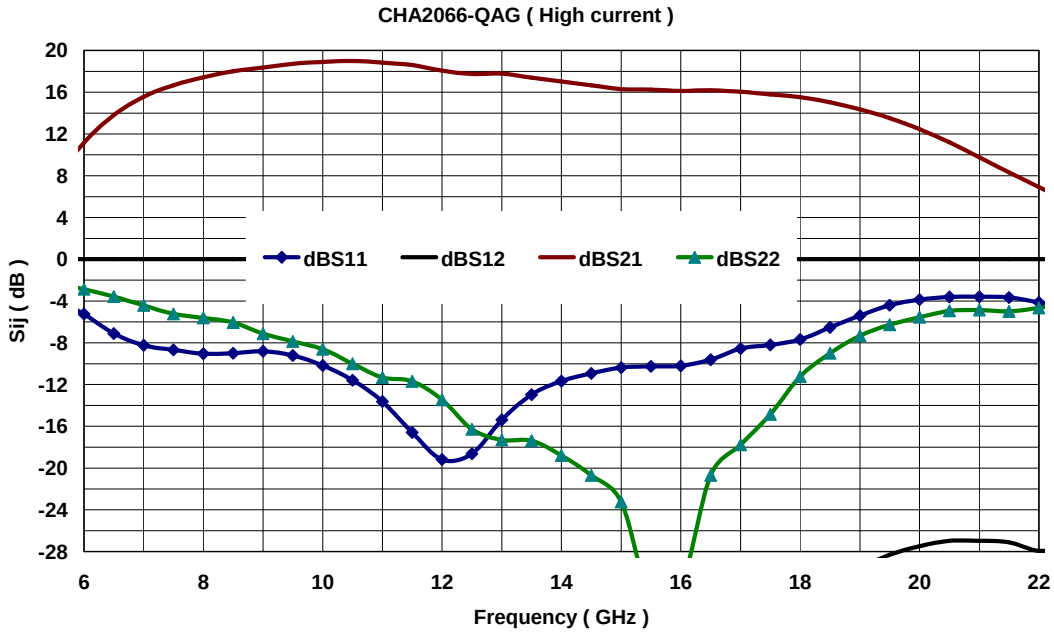
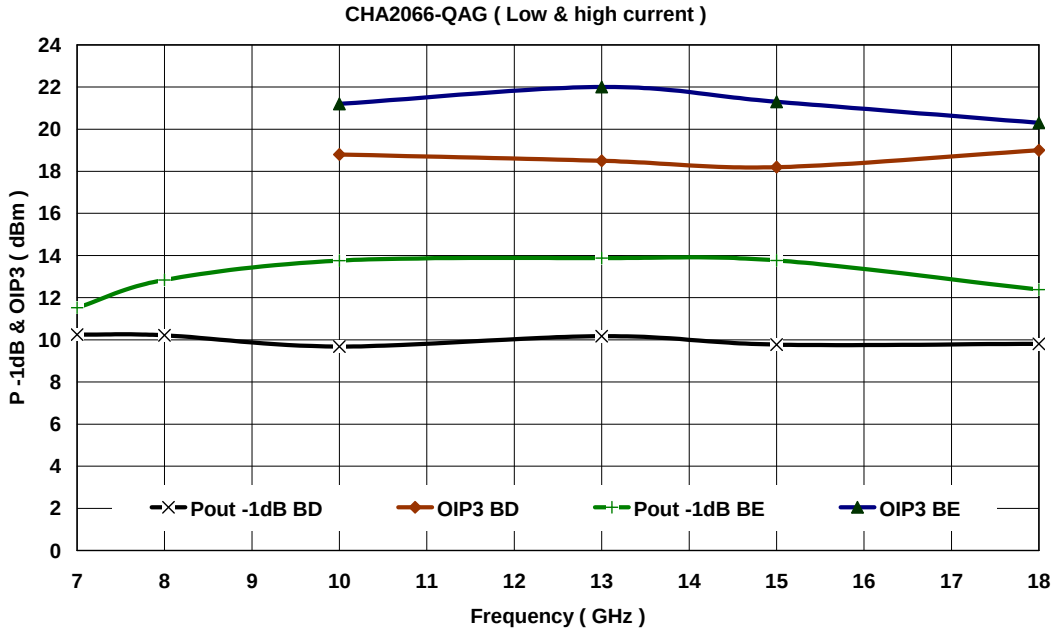
Typical PCB Measured Performance

BE: Low Noise & High Consumption (T amb. 25°C; B & E grounded)

Tamb = +25°C, Vd = +4V



Sij in the package access plans, using the proposed land patern & board.



Pout –1dB & OIP3 in the package, using the proposed land patern & board.

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Typical Package Sij parametres

BE: Low Noise & High Consumption (T amb. 25°C; B & E grounded)

Tamb = +25°C, Vd = +4V

Freq	dBS11	PS11	dBS12	PS12	dBS21	PS21	dBS22	PS22
1.00	-0.06	-32.83	-63.05	154.13	-43.95	-133.71	0.25	-22.35
2.00	-0.44	-65.39	-65.94	130.29	-43.95	170.25	0.13	-46.01
3.00	-0.87	-98.89	-55.38	78.54	-27.08	-76.01	-0.53	-70.57
4.00	-1.38	-137.90	-54.31	104.66	-8.50	-128.93	-1.50	-87.59
5.00	-2.91	174.61	-50.63	69.94	2.61	170.88	-1.70	-109.15
6.00	-5.25	114.52	-52.37	30.30	11.16	98.22	-2.87	-134.71
7.00	-8.24	49.38	-52.51	86.03	15.55	23.53	-4.42	-152.27
8.00	-9.04	-4.12	-42.99	80.40	17.42	-41.65	-5.62	-176.16
9.00	-8.81	-53.24	-38.92	48.79	18.37	-98.51	-7.13	155.31
10.00	-10.18	-100.30	-35.31	22.90	18.91	-150.77	-8.61	116.72
11.00	-13.62	-149.42	-32.83	-11.96	18.84	159.62	-11.31	67.54
12.00	-19.18	138.59	-30.61	-48.80	18.07	113.90	-13.46	17.22
13.00	-15.38	75.97	-31.34	-82.22	17.78	74.36	-17.32	-11.39
14.00	-11.68	24.19	-31.15	-108.12	17.02	34.08	-18.79	-38.57
15.00	-10.38	-7.42	-30.90	-131.51	16.30	-2.99	-23.23	-70.09
16.00	-10.21	-21.88	-30.60	-157.78	16.13	-38.98	-31.30	81.59
17.00	-8.57	-33.43	-32.22	174.12	16.05	-78.76	-17.77	47.88
18.00	-7.68	-43.47	-31.34	173.10	15.52	-120.87	-11.24	33.04
19.00	-5.40	-62.60	-29.57	155.96	14.35	-165.06	-7.34	5.05
20.00	-3.86	-87.55	-27.49	127.88	12.46	151.53	-5.55	-27.38
21.00	-3.60	-115.42	-26.98	96.14	9.77	111.34	-4.86	-54.73
22.00	-4.13	-138.36	-27.93	70.63	6.91	76.47	-4.66	-76.49
23.00	-5.13	-158.10	-27.69	46.58	4.26	43.61	-4.09	-95.03
24.00	-6.56	-169.57	-27.90	26.86	1.48	10.62	-3.57	-111.80
25.00	-7.89	-172.95	-28.39	2.79	-1.62	-22.36	-2.65	-126.37
26.00	-7.56	-165.38	-29.21	-22.16	-5.55	-54.31	-2.10	-141.05
27.00	-5.73	-165.65	-30.78	-35.27	-10.18	-79.17	-1.65	-154.66
28.00	-3.52	-172.96	-31.33	-57.32	-15.13	-98.50	-1.05	-166.34
29.00	-2.28	176.11	-33.18	-69.14	-20.05	-105.53	-0.78	-176.83
30.00	-1.74	165.52	-33.95	-83.12	-23.73	-107.10	-0.28	173.49

Refere to the “definition of the Sij reference plans” section below.

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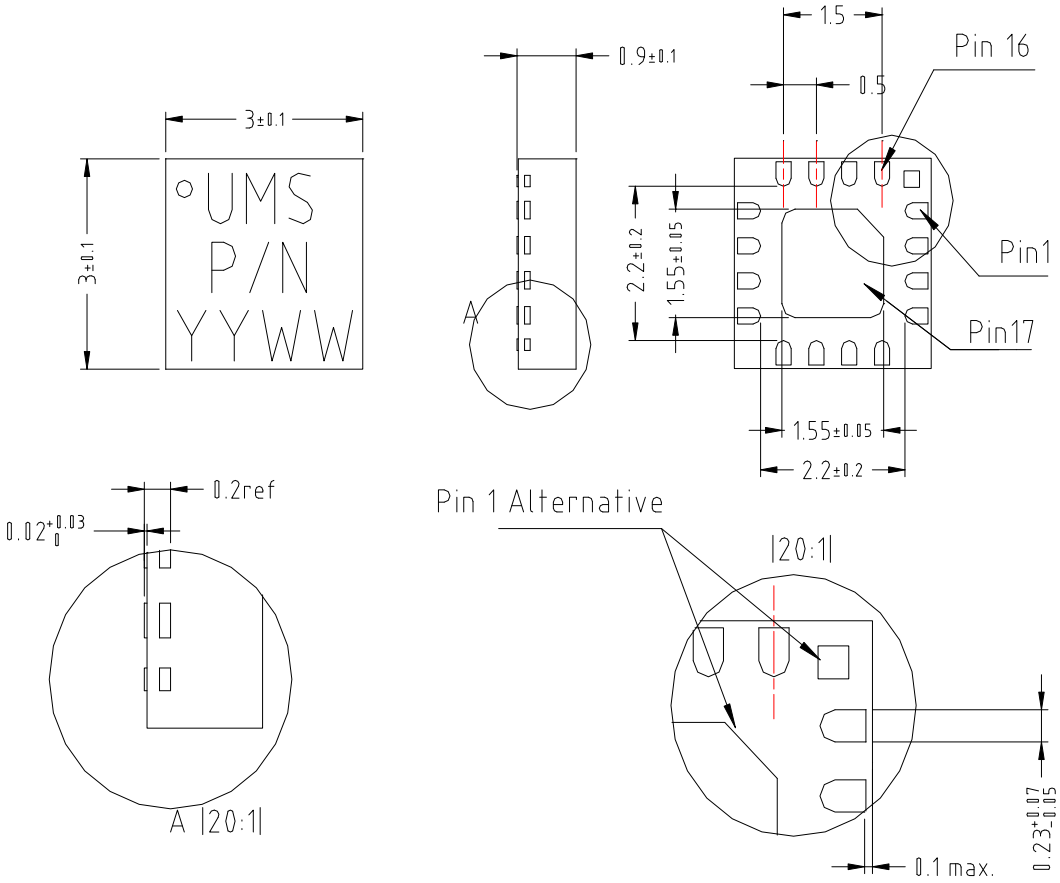
Package outline:



Matt tin, Lead Free	(Green)	1-	NC	9-	GND
Units	mm	2-	GND	10-	RF out
From the standard	JEDEC MO-220	3-	RF in	11-	GND
	17- GND	4-	GND	12-	NC
		5-	NC	13-	NC
		6-	B	14-	Vd
		7-	D	15-	Vg2
		8-	E	16-	Vg1

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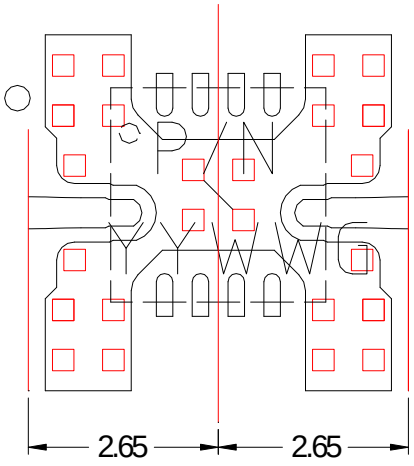
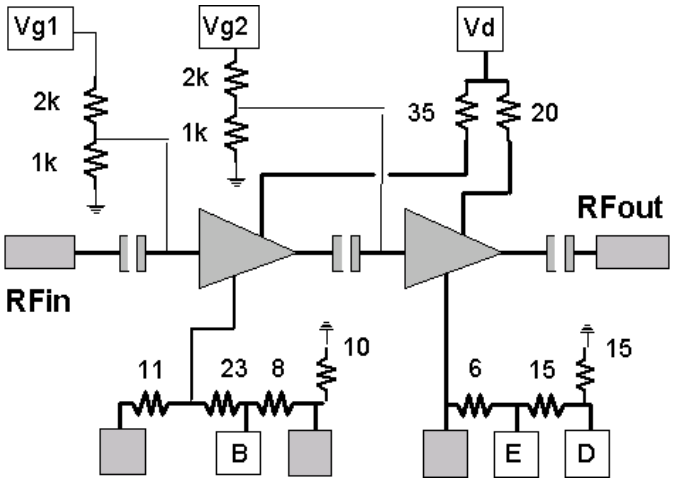
Definition of the Sij reference plans

The reference plans are defined from the footprint of the recommended characterization board shown below under the number 95542.
The reference is the symmetrical axis of the package. The input is and output reference plans are located at 2.65mm offset (input wise and output wise respec.) from this axis. Then, the given Sij incorporates this land patern.



Circuit Biasing options

This circuit is self-biased, and flexibility is provided by the access to number of pads. the internal DC electrical schematic is given in order to use these pads in a safe way.



- The two requirements are:
N°1: Not exceed Vds = 3.5Volt (internal Drain to S ource voltage).
N°2: Not biased in such a way that Vgs becomes posi tive. (Internal Gate to Source voltage)

- We propose two standard biasing:

Low Noise and low consumption BD:	Vd = 4V, B and D grounded, and E not connected.
	Idd = 50mA & Pout-1dB = +10dBm Typical.
Low Noise and high output power BE:	Vd = 4V, B and E grounded.
	Idd = 70mA & Pout-1dB = +14dBm Typical.

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Application note

The design of the motherboard has a strong impact on the over all performance since the transition from the motherboard to the package is comparably large. In case of the SMD type packages of United Monolithic Semiconductors the motherboard should be designed according to the information given in the following to achieve good performance. Other configurations are also possible but can lead to different results. If you need advise please contact United Monolithic Semiconductors for further information.

SMD type packages of UMS should allow design and fabrication of micro- and mm-wave modules at low cost. Therefore, a suitable motherboard environment has been chosen. All tests and verifications have been performed on Rogers RO4003. This material exhibits a permittivity of 3.38 and has been used with a thickness of 200µm [8 mils] and a 1/2oz or less copper cladding. The corresponding 50Ohm transmission line has a strip width of about 460µm [approx. 18 mils].

The contact areas on the motherboard for the package connections should be designed according to the footprint given below. The proper via structure under the ground pad is very important in order to achieve a good RF and lifetime performance. All tests have been done by using a grid of plated through vias with a diameter of less than 300µm [12 mils] and a spacing of less than 700µm [28 mils] from the centres of two adjacent vias. The via grid should cover the whole space under the ground pad and the vias closest to the RF ports should be located near the edge of the pad to allow a good RF ground connection. Since the vias are important for heat transfer, a proper via filling should be guaranteed during the mounting procedure to get a low thermal resistance between package and heat sink. For power devices the use of heat slugs in the motherboard instead of a grid of via's is recommended.

For the mounting process the SMD type package can be handled as a standard surface mount component. The use of either solder or conductive epoxy is possible. The solder thickness after reflow should be typical 50µm [2 mils] and the lateral alignment between the package and the motherboard should be within 50µm [2 mils]. Caution should be taken to obtain a good and reliable contact over the whole pad areas. Voids or other improper connections, in particular, between the ground pads of motherboard and package will lead to a deterioration of the RF performance and the heat dissipation. The latter effect can reduce drastically reliability and lifetime of the product.

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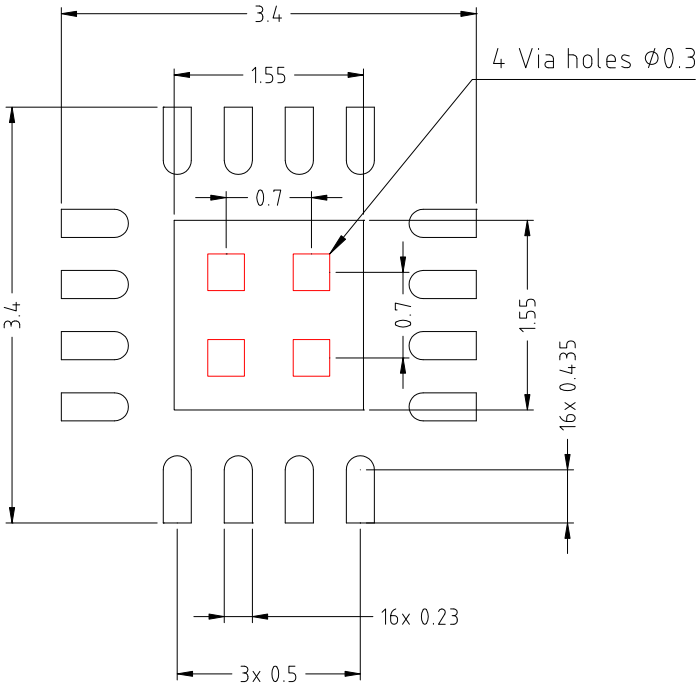

(For production, design must be adapted with regard to PCB tolerances and assembly process)

Basic footprint for a 16L-QFN3x3 (all unit mm)
(Please, refer to the UMS proposed footprint for optimum operation in the following “Proposed Assembly board” section)

The RF ports are DC blocked on chip. The DC connection (Vd) does not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling on the PC board, as close as possible to the package.

SMD mounting procedure

The SMD leadless package has been designed for high volume surface mount PCB assembly process. The dimensions and footprint required for the PCB (motherboard) are given in the drawings above.

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

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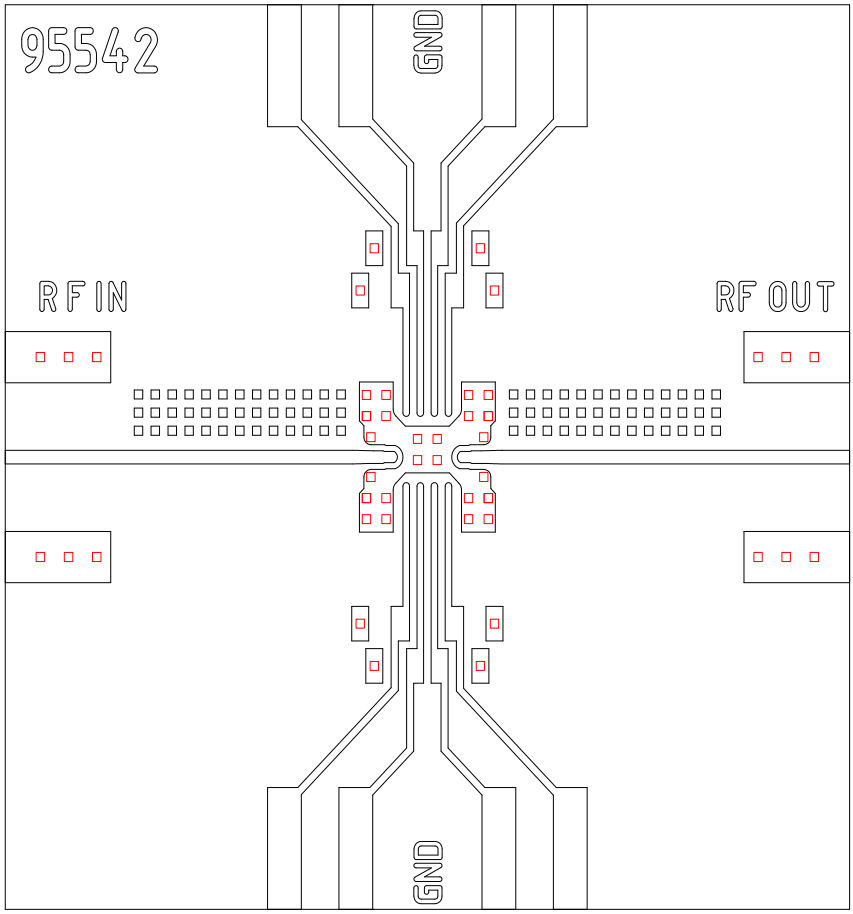
Proposed Assembly board for the 16L-QFN3x3 products characterization.

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a microstrip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.



Ordering Information

QFN 3x3 RoHS compliant package: CHA2066-QAG/XY
Stick: XY = 20 Tape & reel: XY = 21

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