

S band Digital VGA

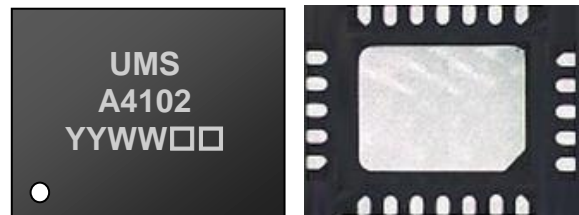
GaAs Monolithic Microwave IC in SMD leadless package

Description

The CHA4102-QEG is a variable gain amplifier monolithic circuit, which integrates 6 bit digital attenuator and a 2 stage driver amplifier that produces 20dB gain, an output power of 23.5dBm and a dynamic attenuator range of 31.5dB.

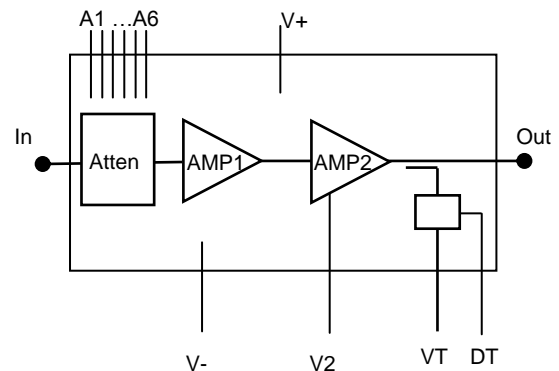
It is designed for a wide range of applications, from military to commercial communication systems.

The circuit is manufactured with a pHEMT process, 0.25 μ m gate length, via holes through the substrate, air bridges and electron beam gate lithography.



Main Features

- Broadband performances: 2-4GHz
- Linear gain : 20dB
- Output power @ 1dB: 23.5dBm
- Dynamic attenuation range: 31.5dBm
- Attenuation error: ± 0.5 dB
- DC bias: $V_d=5$ Volt@ $I_d=150$ mA
- 24L-QFN4x5
- MSL1



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	2		4	GHz
Gain	Linear Gain		20		dB
Att	Attenuation range		31.5		dB
P1dB	Output Power @1dB comp.		23.5		dBm

Electrical Characteristics

Tamb.= +25°C, V+ = +5V

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	2		4	GHz
Gain	Linear Gain (state 0)		20		dB
Gvt	Small signal gain variation versus temperature		0.04		dB/°C
S11	Input return loss		13		dB
S22	Output return loss		12		dB
AttErr1	Attenuation error for states 1 to 2		±0.25		dB
AttErr2	Attenuation error for states 3 to 30		±0.5		dB
AttErr3	Attenuation error for states 31 to 63		±0.7	0.7	dB
RMS_Att Err	RMS Attenuation error		0.2		dB
PhiVar1	Phase variation for states 0 to 7		-2/+3		°
PhiVar2	Phase variation for states 8 to 32		-5/+2.5		°
PhiVar3	Phase variation for states 33 to 63		-3/+5.5		°
RMS_Phi Var	RMS Phase variation		1.2		°
P1dB	Output power at 1dB gain compression		23.5		dB
V+	DC positive supply		+5		V
V2	DC positive supply of the output amplifier		+5		V
VT	DC positive supply of the detector		+5		V
V-	DC negative supply		-5		V
Vctrl_L	Attenuator control voltage (low state)	-	0	0.4	V
Vctrl_H	Attenuator control voltage (high state)	2.4	3.3	5	V
I_V+	General DC current in small signal		42		mA
I_V2	Output amplifier DC current in small signal		155		mA
I_V-	Negative DC current in small signal		23		mA
Vdet1	Detected Voltage for Pout = 23 dBm		1.5		V
Vdet2	Detected Voltage for Pout = -10 dBm		0		V
Ts	Switching time		15		ns

These values are representative of measurements at QFN reference plan

Attenuation Error (AttErr) definition

$$\text{AttErr}(i) = \text{Measured_dB}(S21)\text{state}(i) - \text{Measured_dB}(S21)\text{state}(0) - \text{theoreticalAttenValueState}(i)$$

(i) is in the range [0:63]

AttErr(i) is in dB and AttErrLin(i) is the corresponding linear value :

$$\text{AttErr}(i) = \text{dB}(\text{AttErrLin}(i))$$

Phase Variation (PhiVar) definition

$$\text{PhiVar}(i) = \text{measured_Phase}(S21)\text{@state}(i) - \text{measured_Phase}(S21)\text{@state}(0)$$

(i) is in the range [0:63]

RMS Attenuation Error (RMS_AttErr) definition

$$\text{RMS_AttErr} = \text{dB} \left(\sqrt{\frac{\sum_{i=0}^{63} \text{AttErrLin}(i)^2}{64}} \right)$$

RMS Phase Variation (RMS_PhiVar) definition

$$\text{RMS_PhiVar} = \sqrt{\frac{\sum_{i=0}^{63} \text{PhiVar}(i)^2}{64}}$$

Absolute Maximum Ratings ⁽¹⁾

Tamb.= +25°C

Symbol	Parameter	Values	Unit
V+	Maximum DC positive supply	+6	V
VT	Maximum DC positive supply of the detector	+6	V
V2	Maximum DC positive supply of the output amplifier	+5.5	V
V-	Maximum DC negative supply	-6	V
Vctrl	Attenuation control voltage (Vlow Vhigh)	-0.5 +5.5	V
Pin_Max	Maximum peak input power overdrive at state 0	+20	dBm
Top	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +150	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad N°	Parameter	Values	Unit
V+	13	DC supply voltage TTL interface + 1 st stage	+5	V
V2	2	DC supply voltage 2st stage	+5	V
V-	1	DC supply voltage	-5	

Attenuator control table

Voltage to apply on the pads A1 to A6:

state	Att (dB)	A6	A5	A4	A3	A2	A1	state	Att (dB)	A6	A5	A4	A3	A2	A1
0	0	0	0	0	0	0	0	33	16.5	3.3	0	0	0	0	3.3
1	0.5	0	0	0	0	0	3.3	34	17	3.3	0	0	0	3.3	0
2	1	0	0	0	0	3.3	0	35	17.5	3.3	0	0	0	3.3	3.3
3	1.5	0	0	0	0	3.3	3.3	36	18	3.3	0	0	3.3	0	0
4	2	0	0	0	3.3	0	0	37	18.5	3.3	0	0	3.3	0	3.3
5	2.5	0	0	0	3.3	0	3.3	38	19	3.3	0	0	3.3	3.3	0
6	3	0	0	0	3.3	3.3	0	39	19.5	3.3	0	0	3.3	3.3	3.3
7	3.5	0	0	0	3.3	3.3	3.3	40	20	3.3	0	3.3	0	0	0
8	4	0	0	3.3	0	0	0	41	20.5	3.3	0	3.3	0	0	3.3
9	4.5	0	0	3.3	0	0	3.3	42	21	3.3	0	3.3	0	3.3	0
10	5	0	0	3.3	0	3.3	0	43	21.5	3.3	0	3.3	0	3.3	3.3
11	5.5	0	0	3.3	0	3.3	3.3	44	22	3.3	0	3.3	3.3	0	0
12	6	0	0	3.3	3.3	0	0	45	22.5	3.3	0	3.3	3.3	0	3.3
13	6.5	0	0	3.3	3.3	0	3.3	46	23	3.3	0	3.3	3.3	3.3	0
14	7	0	0	3.3	3.3	3.3	0	47	23.5	3.3	0	3.3	3.3	3.3	3.3
15	7.5	0	0	3.3	3.3	3.3	3.3	48	24	3.3	3.3	0	0	0	0
16	8	0	3.3	0	0	0	0	49	24.5	3.3	3.3	0	0	0	3.3
17	8.5	0	3.3	0	0	0	3.3	50	25	3.3	3.3	0	0	3.3	0
18	9	0	3.3	0	0	3.3	0	51	25.5	3.3	3.3	0	0	3.3	3.3
19	9.5	0	3.3	0	0	3.3	3.3	52	26	3.3	3.3	0	3.3	0	0
20	10	0	3.3	0	3.3	0	0	53	26.5	3.3	3.3	0	3.3	0	3.3
21	10.5	0	3.3	0	3.3	0	3.3	54	27	3.3	3.3	0	3.3	3.3	0
22	11	0	3.3	0	3.3	3.3	0	55	27.5	3.3	3.3	0	3.3	3.3	3.3
23	11.5	0	3.3	0	3.3	3.3	3.3	56	28	3.3	3.3	3.3	0	0	0
24	12	0	3.3	3.3	0	0	0	57	28.5	3.3	3.3	3.3	0	0	3.3
25	12.5	0	3.3	3.3	0	0	3.3	58	29	3.3	3.3	3.3	0	3.3	0
26	13	0	3.3	3.3	0	3.3	0	59	29.5	3.3	3.3	3.3	0	3.3	3.3
27	13.5	0	3.3	3.3	0	3.3	3.3	60	30	3.3	3.3	3.3	3.3	0	0
28	14	0	3.3	3.3	3.3	0	0	61	30.5	3.3	3.3	3.3	3.3	0	3.3
29	14.5	0	3.3	3.3	3.3	0	3.3	62	31	3.3	3.3	3.3	3.3	3.3	0
30	15	0	3.3	3.3	3.3	3.3	0	63	31.5	3.3	3.3	3.3	3.3	3.3	3.3
31	15.5	0	3.3	3.3	3.3	3.3	3.3								
32	16	3.3	0	0	0	0	0								

Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered).

The temperature is monitored at the package back-side interface (Tcase) as shown below. The system maximum temperature must be adjusted in order to guarantee that Tcase remains below the maximum value specified in the next table. So, the PCB system must be designed to comply with this requirement.

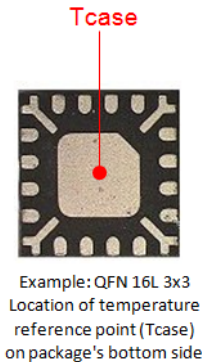
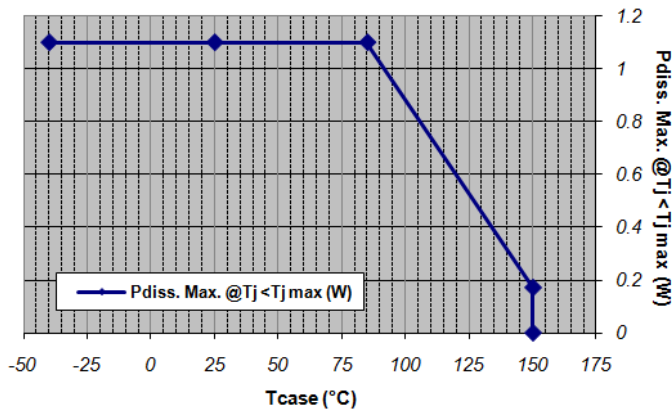
A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

DEVICE THERMAL SPECIFICATION : CHA4102-QEG	
Recommended max. junction temperature (Tj max)	: 162 °C
Junction temperature absolute maximum rating	: 175 °C
Max. continuous dissipated power (Pdiss. Max.)	: 1.1 W
=> Pdiss. Max. derating above Tcase ⁽¹⁾ = 85 °C	: 14 mW/°C
Junction-Case thermal resistance (Rth J-C) ⁽²⁾	: <70 °C/W
Minimum Tcase operating temperature ⁽³⁾	: -40 °C
Maximum Tcase operating temperature ⁽³⁾	: 85 °C
Minimum storage temperature	: -55 °C
Maximum storage temperature	: 150 °C

(1) Derating at junction temperature constant = Tj max.

(2) Rth J-C is calculated for a worst case considering the **hottest junction** of the MMIC and all the devices biased.

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).



6.4

Typical Package Sij parameters

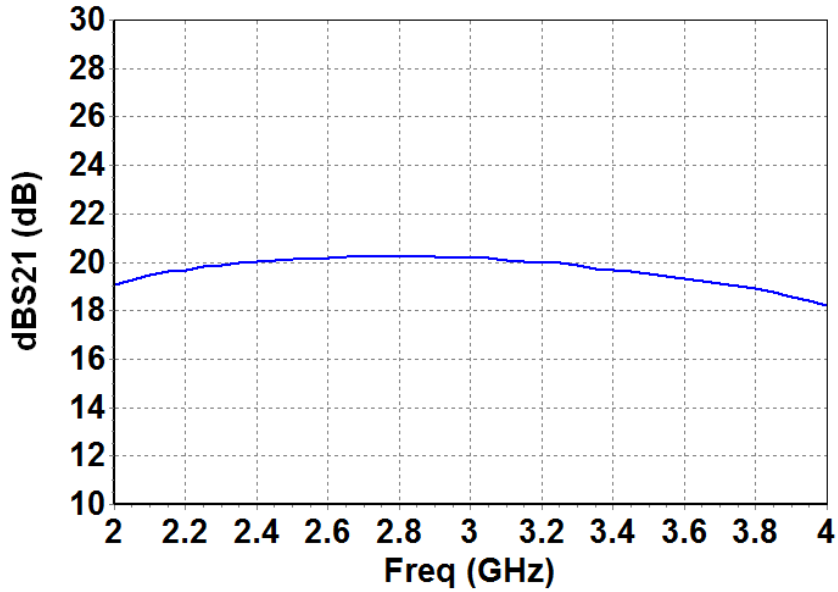
Tamb.= +25°C, V+ = +5V, Id (I_V+ & I_V2) = 220mA ; State 0

Freq (GHz)	S11 (dB)	PhS11 (°)	S12 (dB)	PhS12 (°)	S21 (dB)	PhS21 (°)	S22 (dB)	PhS22 (°)
2.00	-10.38	-117.50	-51.00	-62.41	19.08	-141.10	-18.10	177.30
2.05	-10.26	-121.20	-50.63	-75.73	19.29	-152.90	-18.23	179.20
2.10	-10.20	-124.00	-50.36	-88.28	19.47	-164.20	-18.24	-178.90
2.15	-10.22	-126.20	-50.48	-97.06	19.60	-175.10	-18.23	-176.00
2.20	-10.36	-128.90	-50.82	-110.10	19.69	174.00	-18.09	-174.00
2.25	-10.44	-131.90	-50.31	-123.00	19.80	163.10	-17.81	-172.40
2.30	-10.52	-134.30	-49.96	-134.40	19.90	152.60	-17.37	-171.40
2.35	-10.66	-136.80	-49.78	-144.70	19.95	142.40	-16.88	-170.20
2.40	-10.84	-138.80	-49.73	-156.10	20.01	132.00	-16.34	-170.40
2.45	-11.04	-141.20	-49.76	-166.90	20.08	121.80	-15.81	-171.10
2.50	-11.25	-142.80	-49.27	-178.60	20.12	112.10	-15.33	-172.80
2.55	-11.43	-144.20	-49.01	171.10	20.15	102.30	-14.85	-175.00
2.60	-11.66	-146.00	-48.71	161.10	20.18	92.29	-14.44	-177.30
2.65	-11.88	-147.40	-48.55	152.10	20.21	82.42	-14.08	179.50
2.70	-12.10	-148.50	-48.20	142.00	20.22	72.92	-13.77	176.30
2.75	-12.39	-149.40	-48.13	131.20	20.21	63.45	-13.53	173.20
2.80	-12.49	-149.70	-47.88	122.10	20.24	53.69	-13.34	169.50
2.85	-12.67	-150.10	-47.62	111.90	20.26	43.99	-13.20	165.80
2.90	-12.74	-150.50	-47.22	103.30	20.24	34.52	-13.16	162.20
2.95	-12.79	-151.30	-47.25	93.28	20.19	25.10	-13.18	158.60
3.00	-12.82	-151.60	-46.94	84.71	20.20	15.58	-13.26	155.10
3.05	-12.79	-152.60	-46.70	75.43	20.16	6.05	-13.36	151.50
3.10	-12.76	-153.20	-46.61	66.43	20.09	-3.26	-13.48	148.80
3.15	-12.62	-155.10	-46.51	57.33	20.00	-12.74	-13.83	145.60
3.20	-12.70	-157.30	-46.42	47.34	19.99	-22.83	-14.05	142.30
3.25	-12.58	-159.00	-46.14	39.47	19.97	-31.72	-14.33	140.20
3.30	-12.66	-160.80	-46.14	30.98	19.86	-40.78	-14.70	138.40
3.35	-12.81	-164.90	-46.10	21.85	19.74	-50.68	-15.18	136.70
3.40	-12.97	-167.60	-45.94	13.03	19.68	-60.35	-15.57	134.50
3.45	-13.15	-169.70	-45.86	5.34	19.64	-68.88	-15.96	134.40
3.50	-13.58	-172.60	-45.73	-2.69	19.52	-78.02	-16.39	134.50
3.55	-14.06	-176.40	-45.83	-11.26	19.40	-88.03	-16.95	134.40
3.60	-14.60	-178.40	-45.73	-19.74	19.31	-97.64	-17.35	134.30
3.65	-15.29	-180.00	-45.53	-26.97	19.23	-106.20	-17.70	136.10
3.70	-16.22	179.00	-45.60	-35.58	19.13	-115.50	-18.11	138.40
3.75	-17.32	178.00	-45.74	-44.02	19.00	-125.80	-18.60	141.00
3.80	-18.46	-178.20	-45.75	-52.57	18.90	-134.70	-18.83	143.70
3.85	-19.63	-172.20	-45.82	-60.48	18.77	-144.30	-19.01	147.30
3.90	-20.47	-161.90	-45.93	-68.28	18.58	-154.00	-19.13	152.00
4.00	-20.39	-148.50	-45.97	-76.35	18.40	-164.30	-19.02	155.70

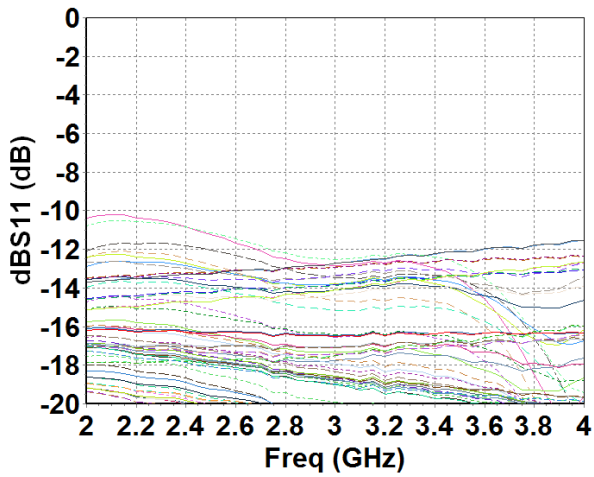
Typical Board Measurements

Tamb.= +25°C, V+ = +5V, V- = -5V, packaged device, reference plan = QFN

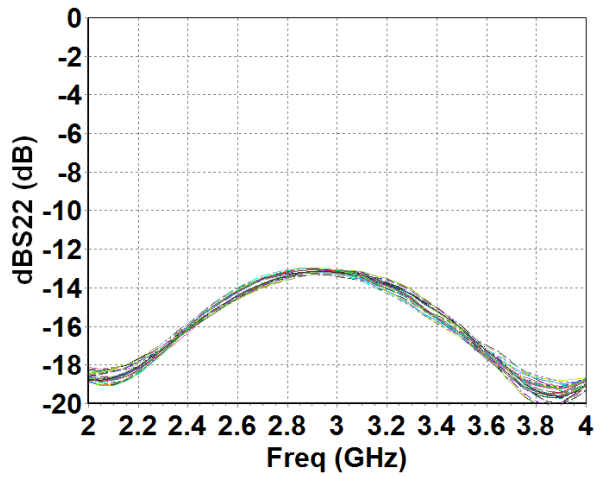
Linear Gain versus Frequency (state 0)



Input Return Loss versus Frequency (all states)



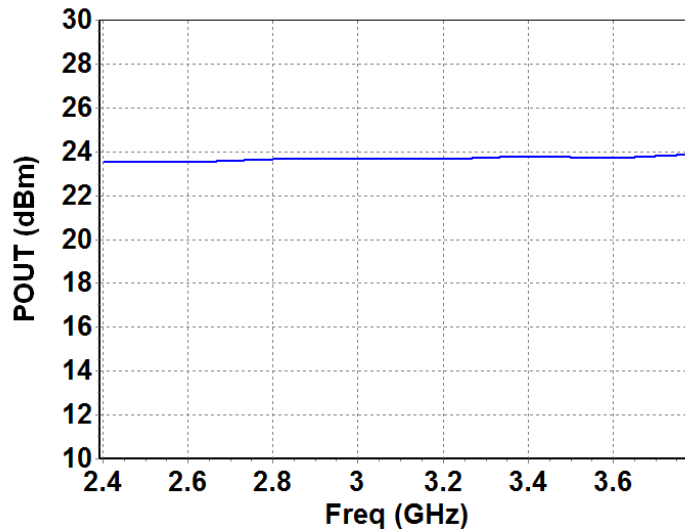
Output Return Loss versus Frequency (all states)



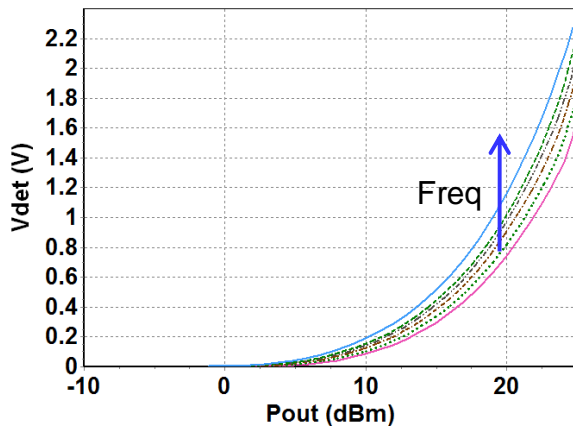
Typical Board Measurements

Tamb.= +25°C, V+ = +5V, V- = -5V, packaged device, reference plan = QFN

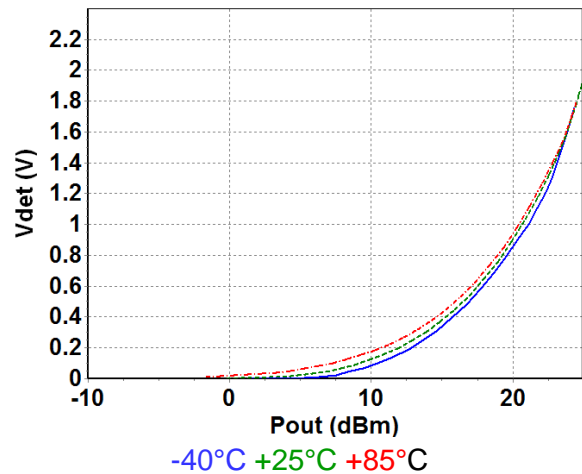
**Output Power versus Frequency
(state 0)**



**Detected Voltage versus Output Power
(Frequency 2.6-3.6GHz)
(Temperature = 25°C)**



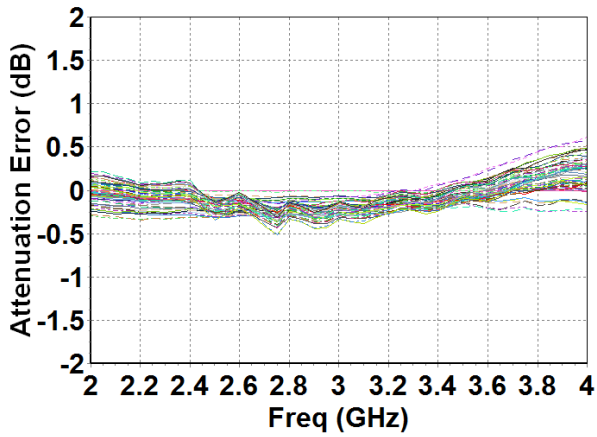
**Detected Voltage versus Output Power
(Frequency 3GHz)
(Temperature = - 40, 25°C, +85°C)**



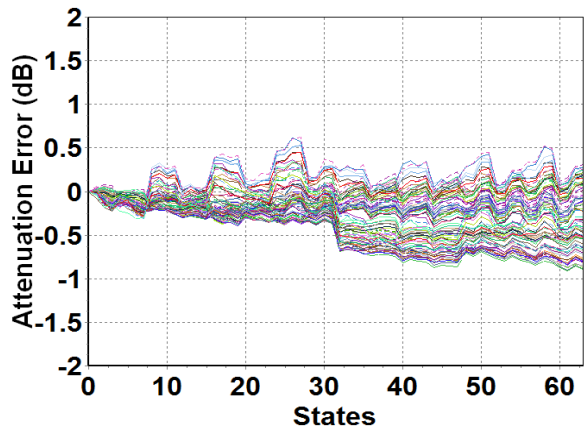
Typical Board Measurements

Tamb.= +25°C, V+ = +5V, V- = -5V, packaged device, reference plan = QFN

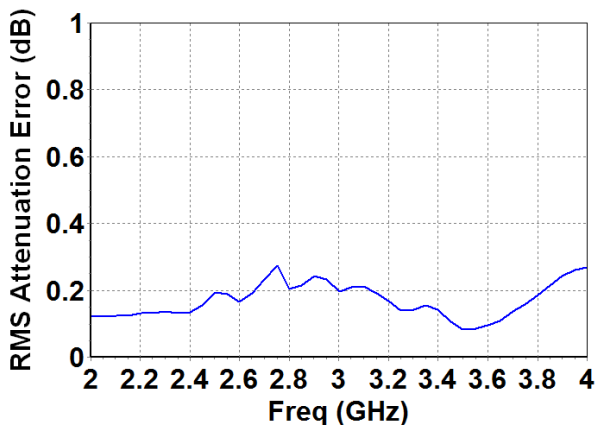
**Attenuation Error versus Frequency
(all states)**



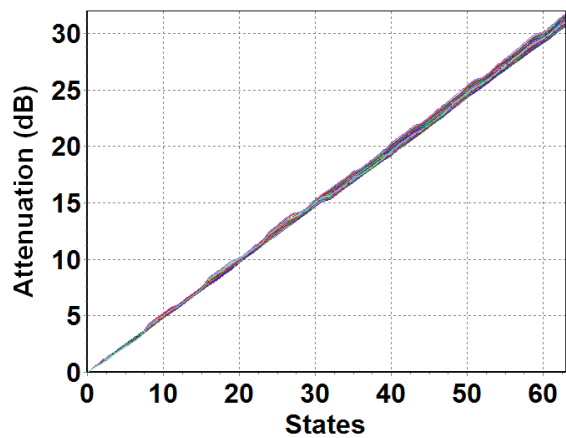
**Attenuation Error versus States
(Frequency 2-4GHz)**



**RMS Attenuation Error versus Frequency
(all states)**



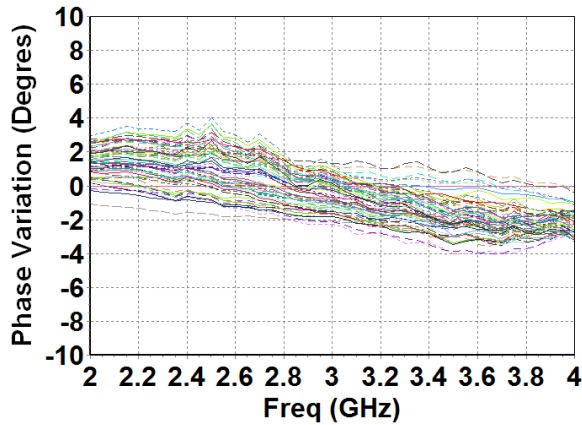
**Attenuation versus States
(Frequency 2-4GHz)**



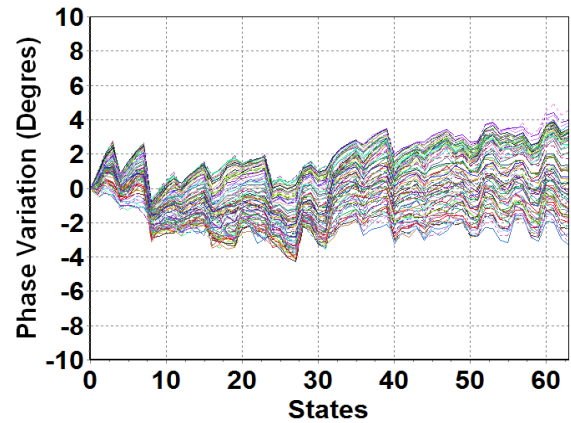
Typical Board Measurements

Tamb.= +25°C, V+ = +5V, V- = -5V, packaged device, reference plan = QFN

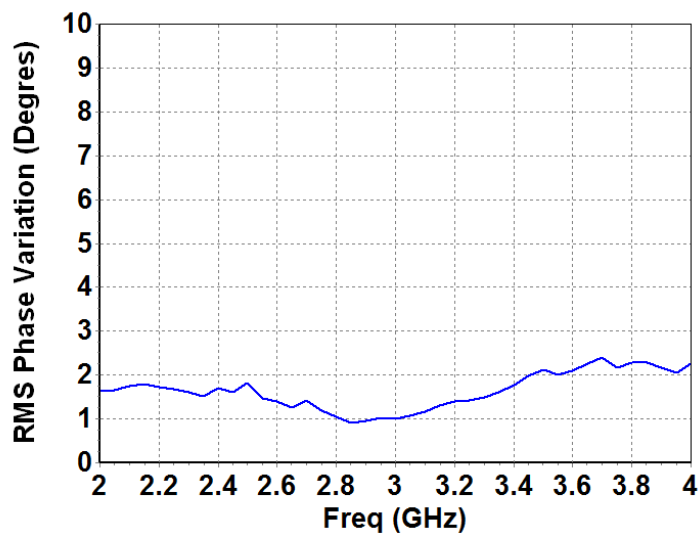
**Phase Variation versus Frequency
(all states)**



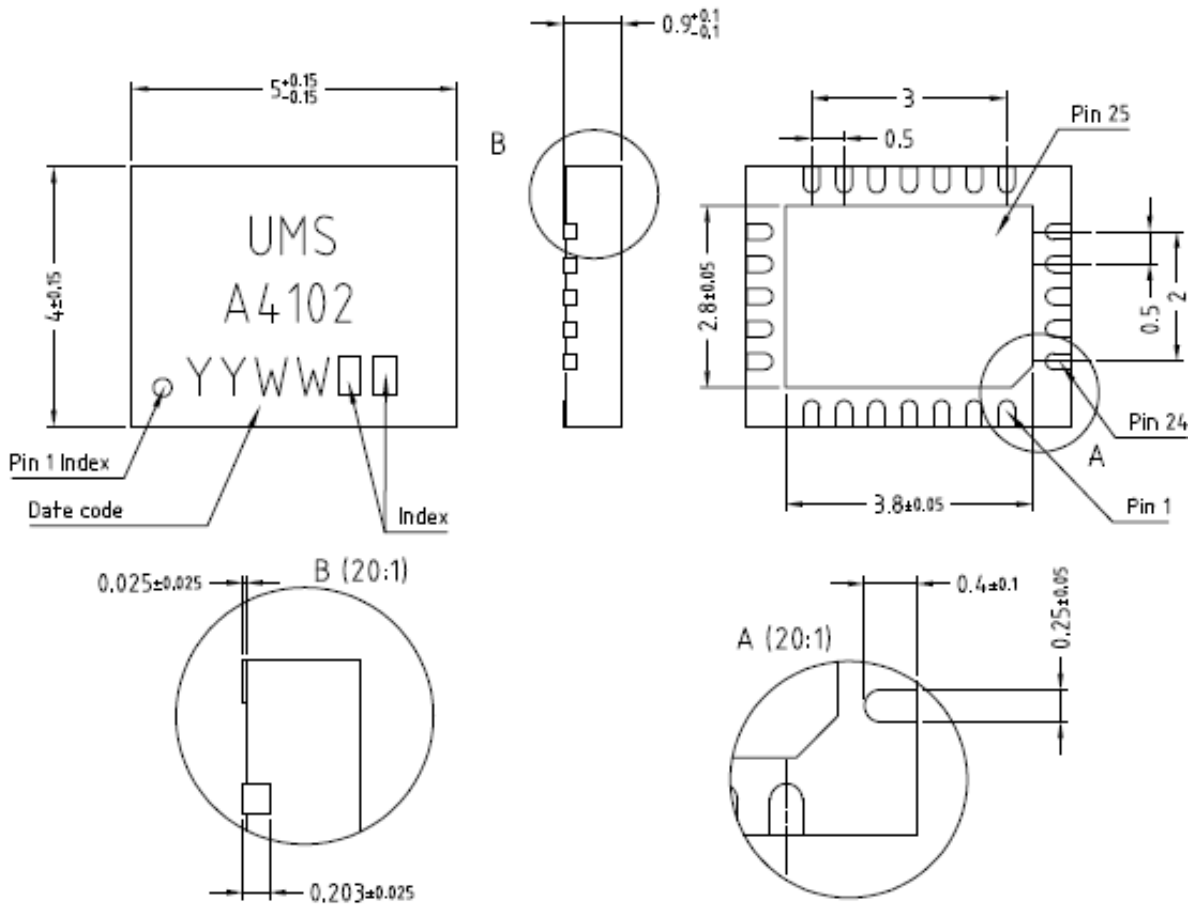
**Phase Variation versus States
(Frequency 2-4GHz)**



**Input Return Loss versus Frequency
(all states)**



Package outline ⁽¹⁾



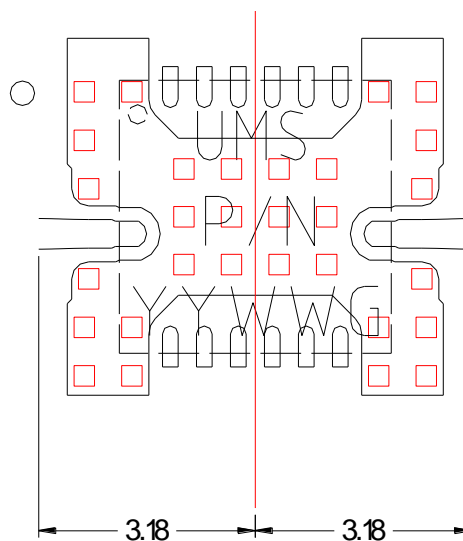
Matt tin, Lead Free (Green)		1- V-	9- Gnd ⁽²⁾	17- A3
Units : mm		2- V2	10- Nc	18- A2
From the standard : JEDEC MO-220 (VGHD)		3- VT	11- Nc	19- A1
		4- DT	12- Gnd ⁽²⁾	20- Nc
	25- Gnd	5- Gnd ⁽²⁾	13- V+	21- Nc
		6- Nc	14- A6	22- RF IN
		7- Nc	15- A5	23- Gnd ⁽²⁾
		8- RF OUT	16- A4	24- Nc

⁽¹⁾ The package outline drawing included in this data-sheet is given for indication. Refer to the application note AN0017 (<http://www.ums-gaas.com>) for exact package dimensions.

⁽²⁾ It is strongly recommended to ground all pins marked "Gnd" through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

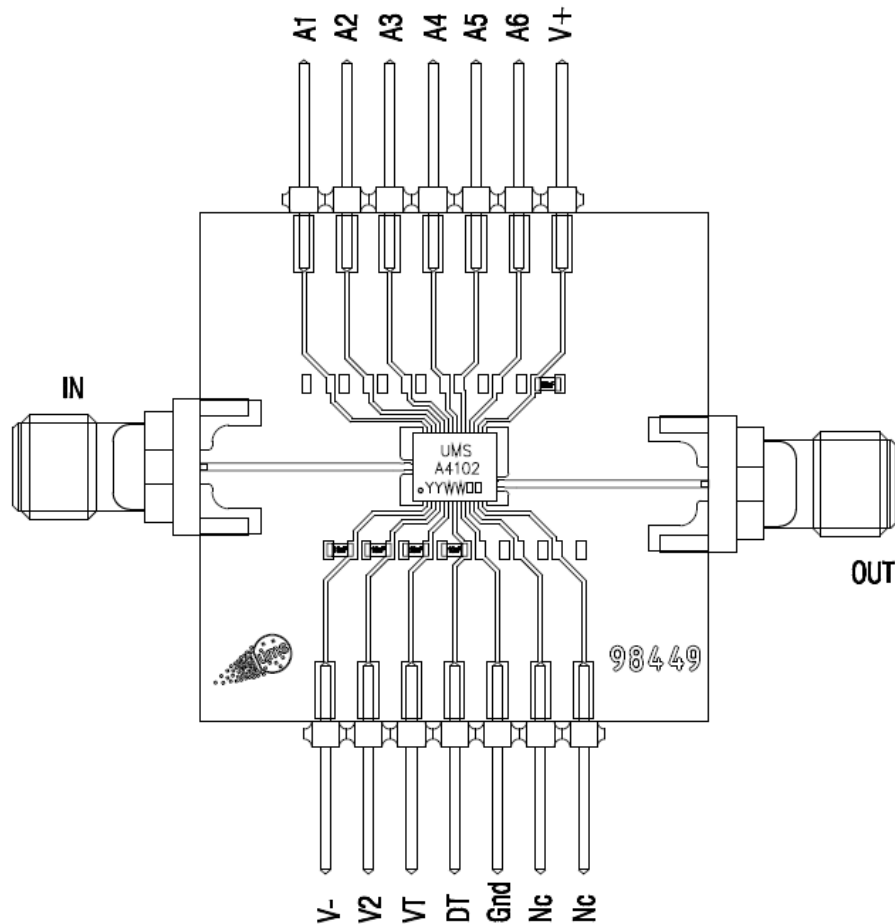
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.18mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation motherboard".



Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF $\pm 10\%$ are recommended for all Biasing accesses.
- See application note AN0017 for details.



Notes

Recommended package footprint

Refer to the application note AN0017 available at <http://www.ums-gaas.com> for package footprint recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <http://www.ums-gaas.com>.

Recommended ESD management

Refer to the application note AN0020 available at <http://www.ums-gaas.com> for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x5 package:

CHA4102-QEG/XY

Stick: XY = 20

Tape & reel: XY = 21

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