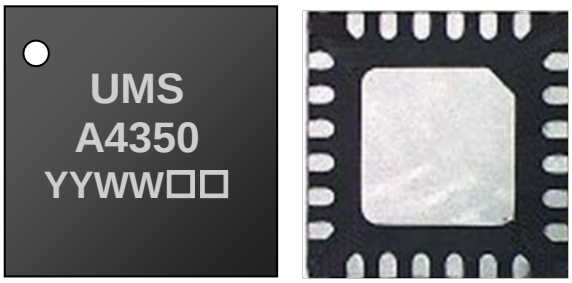
CHA4350-QDG

5.5-11.7GHz Medium Power Amplifier

GaAs Monolithic Microwave IC in SMD leadless package

Description

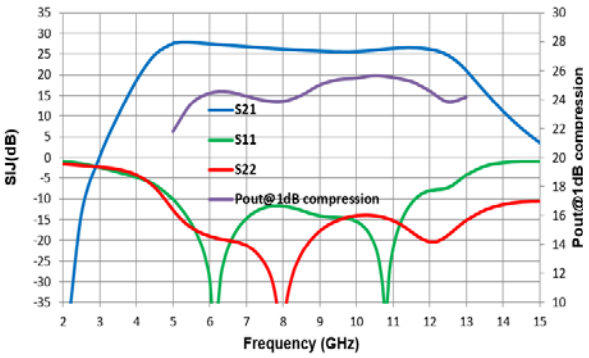
The CHA4350-QDG is a three stage monolithic medium power amplifier circuit.
It is well suited for a wide range of applications from defense to commercial communication systems.
This circuit is highly linear. Its versatile biasing condition helps to tune the performances. In addition, the circuit is fully protected against ESD.
This product is manufactured with a pHEMT process, 0.15µm gate length.
It is supplied in RoHS compliant SMD package.



Main Features

- Broadband performances: 5.5- 11.7GHz
- 26dB Linear Gain
- 24dBm output power @1dB comp.
- 32dBm output IP3
- 28% PAE@ 1dB compression
- DC bias: Vd=5.5Volt@Id=125mA
- 24L-QFN4x4

Gain & RLoss



Main Electrical Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	5.5		11.7	GHz
Gain	Linear Gain		26		dB
OIP3	Output IP3		32		dBm
Pout	Output Power @1dB comp.		24		dBm

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Specifications

Tamb.= +25°C, D1 = D2 = D3 = +5.5V, G2 (# -0.9V) set in order to get Idq = 125mA

Symbol	Parameter	Min	Typ	Max	Unit
Freq	Frequency range	5.5		11.7	GHz
Gain	Linear Gain		26		dB
ΔG	Gain variation in temperature		± 0.04		dB/°C
RL_in	Input Return Loss		-12		dB
RL_out	Output Return Loss		-13		dB
OP1dB	Output power @1dB compression		24		dBm
Psat	Saturated output power		25		dBm
OIP3	Output IP3		32		dBm
PAE	Power Added Efficiency @ 1dB compression		28		%
NF	Noise figure		5.5		dB
Idq	Quiescent Drain current		125		mA
Vg	Gate voltage		-0.9		V

These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation board".

“Power ON” sequence

1. Ground the device
2. Bias MPA gate voltage at Vg low enough (Typically: Vg ≈ -2V)
3. Apply Vds bias voltage (Typically: Vd = 5.5V)
4. Increase slowly Vgs up to quiescent bias drain current Idq
5. Apply RF signal

“Power OFF” sequence

1. Turn off RF signal
2. Bias MPA gate voltage at Vg low enough (Typically: Vg ≈ -2V)
3. Turn Vds bias voltage to 0V
4. Turn Vgs bias voltage to 0V

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	6V	V
Idq	Drain bias quiescent current	0.25	A
Vg	Gate bias voltage	-2 to +0	V
Vdg	Vd-Vg range	8	V
Pin	Input continuous power (2)	5	dBm
Tj	Junction temperature (3)	175	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) Duration < 1s.

(3) Thermal Resistance channel to ground paddle

Recommended Operating Range 4, 5

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	5.5	°C
Id	Drain bias current	125	mA
Vg	Gate bias voltage	-2 to 0	V
Pin	Maximum peak input power overdrive	5	dBm
Ta	Operating temperature range	-40 to 95	°C

(4) Electrical performances are defined for specified test conditions

(5) Electrical performances are not guaranteed over all recommended operating conditions

Temperature Range

Ta	Operating temperature range	-40 to +95	°C
Tstg	Storage temperature range	-55 to +150	°C

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad Nº	Parameter	Values	Unit
D1	12	DC Drain voltage 1st stage	5.5	V
D2	9	DC Drain voltage 2nd stage	5.5	V
D3	7	DC Drain voltage 3rd stage	5.5	V
VG	22	DC Gate voltage tuned for Idq= 125mA	-0.86	V

Electrostatic discharge sensitive device observe handling precautions!

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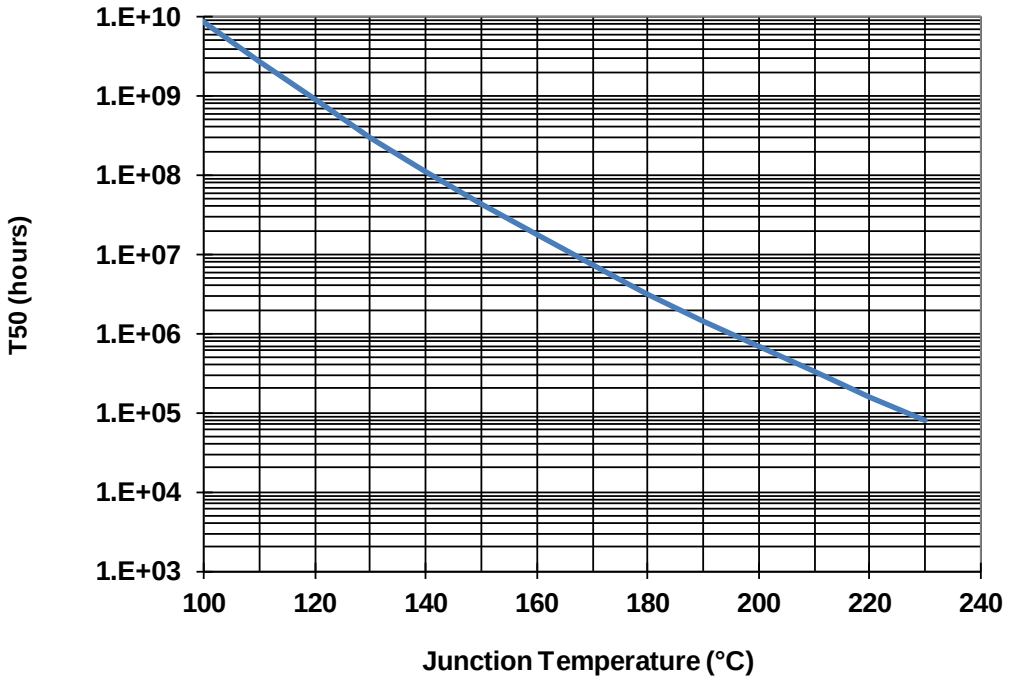
Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is only cooled down by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tcase).
The system maximum temperature must be adjusted in order to guarantee that Tjunction remains below the maximum value specified in the Absolute Maximum Ratings table.
So, the system PCB must be designed to comply with this requirement.

Parameter	Biasing conditions	Tjunction (°C)	R_{TH} (°C/W)	T50 (hours)
R_{TH} (1) Thermal Resistance (Junction to Case)	Vd= 5.5V Id= 125mA Pdiss=0.687W	142	68	9.24E+07

[1] Assuming 85°C Tcase



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Typical Package Sij parameters

Tamb.= +25°C, Vd = +5.5V, Idq = 125mA

Freq (GHz)	S11 (dB)	PhS11 (°)	S21 (dB)	PhS21 (°)	S12 (dB)	PhS12 (°)	S22 (dB)	PhS22 (°)
2,5	-1,6	102,4	-14,1	-161,1	-70,2	74,5	-1,9	-32,9
3,0	-2,3	83,4	-0,3	117,6	-64,7	56,5	-2,3	-92,5
3,5	-3,3	62,2	9,7	53,6	-63,9	3,9	-2,9	-148,2
4,0	-4,8	37,7	18,4	-14,3	-68,5	-36,4	-4,4	159,7
4,5	-7,3	9,1	24,8	-92,7	-73,1	-38,8	-8,1	110,1
5,0	-11,2	-22,4	27,6	-173,8	-74,4	-10,5	-14,7	79,6
5,5	-16,7	-58,3	27,8	118,3	-74,1	35,6	-19,2	80,4
6,0	-21,8	-105,8	27,3	62,9	-68,8	48,0	-20,7	67,6
6,5	-22,4	-163,8	26,9	15,3	-67,5	29,2	-22,9	41,2
7,0	-20,5	160,4	26,6	-28,1	-65,0	14,1	-24,9	2,5
7,5	-19,5	139,3	26,5	-69,1	-65,7	-8,4	-24,8	-43,6
8,0	-19,1	126,6	26,4	-108,5	-65,2	-29,2	-22,6	-81,6
8,5	-19,0	122,8	26,5	-148,2	-63,8	-58,7	-19,6	-113,6
9,0	-17,7	120,2	26,3	171,4	-61,3	-90,6	-18,2	-145,3
9,5	-16,2	111,5	26,0	132,8	-60,0	-117,4	-18,0	-169,3
10,0	-15,1	96,5	25,7	95,9	-56,9	-150,1	-18,6	172,0
10,5	-14,5	74,8	25,8	59,2	-55,9	-172,1	-19,7	162,9
11,0	-15,0	41,7	26,2	18,9	-55,3	169,0	-19,7	159,8
11,5	-15,2	-24,5	26,8	-26,8	-54,2	158,5	-18,4	163,5
12,0	-9,9	-109,3	26,7	-81,9	-52,3	152,9	-16,0	156,9
12,5	-5,1	-172,5	24,3	-141,7	-48,7	140,2	-13,9	140,7
13,0	-3,4	146,0	20,1	168,7	-47,7	114,5	-13,7	124,5
13,5	-2,6	119,2	15,8	129,1	-46,7	97,7	-13,3	114,8
14,0	-2,2	98,4	11,8	95,5	-47,2	84,1	-13,0	106,3
14,5	-1,9	81,8	8,1	64,1	-47,7	72,9	-12,8	100,7
15,0	-1,7	67,9	4,6	34,5	-46,5	69,7	-12,0	96,7
15,5	-1,4	55,6	1,1	6,5	-46,0	54,8	-11,2	89,7
16,0	-1,2	43,5	-2,3	-20,5	-45,2	34,8	-10,6	83,2
16,5	-1,1	31,9	-5,6	-46,1	-46,0	7,3	-10,1	78,7
17,0	-1,0	21,5	-8,9	-71,5	-48,4	-32,8	-9,4	74,2
17,5	-0,9	11,7	-12,1	-96,6	-55,3	-105,2	-8,6	69,7
18,0	-0,8	1,9	-15,4	-122,2	-54,2	130,8	-7,6	64,7
18,5	-0,8	-7,8	-18,8	-147,1	-49,9	88,4	-6,7	58,5
19,0	-0,9	-16,4	-22,4	-172,0	-49,3	88,1	-5,7	51,6

The Sij measurement calibration planes are defined in the paragraph “Definition of the Sij reference planes”.

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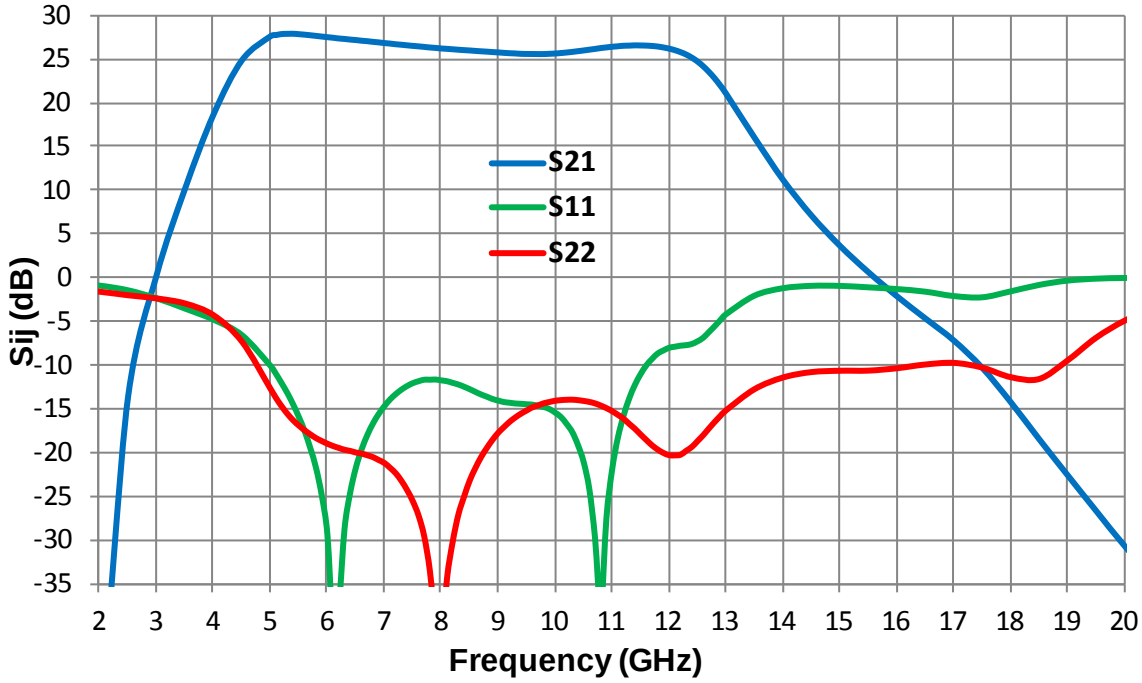
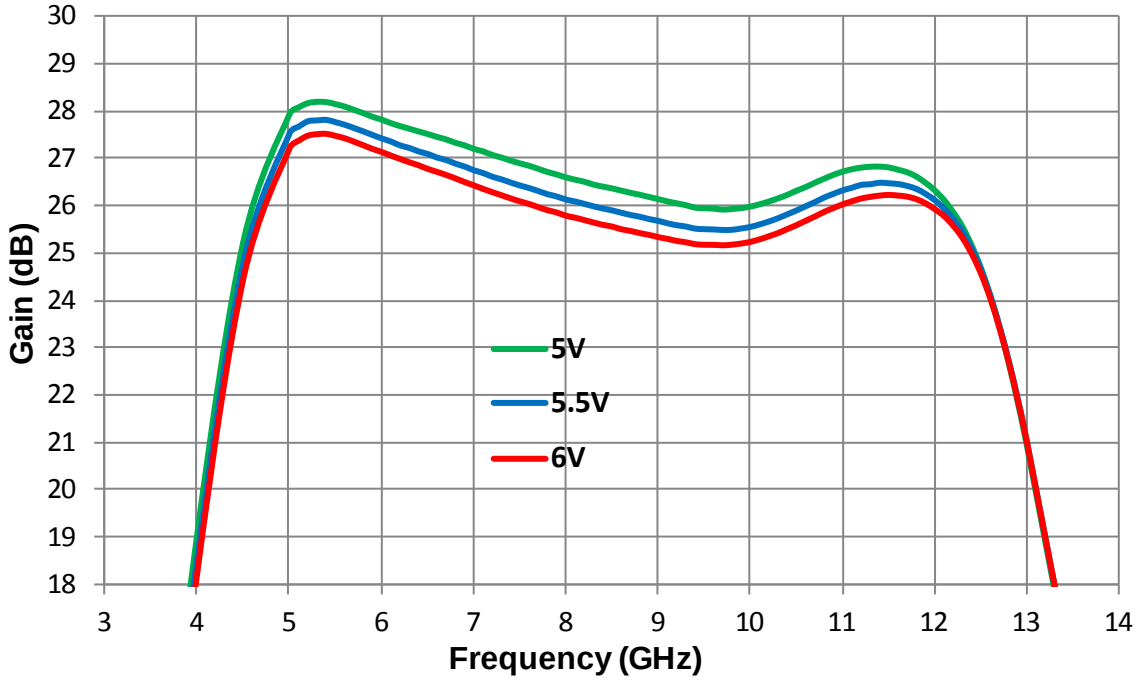
Typical Board Measurements

Tamb.= +25°C, Idq = 125mA
Measurement performed in the QFN plans access.

Linear Gain & Return Loss
Vd = +5.5V



Linear Gain versus Frequency
Vd = +5.0V / +5.5V / +6.0V



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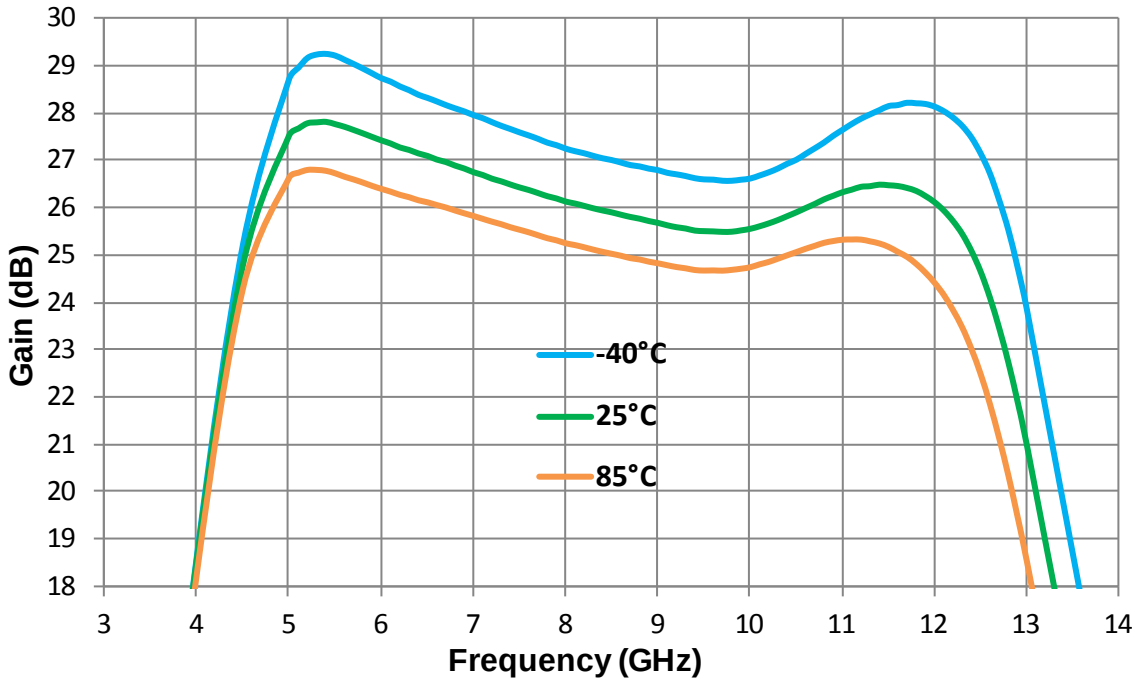
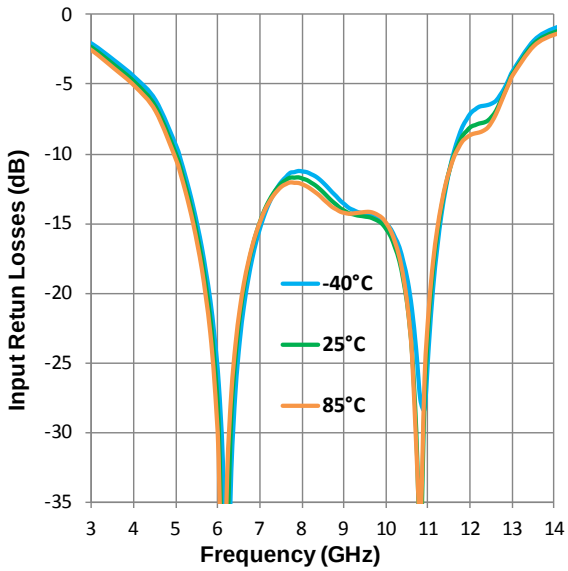
Typical Board Measurements

Tamb.= +25°C, Vd = +5.5V, Idq = 125mA
Measurement performed in the QFN plans access.

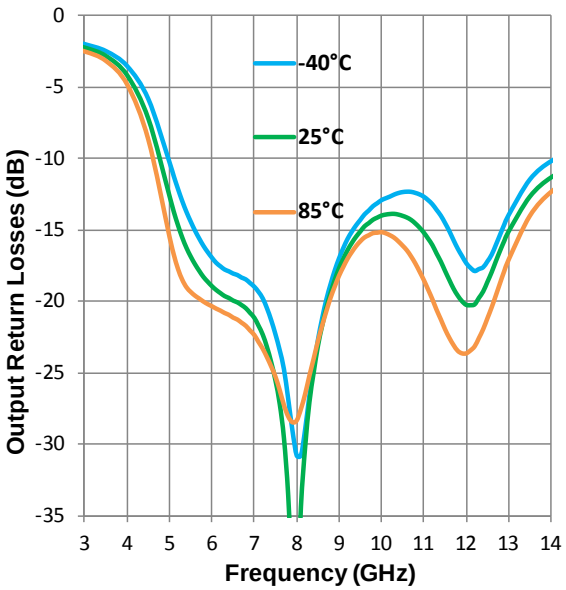
Linear Gain versus Frequency in Temperature



Input Return Losses versus Frequency in Temperature



Output Return Losses versus Frequency in Temperature



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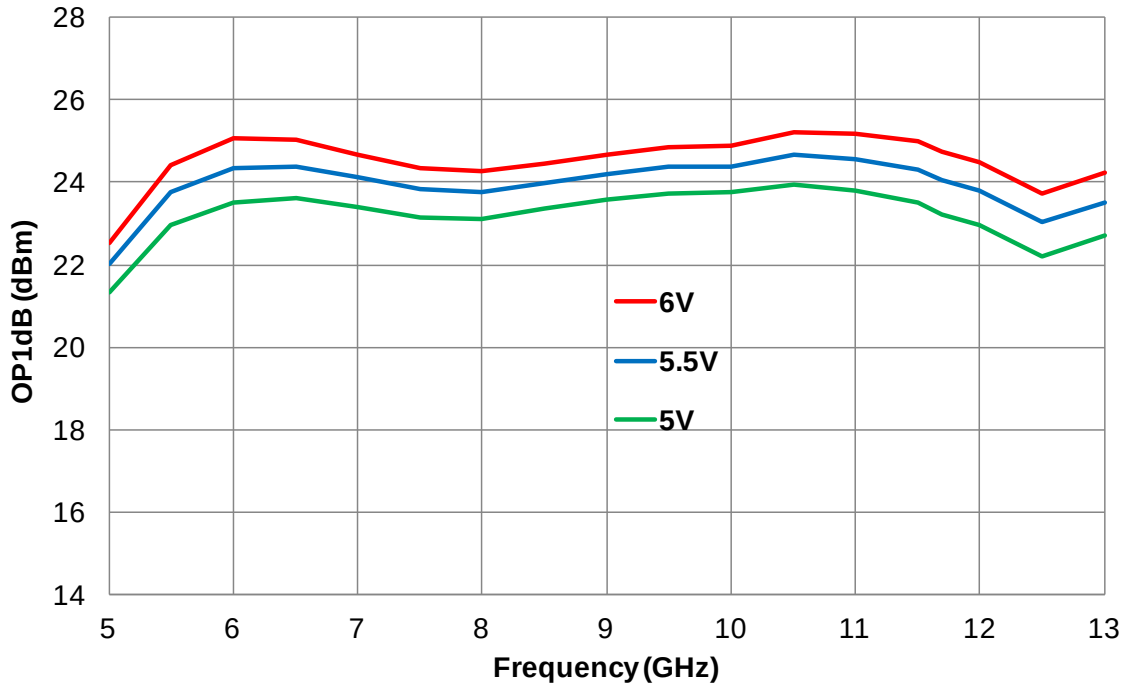
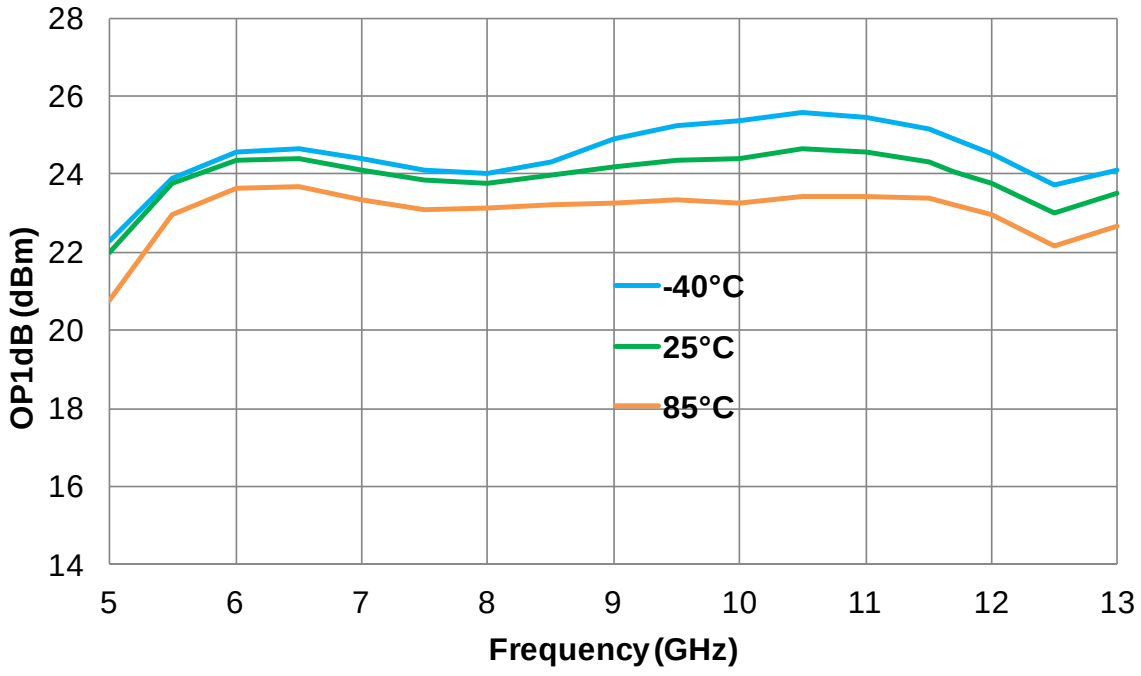
Typical Board Measurements

Tamb.= +25°C, Idq = 125mA
Measurement performed in the QFN plans access.

Output power at 1 dB Compression versus Frequency
Vd = +5.0V / +5.5V / +6.0V



Output power at 1 dB Compression versus Frequency in Temperature
Vd = +5.5V



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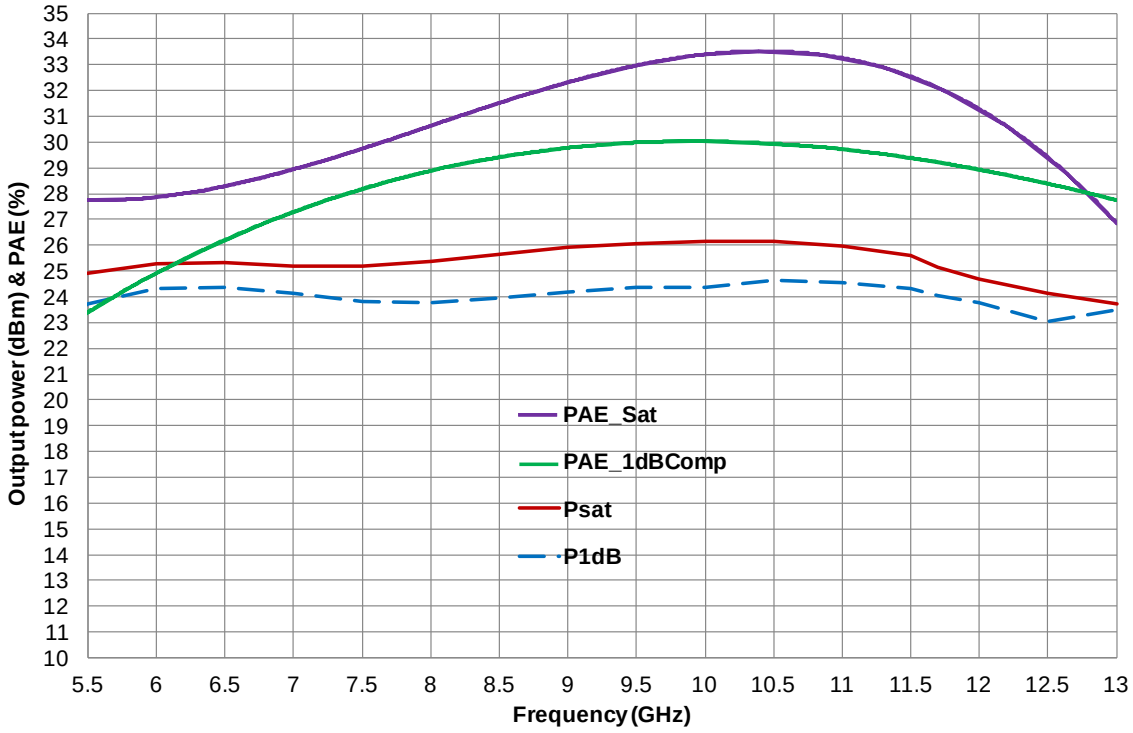
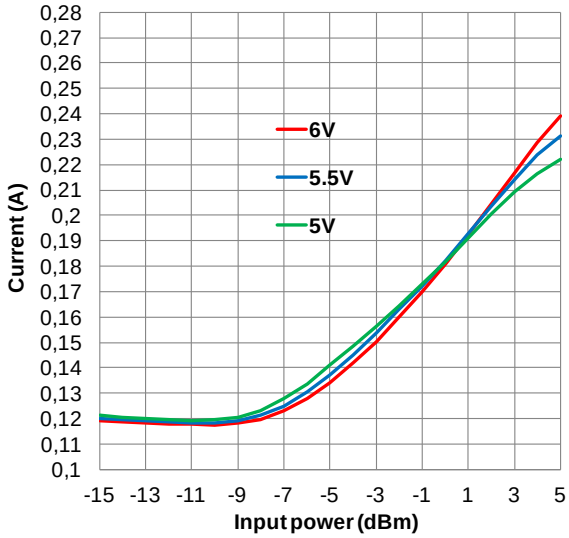
Typical Board Measurements

Tamb.= +25°C, Idq = 125mA
Measurement performed in the QFN plans access.

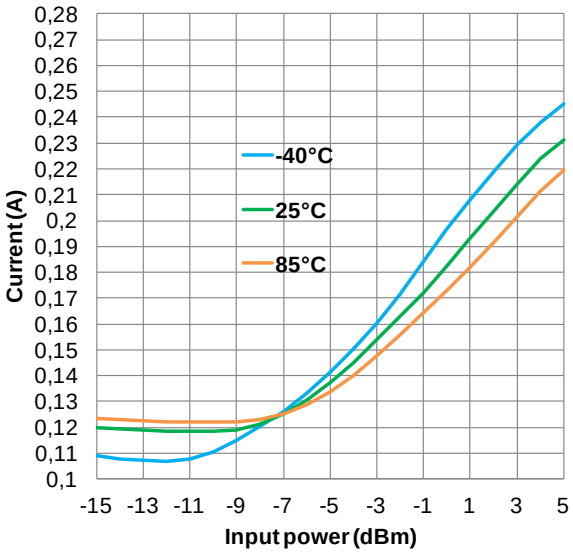
Output Power & PAE versus Frequency
Vd = +5.5V



Total Drain Current versus Input Power at 9GHz
Vd = +5.0V / +5.5V / +6.0V



Total Drain Current versus Input Power at 9GHz in Temperature
Vd = +5.5V



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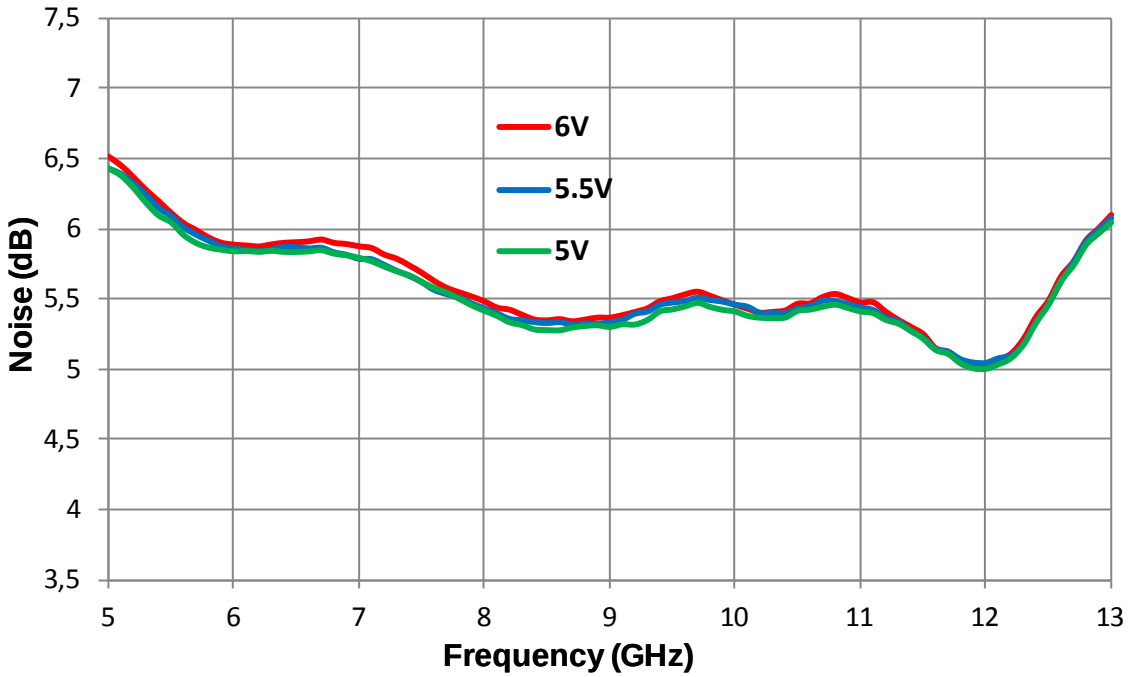
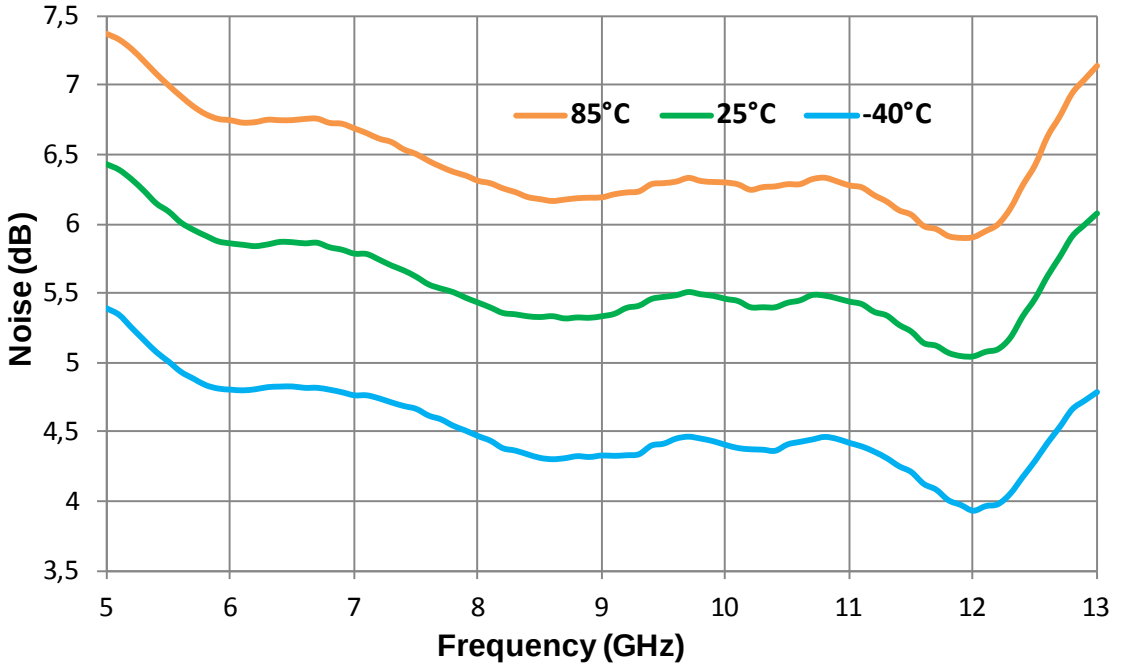
Typical Board Measurements

Tamb.= +25°C, Idq = 125mA
Measurement performed in the QFN plans access.

Noise Figure versus Frequency
Vd = 5.0V / 5.5V / 6.0V



Noise Figure versus Frequency in Temperature
Vd = 5.5V



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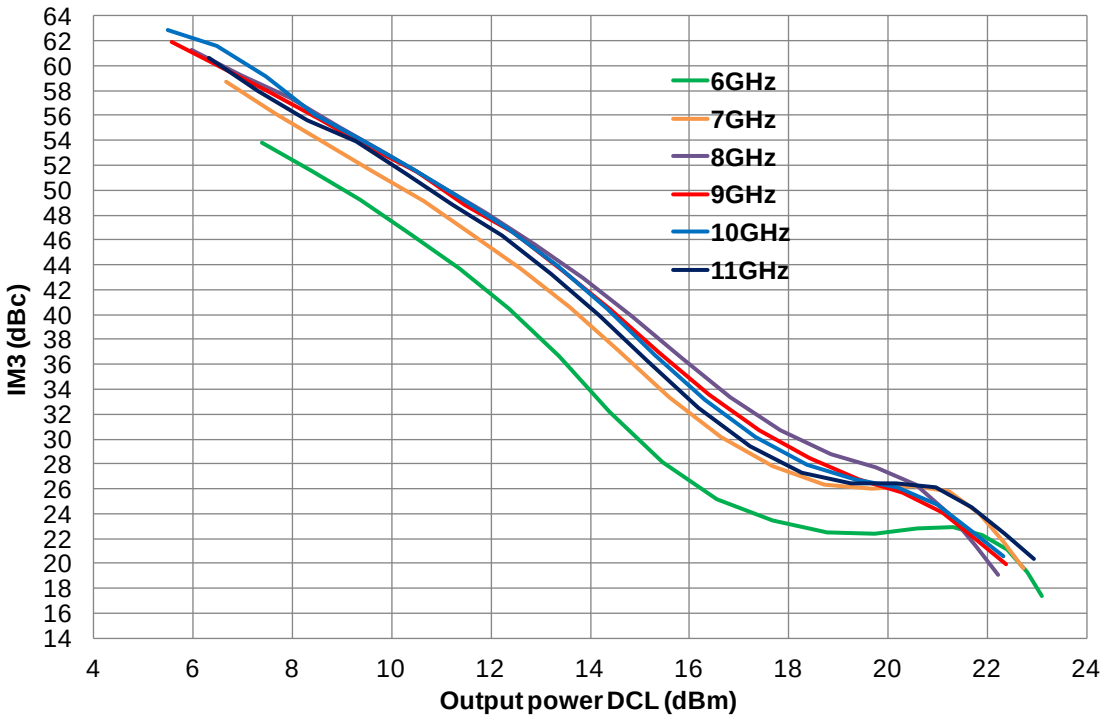
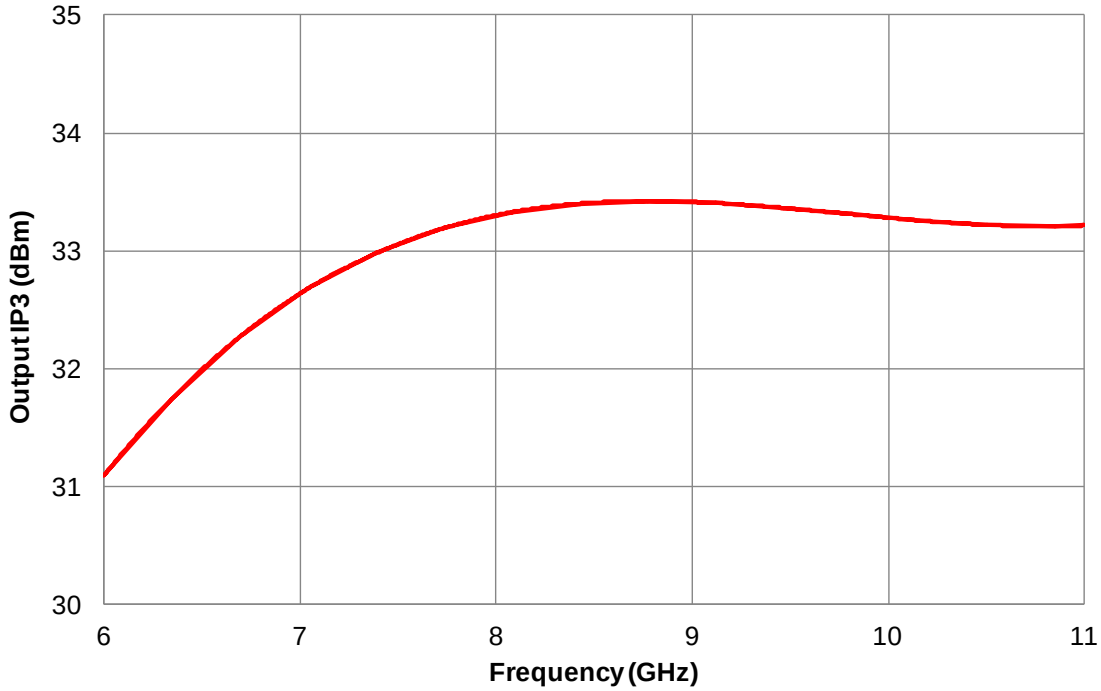
Typical Board Measurements

Tamb.= +25°C, Vd = +5.5V, Idq = 125mA
Measurement performed in the QFN plans access.

Output IM3 versus Output Power



Output IP3 versus Frequency



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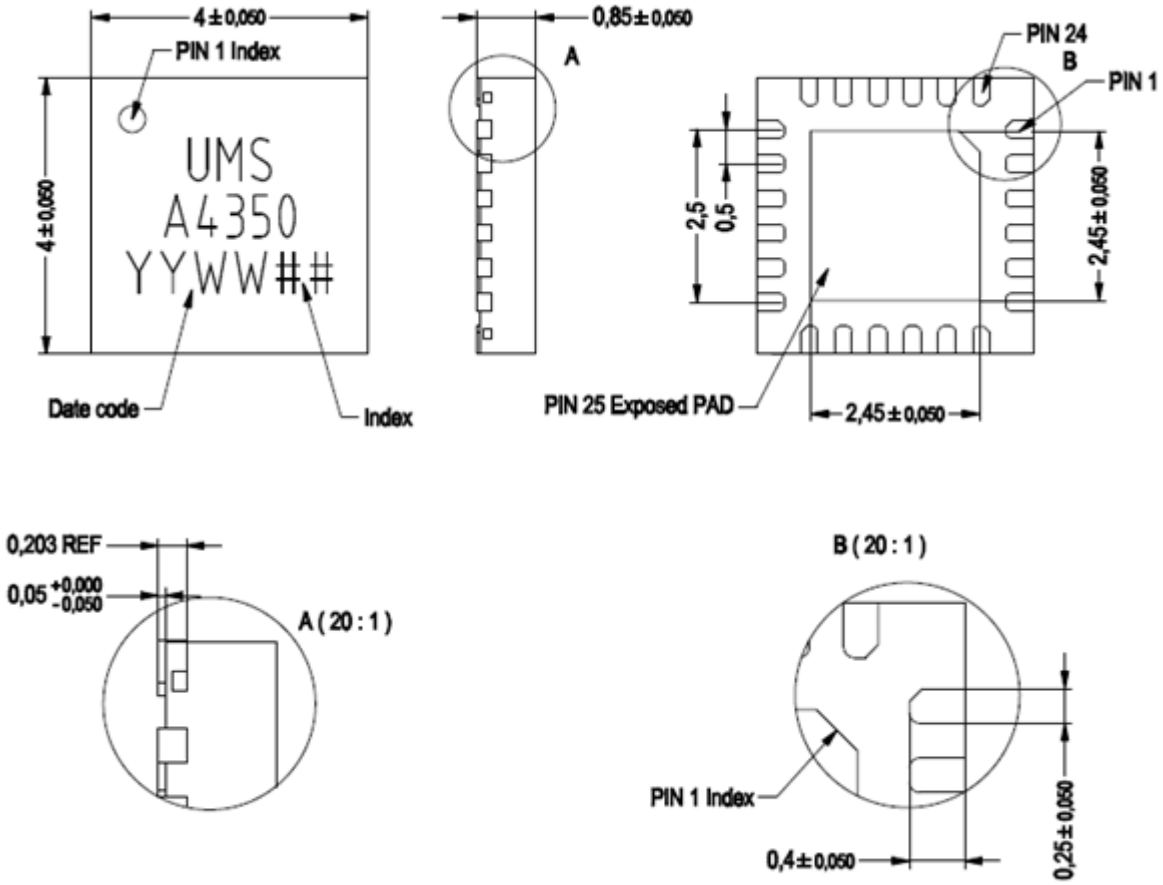
Package outline (1)



Matte tin, Lead Free (Green)	1- Gnd(2)	11- Nc	21- Nc
Units : mm	2- Gnd(2)	12- D1	22- Vg
From the standard : JEDEC MO-220	3- Gnd(2)	13- Gnd(2)	23- Nc
(VGGD)	4- RFout	14- Gnd(2)	24- Nc
17- GND	5- Gnd(2)	15- RFin	25- Gnd(2)
	6- Gnd(2)	16- Gnd(2)	
	7- D3	17- Gnd(2)	
	8- Gnd(2)	18- Gnd(2)	
	9- D2	19- Nc	
	10- Nc	20- Nc	

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (https://www.ums-rf.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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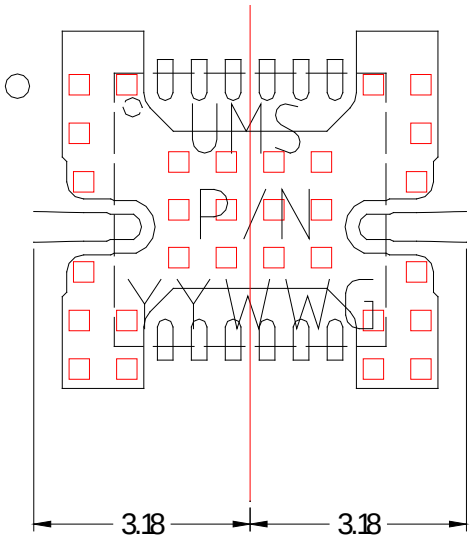
Definition of the Sij reference planes

The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 3.18mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended in paragraph "Evaluation mother board".



ESD sensitivity

Standard	Value
MIL-STD-1686C	HBM Class 1 (<2000V)
ESD STM5.1-1998	HBM Class 0 (<250V)

Package Information

Parameter	Value
Package body material	RoHS-compliant
	Low stress Injection Molded Plastic
Lead finish	100% matte tin (Sn)
MSL Rating	MSL1

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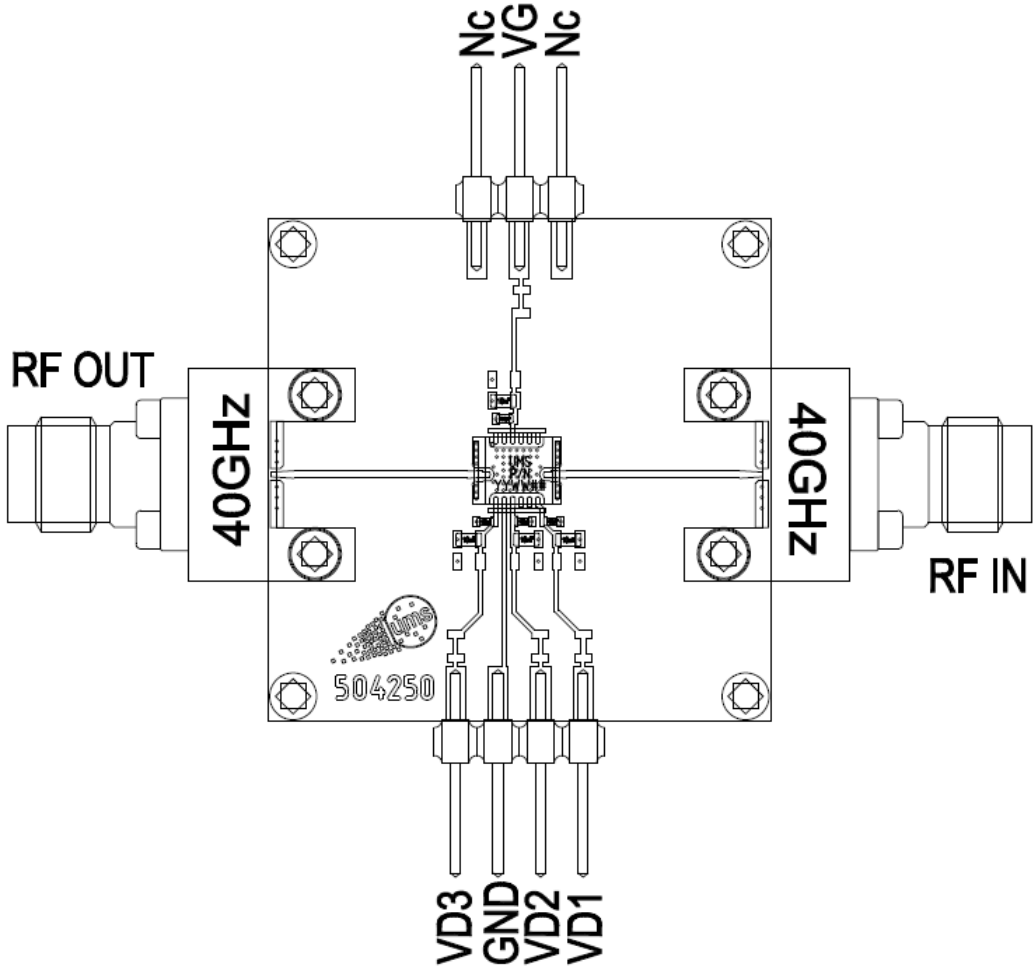
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF and 100pF ±10% are recommended for all DC accesses.
- See application note AN0017 for details.
- Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.



Note: All board measurements are performed using shielded cables, even for DC bias, to ensure safe operation.

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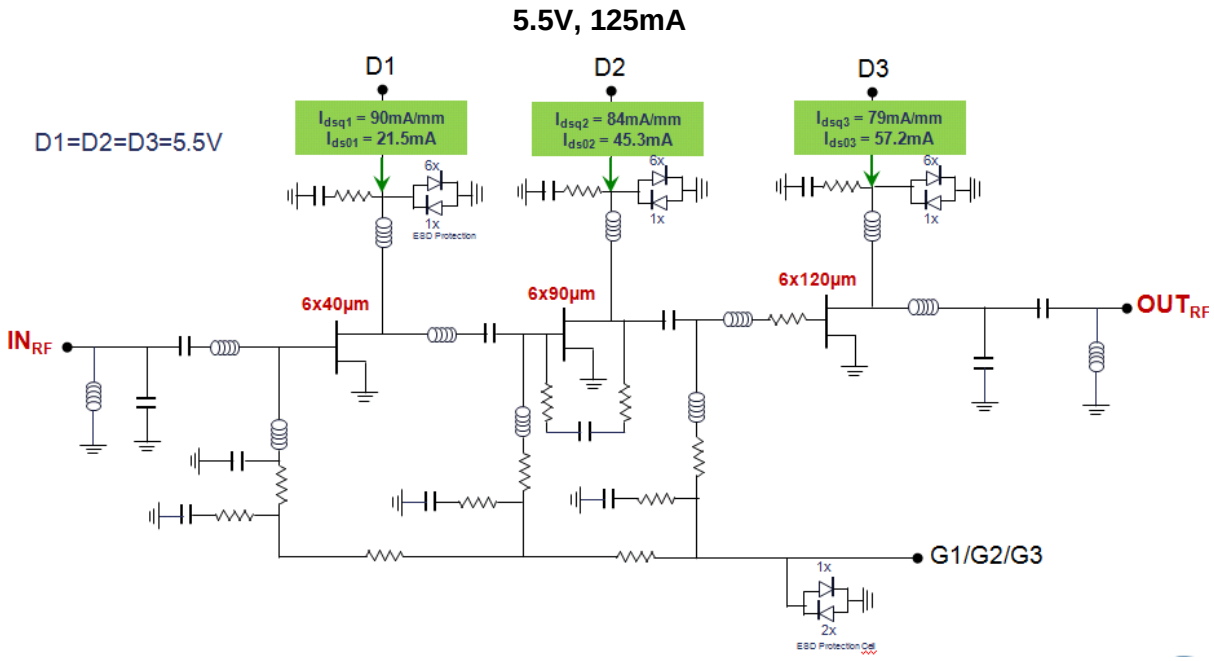
DC Schematic



Notes

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.

ESD protections are also implemented on gate and control accesses.
The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (10nF + 100pF) on the PC board, as close as possible to the package.

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Recommended package footprint

Refer to the application note AN0017 available at https://www.ums-rf.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017 at https://www.ums-rf.com.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at https://www.ums-rf.com.

Recommended ESD management

Refer to the application note AN0020 available at https://www.ums-rf.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x4 package:	CHA4350-QDG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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